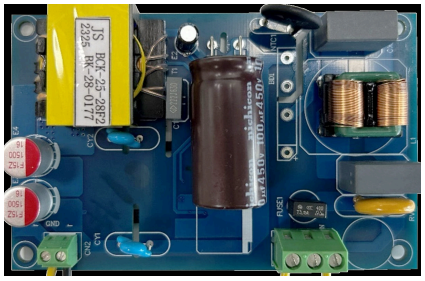
STDES-VPGAN50FL

Data brief

50 W QR open frame SMPS reference design with VIPerGaN50 and SRK1001



Fully assembled board developed for performance evaluation only, not available for sale

Product summary	
50 W QR open frame SMPS reference design with VIPerGaN50 and SRK1001	STDES-VPGAN50FL
Advanced quasi-resonant offline high voltage converter with E-mode GaN HEMT	VIPERGAN50
N-channel 100 V, 5 mOhm typ., 107 A STripFET F7 Power MOSFET in a PowerFLAT 5x6 package	STL110N10F7
Adaptive synchronous rectification controller for flyback converter	SRK1001
Applications	AC-DC Converters

Features

- Input voltage range: AC from 176 to 265 V ac with 47 Hz to 63 Hz frequency
- Output voltage: single output 12 V dc
- Maximum output power: 50 W
- Peak efficiency: >94.5%
- Form factor: 107.7 mm (L)*68.4 mm (W)*20 mm (H)

Description

The STDES-VPGAN50FL implements a quasi-resonant flyback converter based on the VIPERGAN50 HV converter with optocoupler feedback for voltage regulation.

The device combines a high performance low voltage quasi-resonant PMW controller chip with a 650V E-mode GaN HEMT in the same package.

The advanced power management with the low quiescent current helps to achieve low standby consumptions

To increase the system efficiency, the rectification is based on the SRK1001 adaptive synchronous rectification controller. This controller drives the gate of the 100V STripFET F7 technology powering the MOSFET STL110N10F7.

The evaluation board implements a robust adapter protected for output overvoltage, output undervoltage, output over power and output short-circuit.

The STDES-VPGAN50FL helps designers to develop adapters with a short bill of materials to obtain a cost-effective and fast design.

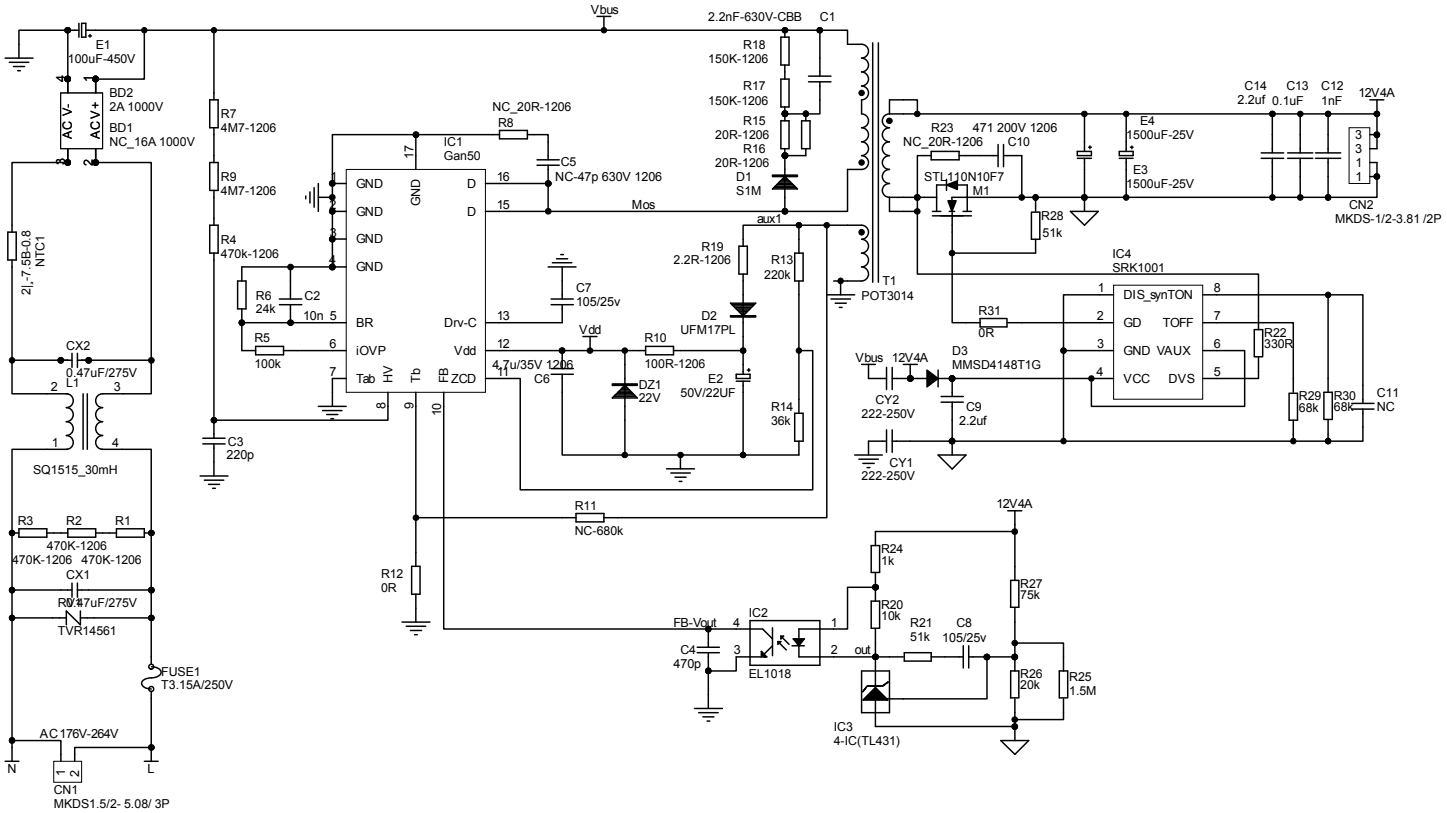
1 Electrical characteristics

Table 1. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Nominal	Max.	Unit
Input parameters						
V_{IN}	Input line voltage		176	230	265	Vrms
f_{LINE}	Input line frequency		47	50/60	63	Hz
P_{STBY}	No load input power	V_{IN}=176V_{RMS} V_{IN}=230V_{RMS}	64	98		mW
Output parameters						
V_{OUT}	Output voltage	V_{IN}=176V_{RMS}~ 264V_{RMS} I_{OUT}= 0A~ 4.15A		12		V
V_{ripple}	Output voltage ripple	Peak to peak value with 20 MHz bandwidth		110		mV
I_{OUT}	Output current		0		4.15	A
P_{OUT}	Continuous output power		0		50	W
η	Efficiency at 50 W	V_{IN}=176 Vac	93.59	94.34	94.86	%
		V_{IN}=230 Vac	92.65	94.27	95.06	

2 Schematic diagrams

Figure 1. STDES-VPGAN50FL circuit schematic



Revision history

Table 2. Document revision history

Date	Revision	Changes
20-Dec-2023	1	Initial release.

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