8-port IO-Link master based on IOLM4P L6360

Fully assembled board developed for performance evaluation only, **not available for sale**

Features

- 8-port IO-Link master STDES-8PIOLM4P (172 x 60 mm) main board, 24V power connector, 8 Port M12 connector and USB micro connector for communication
- Main controller is STM32F746ZG, Arm 32-bit Cortex®-M7 CPU with FPU, adaptive real-time accelerator (ART Accelerator) and L1-cache: 4KB data cache and 4KB instruction cache, allowing 0-wait state execution from embedded flash memory and external memories. Frequency up to 216 MHz, MPU, 462 DMIPS/2.14 DMIPS/MHz (Dhrystone 2.1), and DSP instructions
- Two IOLM4P-STM32L4 modules used and each is an IO-Link V1.1.2 compliant 4-port master controller stack
- USB micro connector for PC control tool communication
- Alternate UART port for STM32F7 module running code debug
- 8 L6360 IO-Link master transceiver ICs
- Easy to extend and integrate the IOLM4P into different application
- Fully compatible with all IO-Link devices
- On-board reverse polarity protection
- EEPROM interface for local data storage support
- SWD connector for debugging and programming capability
- Optional Ethernet RJ45 connector for specific application
- On board connector for IOLM4P master firmware updating
- RoHS compliant

Product summary

Product summary	
8-port IO-Link master based on IOLM4P L6360	STDES-8PIOLM4P
High-performance and DSP with FPU Arm Cortex-M7 MCU with 1 Mbyte of Flash memory, 216 MHz CPU	STM32F746ZGT6
IO-Link communication master transceiver IC	L6360
3 A step-down switching regulator	L7986ATR
Octal channel high side driver	VN808CM-32-E
Automation sensor transient and overvoltage protection	SPT01-335DEE
Applications	Factory Automation

Description

The STDES-8PIOLM4P is an 8-port IO-Link master design based on the IOLM4P.

The IOLM4P is an all-in-one IO-Link master 4-port solution and it has the protocol stack programmed by the ST partner TEConcept.

It enables a fast and easy 8-port IO-Link master prototype, with a competitive cost, which can greatly reduce the time to market for the customers multiport IO-Link master design.

The STDES-8PIOLM4P is a reference design board with a L6360TR as an IO-Link device transceiver.

The IOLM4P is STM32L431CB MCU with IO-Link master stack.

The STM32F746ZG is the main controller to play as gateway between USB/Ethernet and IO-Link.

The Ethernet IP function, is implemented through external Ethernet PHY KSZ8863, which has two PHY units and supports both 10BASE-T and 100BASE-TX.

The STDES-8PIOLM4P is a turnkey solution ready for industrialization.

The IOLM4P is based on a STM32F746ZG MCU preprogrammed by Arrow Electronics integrated TEConcept IO-Link master stack, easy to develop for the customer.

A dedicated SWD 5-pin connector can program the microcontroller STM32F746ZG.

This STDES-8PIOLM4P is an ST total solution with one-stop BOM purchasing.

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For further information contact your local STMicroelectronics sales office.

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1 Solution overview

The solution includes three parts:

The two IOLM4P chips which integrated the IO-Link master stack.

The main controller STM32F7 which can access the two IOLM4P chips through the SPI interface and receive commands/print all the log with the COM port TXD/RXD.

The USB controller which can easily access the two IOLM4P chips through PC program and it can be integrated with the PC tool of TEConcept control tool.

The IOLM4P has the fully protocol stack which is based on the STM32L4 chip and it has one SPI controller interface which can be used for the host controller.

The STM32F7 can run the high level master access program and then access the SPI interface of the IOLM4P chip.

The high level master access program will have to be purchased from ST partner TEConcept.

The USB controller FTDI can be used with the PC program which is also based on the high level master access program.

Figure 1. **STDES-8PIOLM4P functional block diagram**
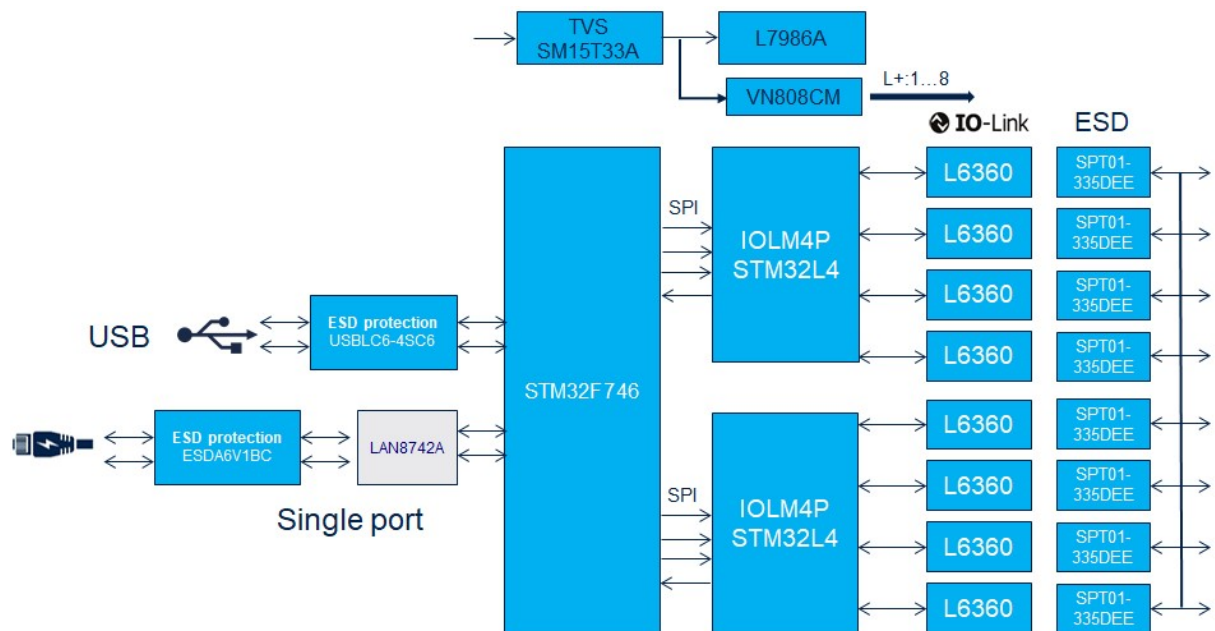
2 Schematic diagrams

Figure 2. STDES-8PIOLM4P circuit schematic (1 of 12)
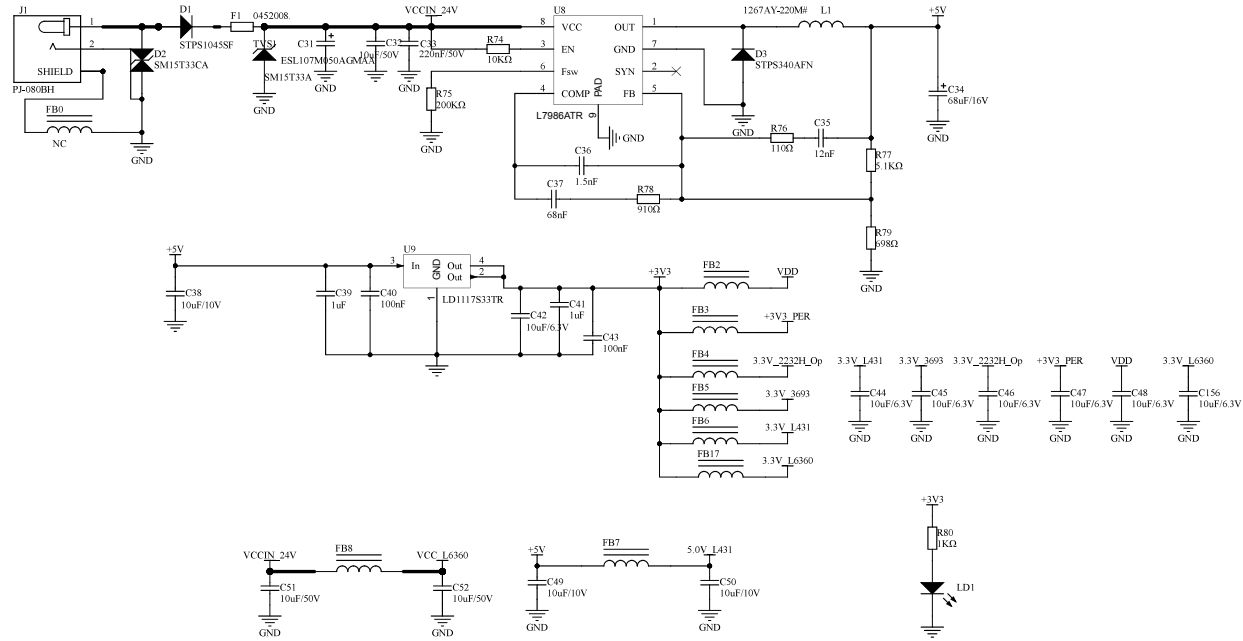
Figure 3. STDES-8PIOLM4P circuit schematic (2 of 12)
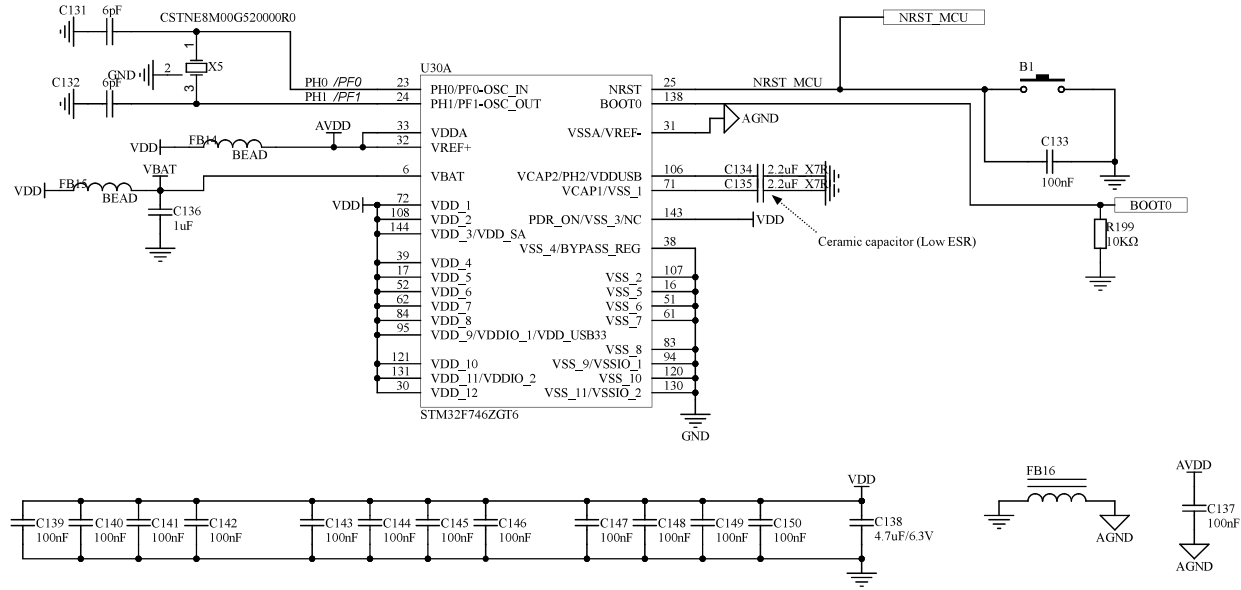
Figure 4. **STDES-8PIOLM4P circuit schematic (3 of 12)**
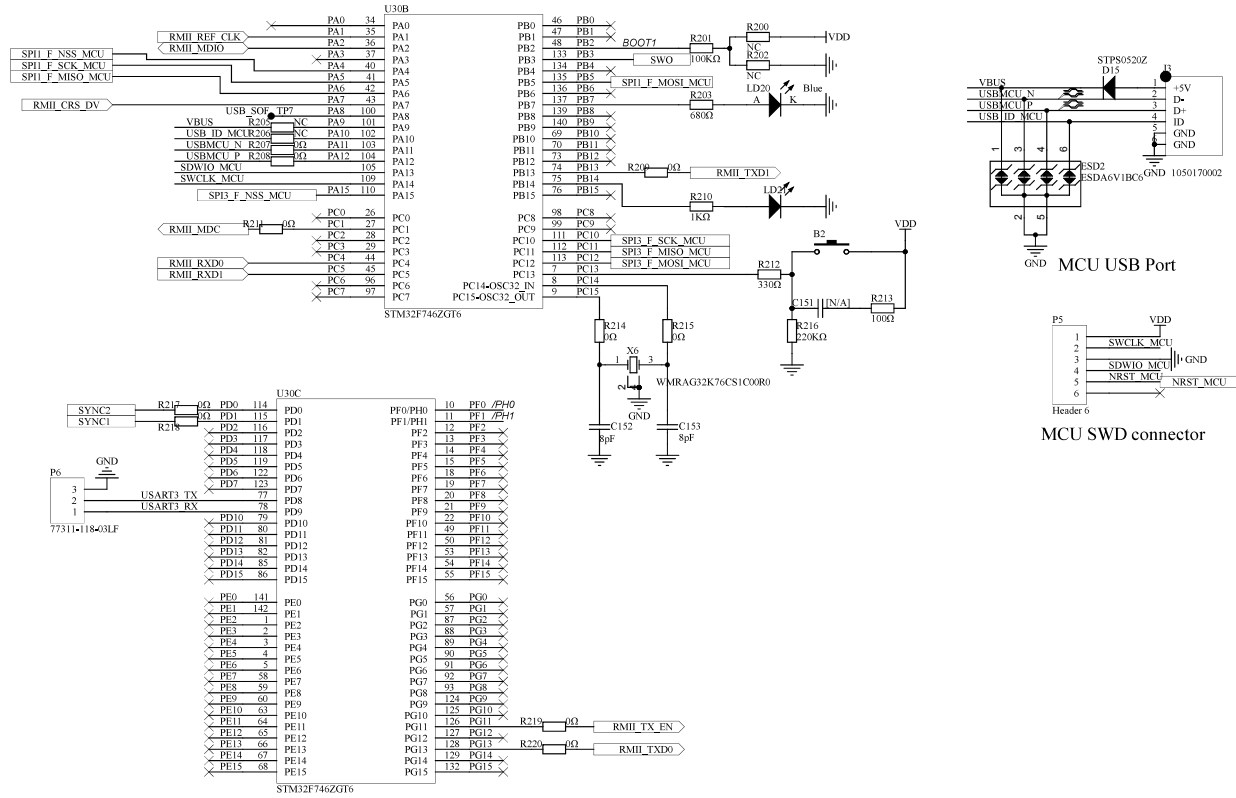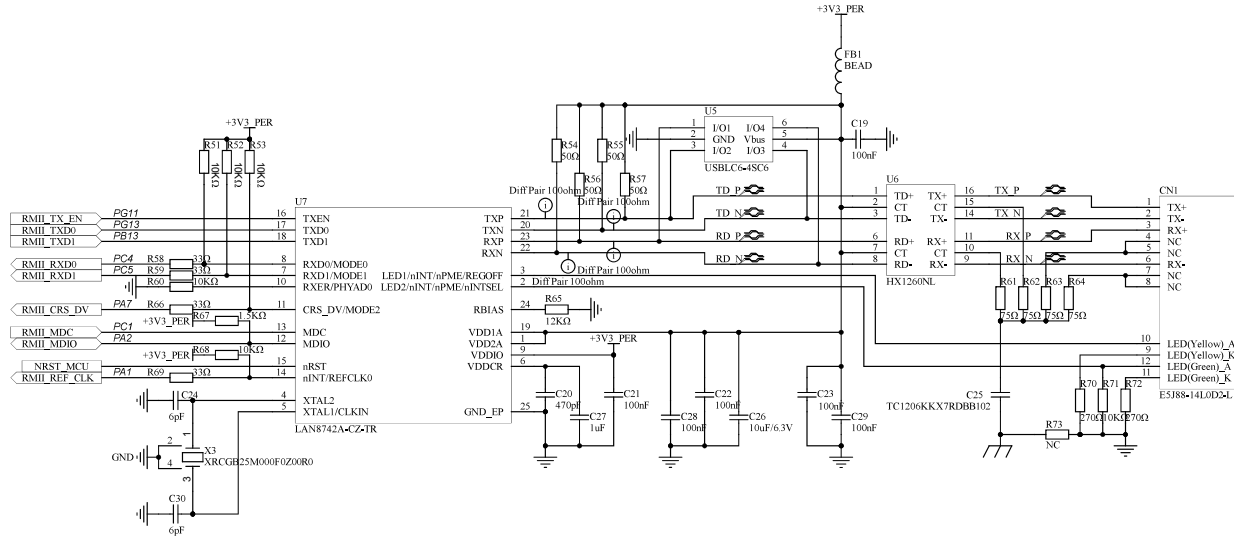

MCU USB Port

MCU SWD connector

Figure 5. STDES-8PIOLM4P circuit schematic (4 of 12)

Figure 6. **STDES-8PIOLM4P circuit schematic (5 of 12)**

EEPROM

USB to SPI

Figure 7. STDES-8PIOLM4P circuit schematic (6 of 12)

3.3V_3693

R221
2.2KΩ

P7
1
2
3

SEL_SPI1

GND

10129380-903002BLF

SEL-SPI : "0"--->MCU
SEL-SPI : "1"--->FTDI

SPI selection

U31

SPI1_F_SCK_2232H — R222 0Ω 15 — 1S1
SPI1_F_SCK_MCU — R223 0Ω 1 — 1S2

SPI1_F_MOSI_2232H — R224 0Ω 4 — 2S1
SPI1_F_MOSI_MCU — R225 0Ω 6 — 2IS2

SPI1_F_MISO_2232H — R226 0Ω 7 — 3S1
SPI1_F_MISO_MCU — R227 0Ω 9 — 3S2

SPI1_F_NSS_2232H — R228 0Ω 12 — 4S1
SPI1_F_NSS_MCU — R229 0Ω 14 — 4S2

17 — NC

VCC 2 — 3.3V_3693
D1 16 — SPI_SCK1
D2 5 — SPI_MOSI1
D3 8 — SPI_MISO1
D4 13 — SPI_NSS1
1-2-3 SEL 3 — SEL_SPI1
4SEL 10
GND 11

C154
100nF
GND

STG3693QTR

GND

From debug port or MCU

Quad SPDT switch

1-2-3-SEL	4 SEL	SWITCH 1	SWITCH 2	SWITCH 3	SWITCH 4
H	X	D1-1S1	D2-2S1	D3-3S1	X
L	X	D1-1S2	D2-2S2	D3-3S2	X
X	H	X	X	X	4D-4S1
X	L	X	X	X	4D-4S2

3.3V_3693

R230
2.2KΩ

P8
1
2
3

SEL_SPI2

GND

10129380-903002BLF

SEL-SPI : "0"--->MCU
SEL-SPI : "1"--->FTDI

SPI selection

U32

SPI2_F_SCK_2232H — R231 0Ω 15 — 1S1
SPI3_F_SCK_MCU — R232 0Ω 1 — 1S2

SPI2_F_MOSI_2232H — R233 0Ω 4 — 2S1
SPI3_F_MOSI_MCU — R234 0Ω 6 — 2IS2

SPI2_F_MISO_2232H — R235 0Ω 7 — 3S1
SPI3_F_MISO_MCU — R236 0Ω 9 — 3S2

SPI2_F_NSS_2232H — R237 0Ω 12 — 4S1
SPI3_F_NSS_MCU — R238 0Ω 14 — 4S2

17 — NC

VCC 2 — 3.3V_3693
D1 16 — SPI_SCK2
D2 5 — SPI_MOSI2
D3 8 — SPI_MISO2
D4 13 — SPI_NSS2
1-2-3 SEL 3 — SEL_SPI2
4SEL 10
GND 11

C155
100nF
GND

STG3693QTR

GND

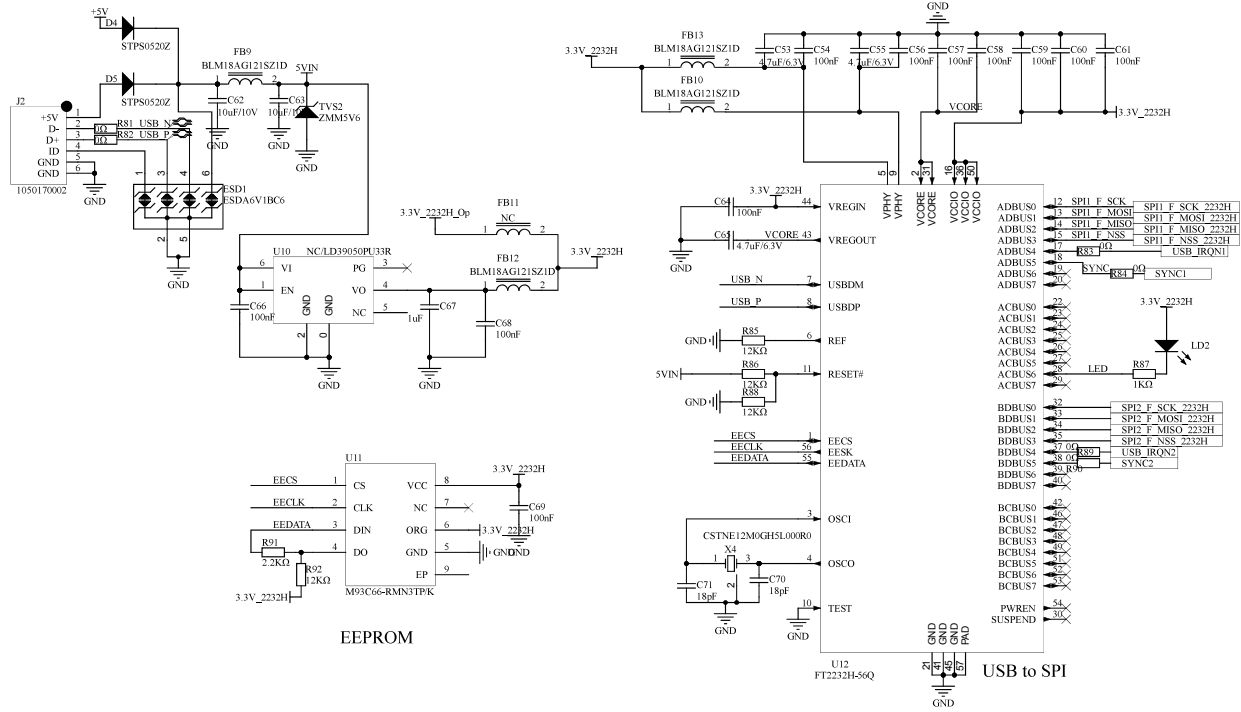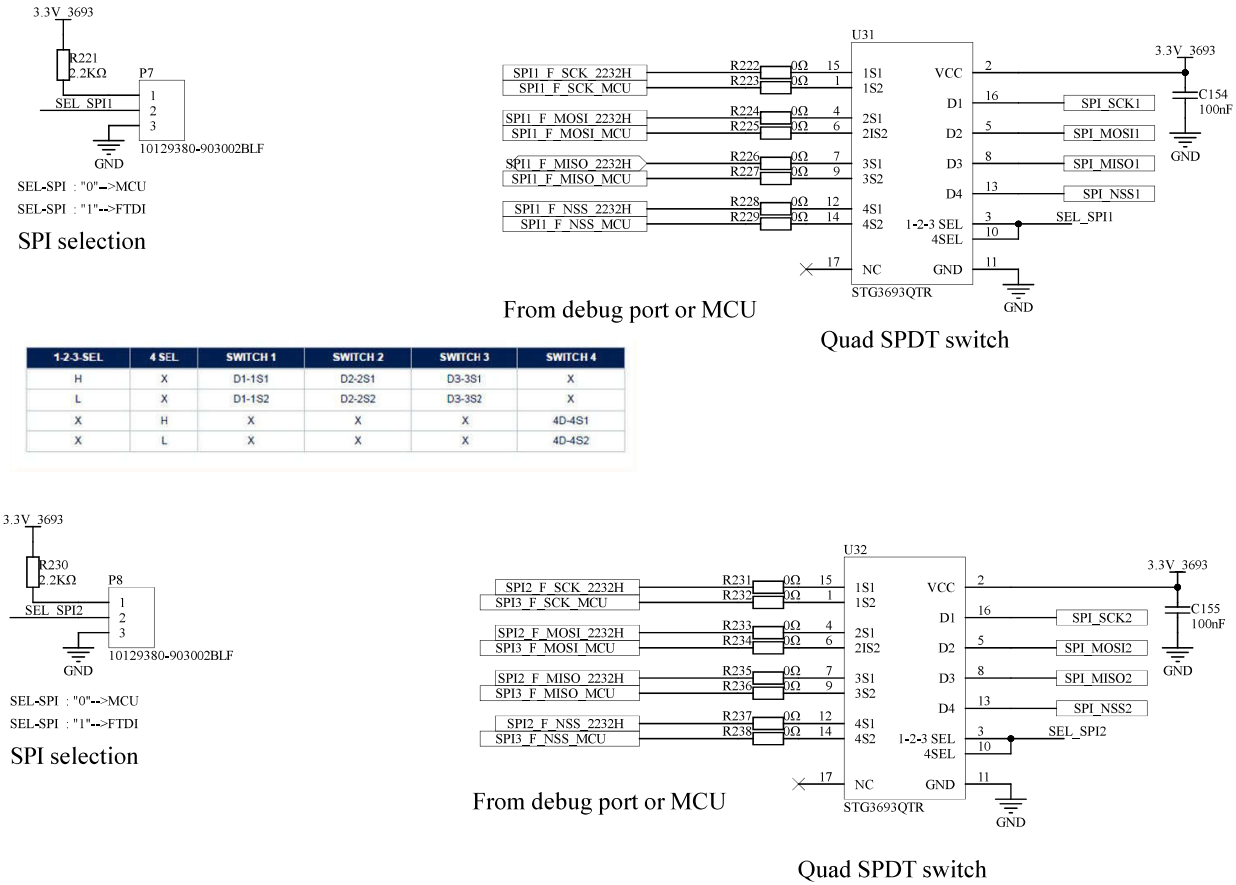From debug port or MCU

Quad SPDT switch

Figure 8. STDES-8PIOLM4P circuit schematic (7 of 12)

L6360
1A-1D: Boost L+
2A-2D: Out_I/Q
3A-3D: EN_L+
4A: RESPHY
4B-4D: not use

U1

STM32L431RBT6

Pin	Signal		Pin	Signal
20	SPI1_NSS		10	1A/MISO
15	SPI1_SCK		11	1B/MOSI
22	SPI_MISO		29	1C/SCK
23	SPI_MOSI		33	1D/NSS

SPI_NSS1 20 SPI1_NSS
SPI_SCK1 15 SPI1_SCK
SPI_MISO1 22 SPI_MISO
SPI_MOSI1 23 SPI_MOSI
R1 0R

I2C1_SDA1 59 I2C1_SDA
I2C1_SCL1 58 I2C1_SCL
I2C2_SDA1 30 I2C2_SDA
I2C2_SCL1 34 I2C2/SCL

R2 3.3KΩ R3 3.3KΩ R4 3.3KΩ R5 3.3KΩ
3.3V_L431
I2C2_SDA1
I2C2_SCL1

C1 18pF
5 OSC_IN
X1 ABM8G-14.7456MHZ-18-D2Y-T
C2 18pF
6 OSC_OUT
GND

SWDIO1 46 SWDIO
SWCLK1 49 SWCLK

5.0V_L431 R14 3.3KΩ R16 4.7KΩ
14 WKUP
21 USB_IRQN
USB_IRQN1
GND

3.3V_L431 R17 3.3KΩ
RESET1 7 NRST
45 SYNC
SYNC1

BOOT0_1 60 BOOT0
28 BOOT1
R24 4.7KΩ
TP1 35 TP1
TP2 36 TP2
TP3 44 TP3
GND

3.3V_L431
1 VBAT
32 VDD_1
48 VDD_2
64 VDD_3
19 VDD_4
13 VDDA
3.3V_L431 R29 10Ω
C3 100nF
GND

1A/MISO 10 1A
1B/MOSI 11 1B
1C/SCK 29 1C
1D/NSS 33 1D

2A 41 2A
2B 55 2B
2C 56 2C
2D 57 2D

3A 50 R6 470Ω 3A
3B/SPI3_SCK 51 R7 470Ω 3B
3C/SPI3_MISO 52 R8 470Ω 3C
3D/SPI3_MOSI 53 R9 470Ω 3D

4A 2 R10 470Ω 4A
4B 3 R11 470Ω 4B
4C 4 R12 470Ω 4C
4D 54 R13 470Ω 4D

IRQA 37 IRQA
IRQB 38 IRQB
IRQC 39 IRQC
IRQD 40 IRQD

EN_TXA 26 EN_TX_A
EN_TXB 27 EN_TX_B
EN_TXC 61 EN_TX_C
EN_TXD 62 EN_TX_D

UART_TX_A/PHY_ID0 42 UART_TX_A R18 0Ω UART_TX_A
UART_RX_A 43 UART_RX_A R19 0Ω UART_RX_A
UART_TX_B/PHY_ID1 16 UART_TX_B R20 0Ω UART_TX_B
UART_RX_B 17 UART_RX_B R21 0Ω UART_RX_B
UART_TX_C/PHY_ID2 24 UART_TX_C R22 0Ω UART_TX_C
UART_RX_C 25 UART_RX_C R23 0Ω UART_RX_C
UART_TX_D/PHY_ID3 9 UART_TX_D R25 0Ω UART_TX_D
UART_RX_D 8 UART_RX_D R26 0Ω UART_RX_D

VCAP_1 31
VCAP_2 47
VSS_3 63
VSS_4 18
VSSA 12
R27 0Ω R28 0Ω
GND

IO-LINK chip

3.3V_L431
C5 100nF C6 100nF C7 100nF C8 100nF C9 100nF
GND

3.3V_L431 P1
BOOT0_1 1
1
2
3
Header 3
R15 2.2KΩ
GND

P2
1 SWCLK1
2
3 SWDIO1
4
5 RESET1
6
Header 6
3.3V_L431
GND
SWD connector

U2
1 E0   VCC 8
2 E1   WC 7
3 E2   SCL 6 I2C1_SCL1
4 VSS SDA 5 I2C1_SDA1
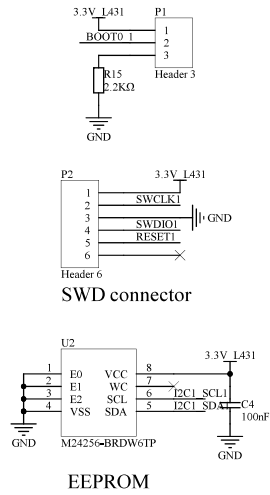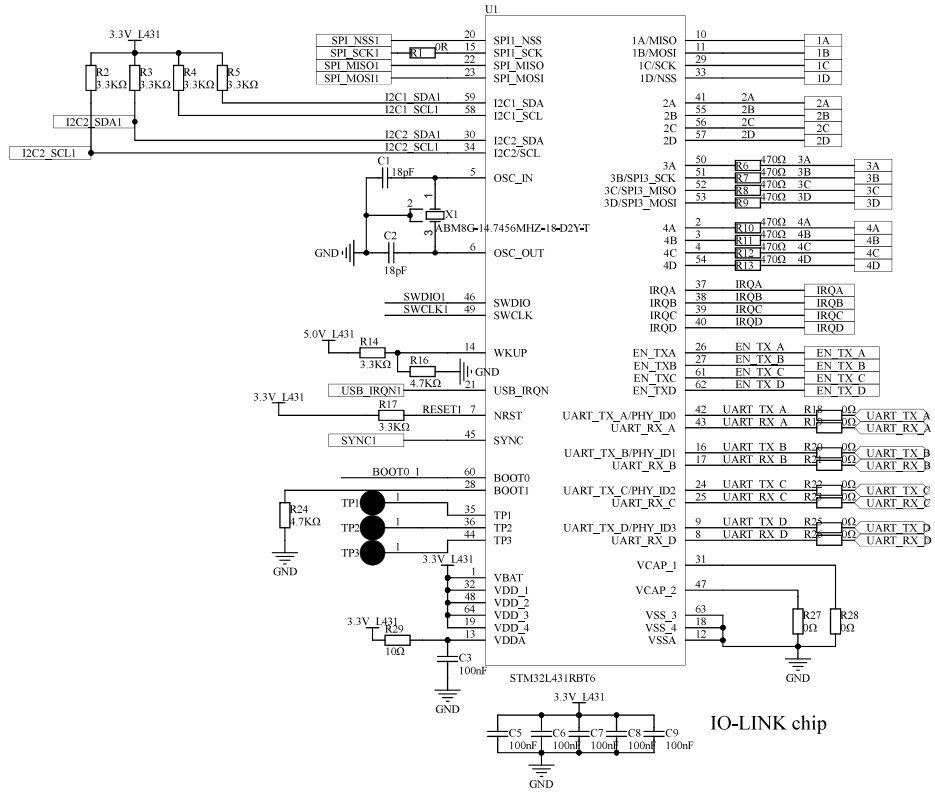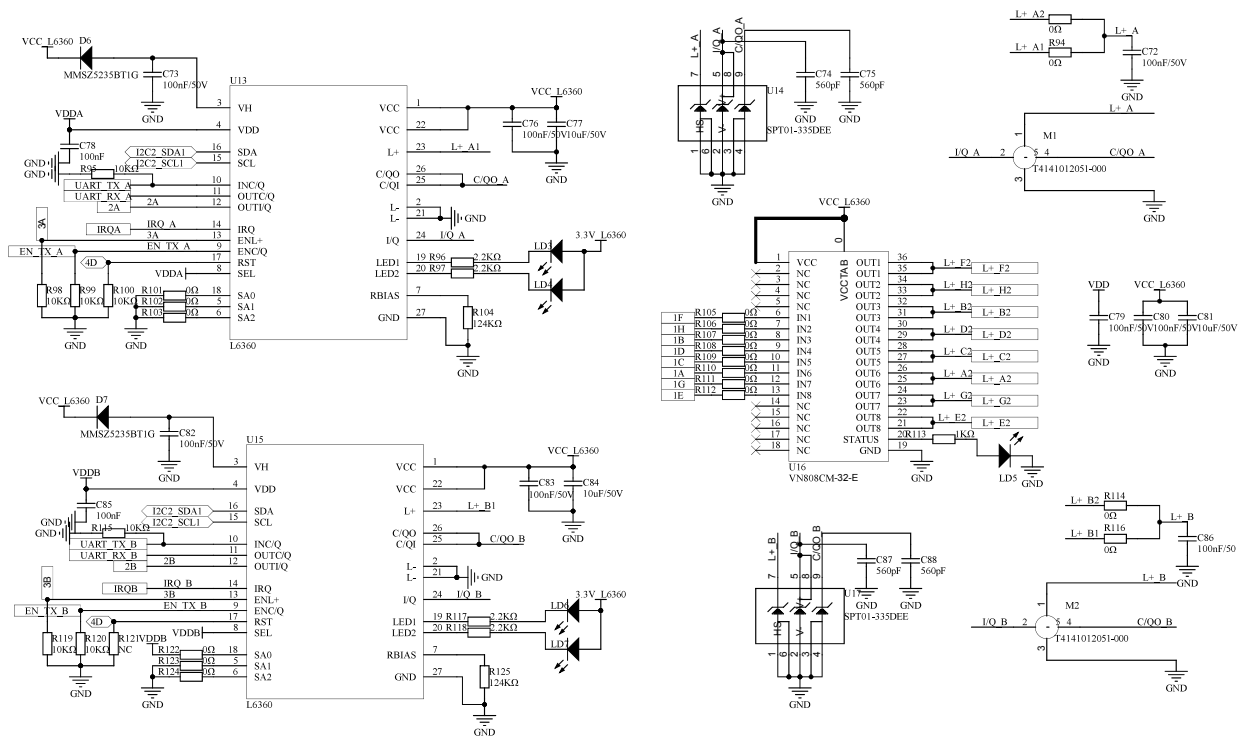M24256-BRDW6TP
GND
3.3V_L431
C4 100nF
GND
EEPROM

Figure 9. STDES-8PIOLM4P circuit schematic (8 of 12)

Figure 10. STDES-8PIOLM4P circuit schematic (9 of 12)

Figure 11. STDES-8PIOLM4P circuit schematic (10 of 12)

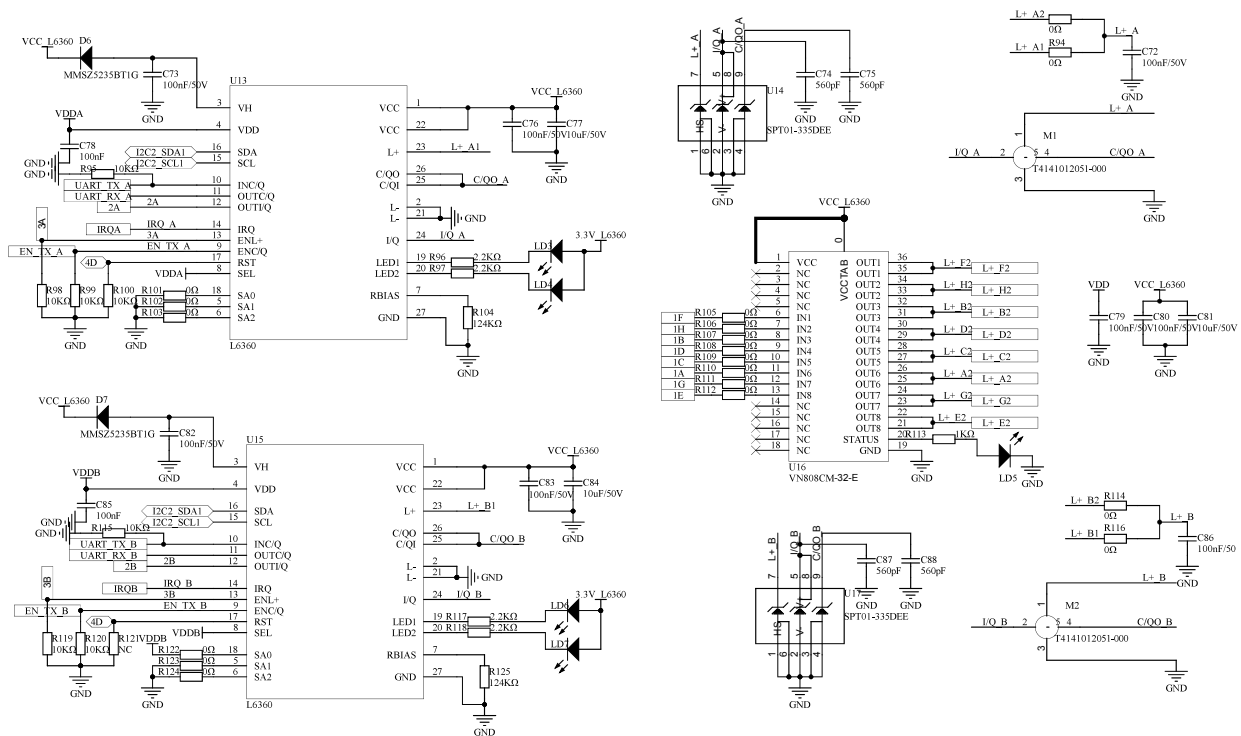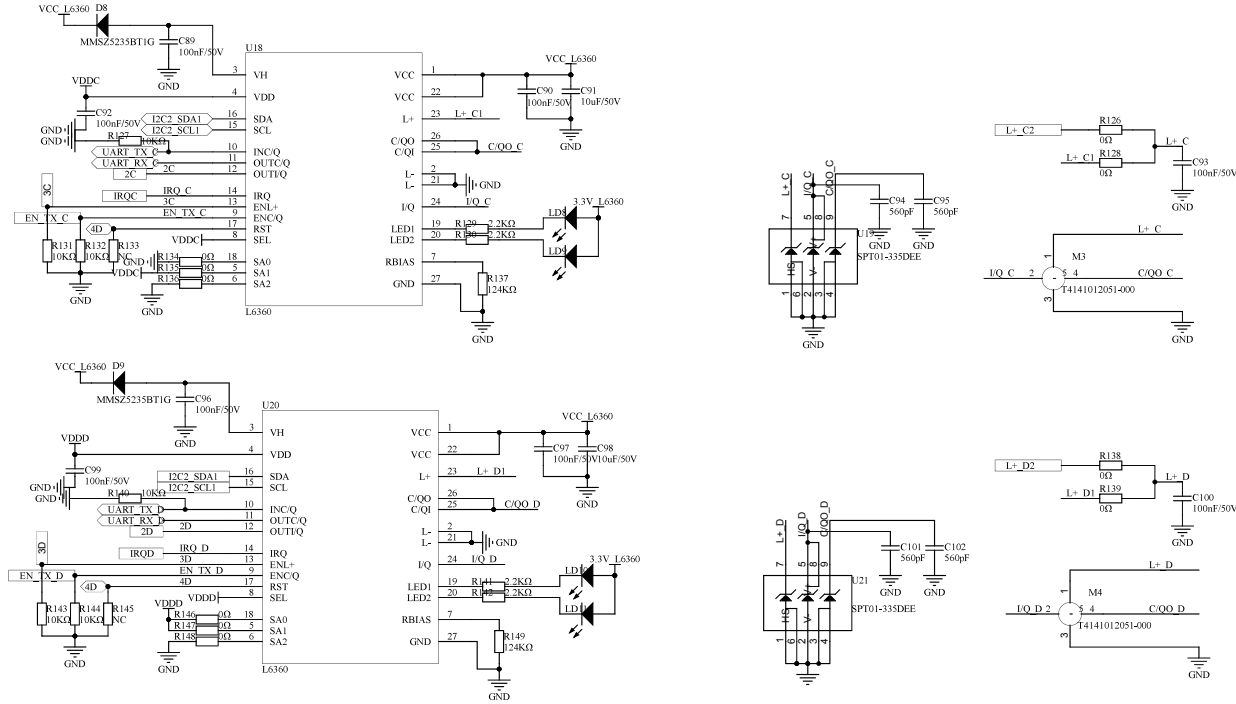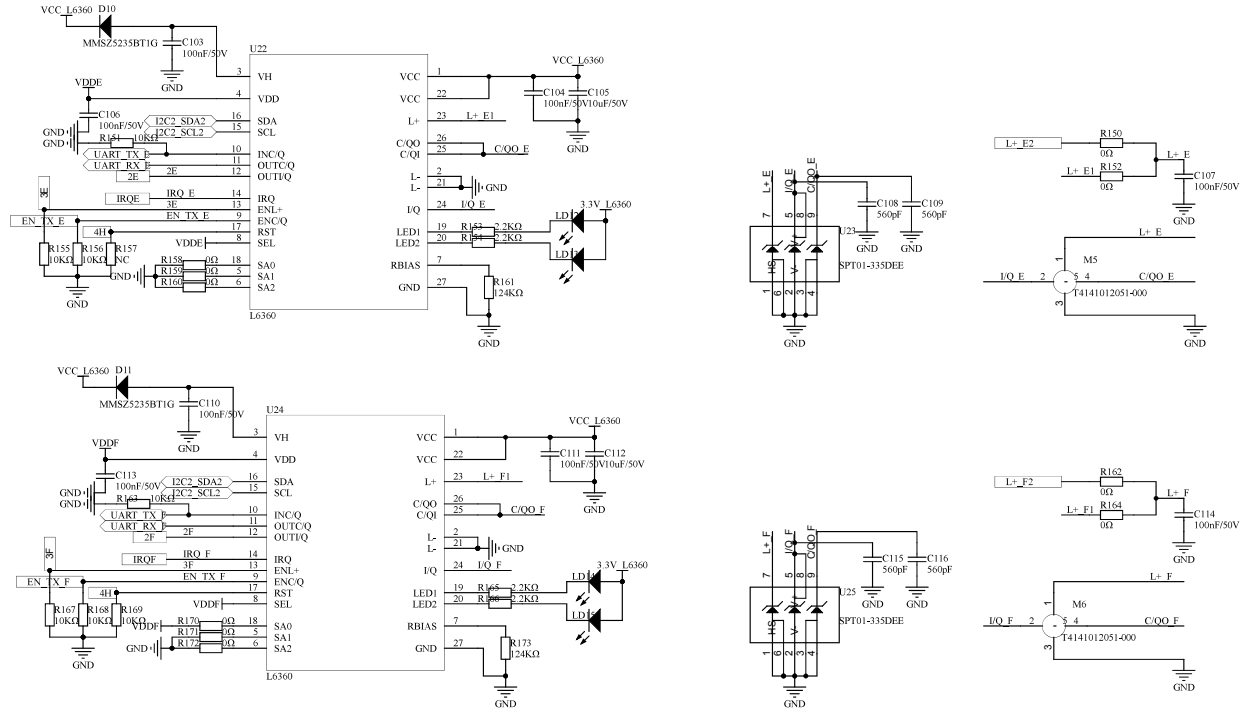# Figure 12. STDES-8PIOLM4P circuit schematic (11 of 12)

Figure 13. STDES-8PIOLM4P circuit schematic (12 of 12)

Revision history

Table 1. Document revision history

Date	Revision	Changes
23-Mar-2023	1	Initial release.

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