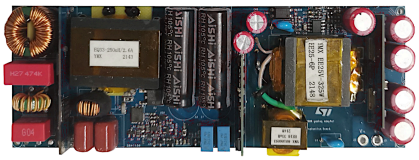
STDES-200GANADP

Data brief

19 V - 200 W adapter reference design based on STCMB1, SRK2001A and MASTERGAN1



Fully assembled board developed for performance evaluation only, not available for sale

Product summary	
19V - 200W gaming adaptor based on STCMB1, SRK2001A and MASTERGAN1	STDES-200GANADP
Transition mode (TM) PFC with X-cap discharge and LLC resonant combo controller	STCMB1
High power density 600V half-bridge driver with two enhancement mode GaN HEMTs	MASTERGAN1
N-channel 600 V, 91 mOhm typ., 25 A MDmesh M6 Power MOSFET	STL36N60M6
N-channel 60 V, 0.0024 Ohm typ., 140 A STripFET F7 Power MOSFET	STL140N6F7
Adaptive synchronous rectification controller for LLC resonant converter	SRK2001A
Applications	AC-DC Converters/ Smart Chargers and Adapters/Lighting and Controls

Features

- Input voltage range: universal AC from 90 to 264 V_{AC} with 47 to 63 Hz frequency
- Output voltage: 19 V_{DC} at 10.5 A continuous operation
- Maximum output power: 200 W
- Efficiency standards: meets CoC ver. 5 Tier 2 and DoE level 6 efficiency requirements
- Full load efficiency: >94% at 115 V_{AC}, and >95% at 230 V_{AC}
- Efficiency at 250 mW > 50%, compliant with EuP lot 6 Tier 2 limit for household and office equipment
- No load mains consumption: 118 mW at 230 V_{AC}, below European CoC ver.5 Tier 2 limit for external power supplies

Description

The STDES-200GANADP reference design is a 19 V-200 W converter tailored for the typical specification of an AC-DC adapter for all-in-one systems, gaming applications, SMPS for LED TV, and lighting applications. It ensures a wide input main range, a very low power consumption at light load, and a good average efficiency.

The architecture is based on a two-stage approach: a front-end transition mode PFC preregulator and a downstream LLC resonant half bridge converter. The PFC and LLC controllers are integrated in the STCMB1 combo IC.

The SRK2001A control implements the synchronous rectification. The PFC section uses a proprietary and constant-on-time control methodology that does not require a sinusoidal input reference, reducing the system cost and external component count. The LLC section is based on a proprietary time shift control method. This improves dynamic behavior and input ripple rejection, resulting in a cleaner output voltage.

A higher efficiency is ensured thanks to the reduction of switching and conduction losses and to the elimination of reverse recovery loss thanks to the MASTERGAN application.

Users do not have to take care anymore of GaN driving complexity to enjoy the benefits of GaN technology, thanks to the highly integrated MASTERGAN1 IC, enhancing the robustness of the application and layout simplifications.

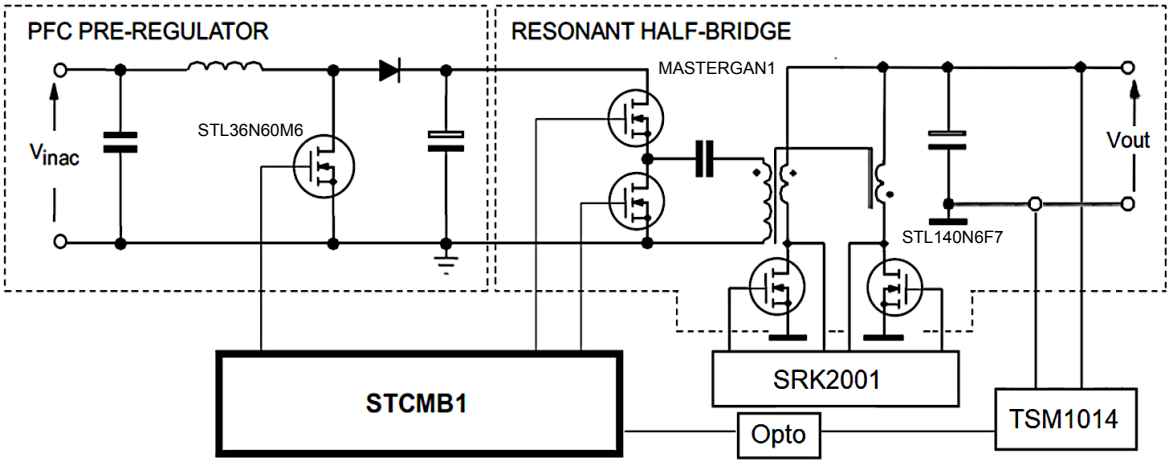
1 Electrical specifications

Table 1. STDES-200GANADP electrical specifications

Symbol	Parameter	Test conditions	Min.	Nominal	Max.	Unit
Input parameters						
V_{IN}	Input line voltage		90	115/230	264	Vrms
f_{LINE}	Input Line Frequency		47	50/60	63	Hz
P_{STBY}	No load input power	V_{IN} = 115 V_{RMS} and 230 V_{RMS}			150	mW
Output parameters						
V_{OUT}	Output voltage	VIN = 90 V_{RMS}~264 V_{RMS} I_{OUT} = 0A~3A		19		V
V_{ripple}	Output voltage ripple	Peak to peak value with 20 MHz bandwidth			250	mV
I_{out}	Output current		0		10.5	A
P_{out}	Continuous output power		0		200	W
η_{ave}	Four-point average efficiency: 25%, 50%,75%, and 100% load	At 115 V_{AC} and measured at the end on the kit		92		%
η_{ave}	Four-point average efficiency: 25%, 50%,75%, and 100% load	At 230 V_{AC} and measured at the end on the kit		93		%
Ambient and EMI parameters						
T_{AMB}	Ambient temperature	Free convection sea level	0	25	40	°C

2 Overview

Figure 1. STDES-200GANADP architecture block diagram



3 Schematic diagrams

Figure 2. STDES-200GANADP circuit schematic (1 of 4)

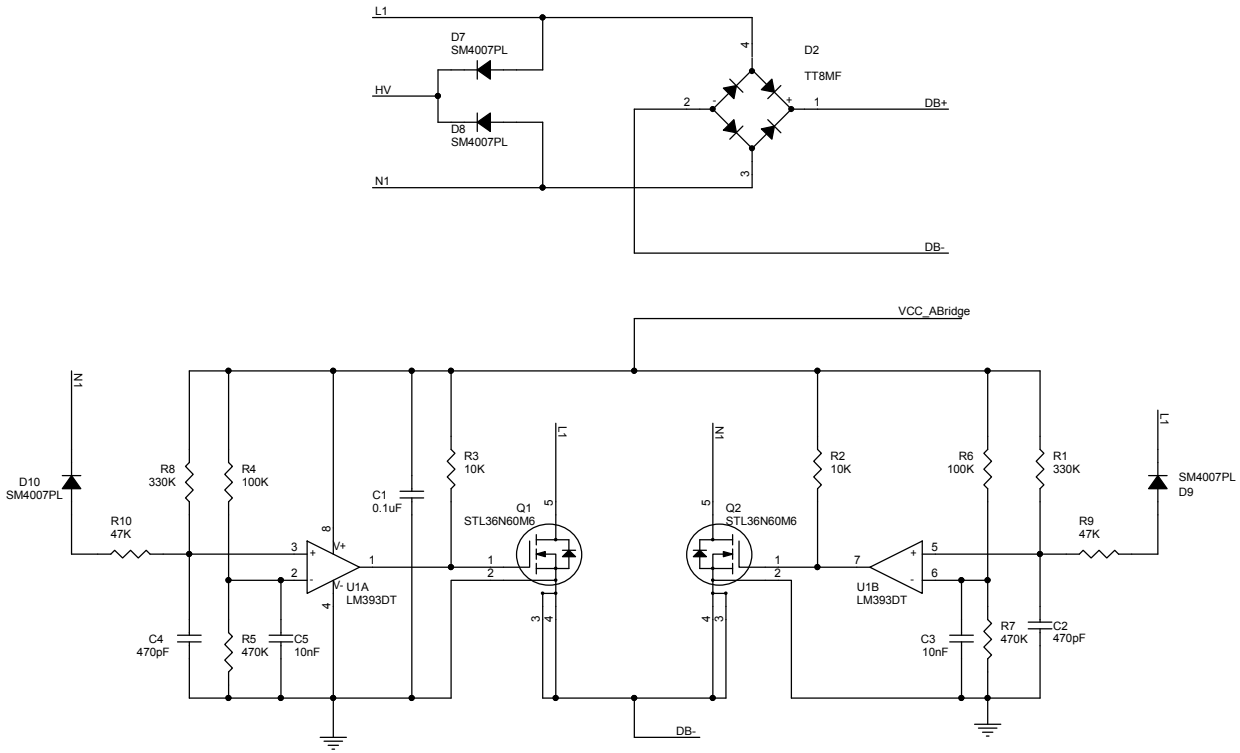


Figure 3. STDES-200GANADP circuit schematic (2 of 4)

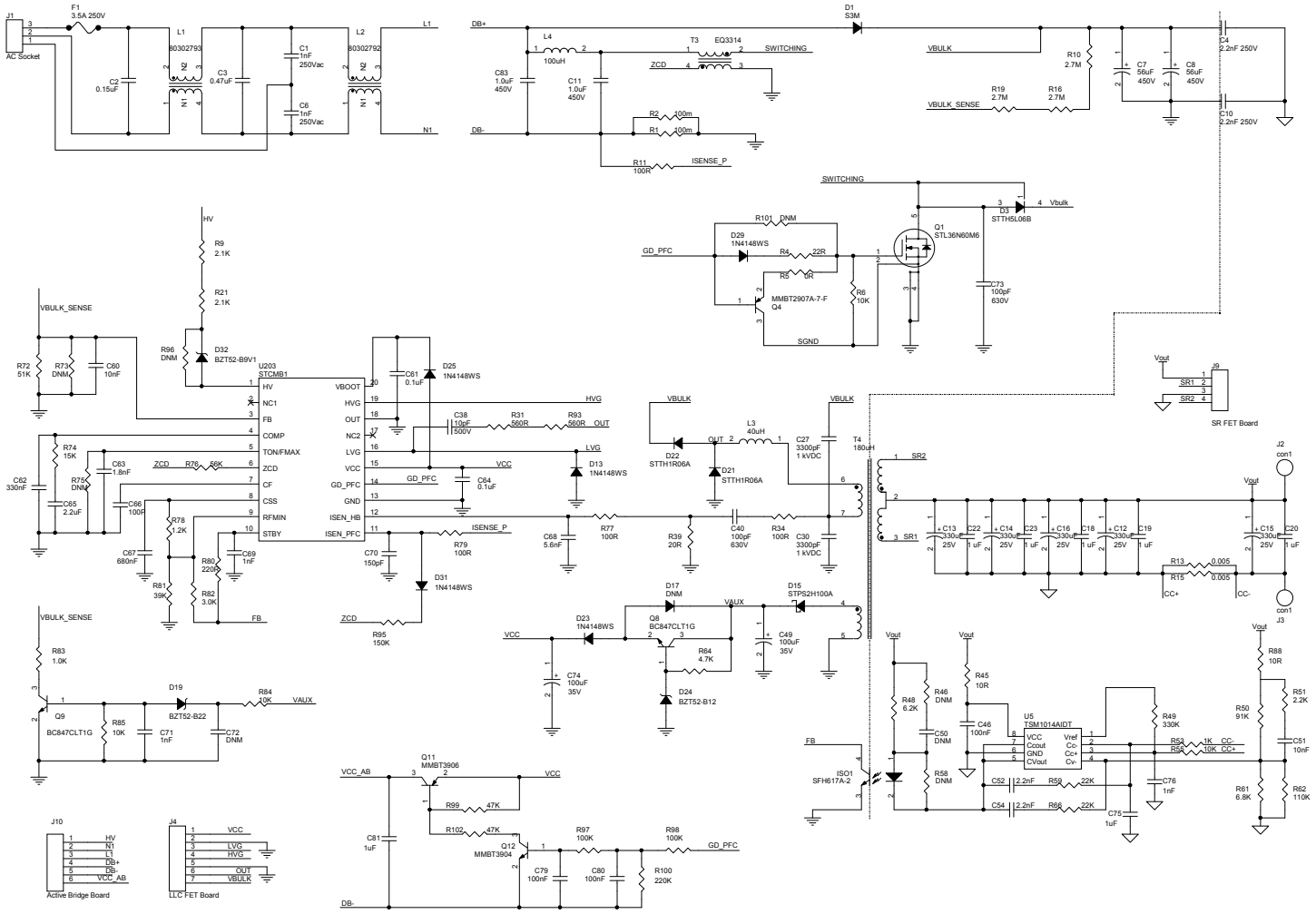


Figure 4. STDES-200GANADP circuit schematic (3 of 4)

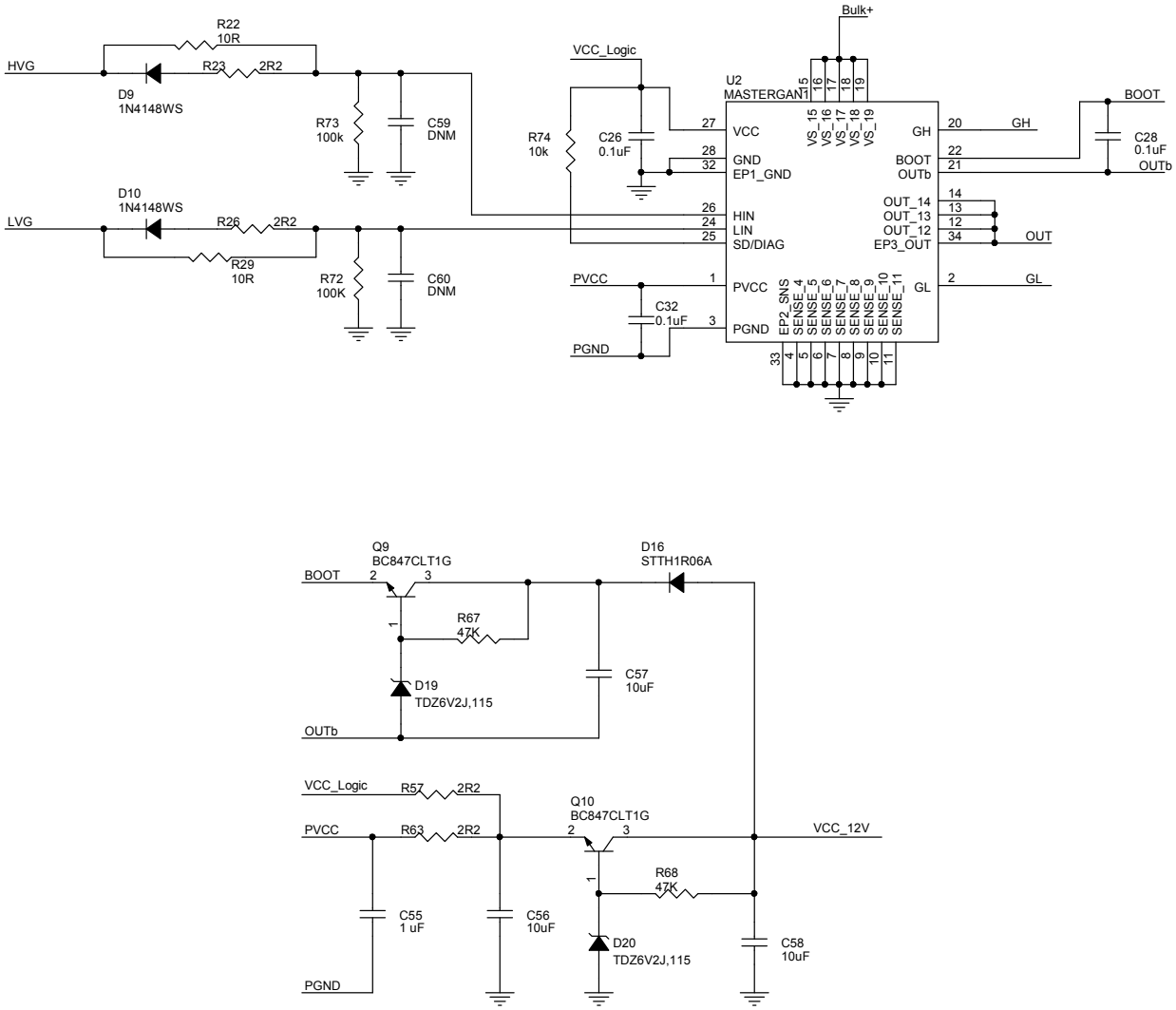
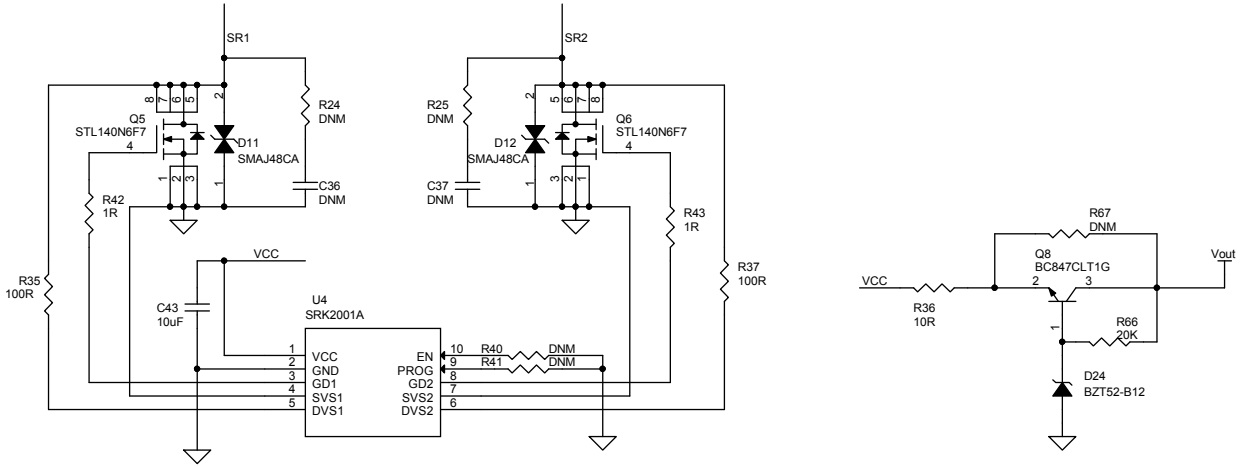


Figure 5. STDES-200GANADP circuit schematic (4 of 4)



Revision history

Table 2. Document revision history

Date	Revision	Changes
17-Nov-2022	1	Initial release.

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