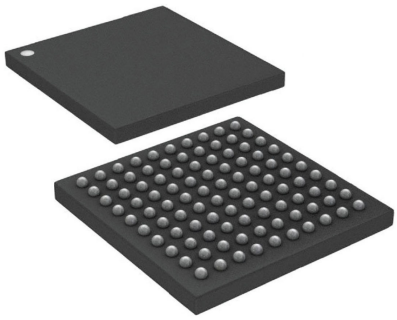
STA8610A

Data brief

TeseoVI automotive quad-band RTK/PPP precise positioning



LFBGA100 8.5 × 8.5 × 1.4 mm 0.8 mm ball pich

Product status link
STA8610A

Product summary		
Order code	**Packing**	**Secure**
STA8610A	Tray	No
STA8610AS1		Yes
STA8610ATR	Tape and reel	No
STA8610AS1TR		Yes

Features

Highlights

- *AEC*-Q100 automotive qualification on going
- *ESD*: 2 kV (*HBM*) and 500 V (*CDM*)
- Automotive grade 105°C

GNSS features

- STMicroelectronics' sixth generation positioning receiver with six constellations: *GPS*, *Galileo*, *GLONASS*, *BeiDou*, *QZSS*, *NAVIC* (former *IRNSS*)
- Open platform supported by a software development kit (*SDK*)
- Standard *PVT* positioning supporting up to quad-band for submeter accuracy applications
- Measurement engine with up to quad-band to support precise positioning algorithms
- Code phase, carrier phase, doppler frequency measurement
- Support any *SBAS* systems
- Independent *GPS*/*QZSS* L5, *Galileo* E5a/b, *BeiDou* B2a acquisition & tracking
- 192 (96 data & 96 pilot) signal tracking channels

Measurement engine core

- Arm® Cortex®-M7
- Embedded RAM/NVM/cache

Positioning engine core (*RTK*/*PPP*)

- Arm® Cortex®-M7
- Positioning engine core to support decimeter-level positioning firmware (RTK/PPP clients)
- Open platform (*SDK* offer) for precise positioning software partners
- Operating frequency up to 314 MHz
- Double precision floating-point unit
- Embedded cache (16 KB + 16 KB)
- Embedded 512 KB *RAM*

External octo-SPI memory interface

- Quad/octal flash/RAM controller
- HyperBus™ flash/RAM controller

Security

- Cybersecurity (ISO21434) support (STA8610AS1 only)
- Chip integrity (secure boot, secure firmware update, secure link) thanks to an embedded hardware security module (*HSM*), (STA8610AS1 only)
- Signal integrity (antijamming/antispoofing)
- Interface integrity (on-the-fly decryptor engine) (STA8610AS1 only)

Communication interfaces

- Three *UART* ports for host communication supporting hardware flow control
- Two synchronous serial ports (*SSP*) for host communication or STA5635A RFIC programming
- One I²C port for sensor interfacing

- One *SPIQ* port for sensor interfacing
- 2× *PPS* configurable outputs
- IQ interface to support dual antenna architecture (with external STA5635x)
- 2× timestamp inputs (PPS_IN)

Core peripherals

- Embedded *DMA*
- 32 kHz oscillator real-time clock
- Watchdog timer
- Nested vector interrupt controller
- JTAG

Power management unit

- Separate power supply domains:
  - Backup domain: 1.71 V to 3.63 V
  - Switchable domain: 1.71 V to 3.63 V
  - Optional external core supply voltage: 0.9 V to 1.0 V
- On-chip *LDO*s with high-voltage/low-voltage monitors

1 Introduction

1.1 Description

The STA8610A is a quad-band multiconstellation positioning receiver IC. It supports multiband constellations up to quad-band with a single die approach. It includes a dual-processor architecture that gives enough resources for supporting the *RTK*/*PPP* precision algorithms on chip.

Thanks to the software development kit (*SDK*), the STA8610A is an ideal open platform to be augmented with high-value sofware features such as *RTK*/*PPP*, and precise heading. The dual-antenna architecture is also supported thanks to the IQ interface to be connected with the external STA5635A RF IC. It is the ideal platform for supporting antispoofing and precise heading algorithms.

The STA8610AS1 also includes a hardware security module (*HSM*) to support secure boot. This module, with the signal and interface integrity mechanism, makes the STA8610A the ideal solution for applications where integrity is a key factor.

The STA8610A supports a highly evolved antijamming and antispoofing mechanism to mitigate attacks thanks to independent L5 acquisition and tracking, and to the *Galileo OSNMA* capability. The innovative RF architecture and *GNSS* baseband make it ready to support new emerging low Earth orbit (*LEO*) constellations. It is compliant with the ST automotive-grade qualification, which is included in addition to the AEC-Q100 requirements.

The usage of in-house manufacturing fabrication plants combined with a set of production flow methodologies targeting zero defect per million, makes the STA8610A the ideal solution for stringent automotive quality and supply chain requirements.

The device is delivered in a BGA package.

Note: For information on the Arm® core, refer to the Arm® Cortex®-M7 technical reference manual, available from the www.arm.com website.

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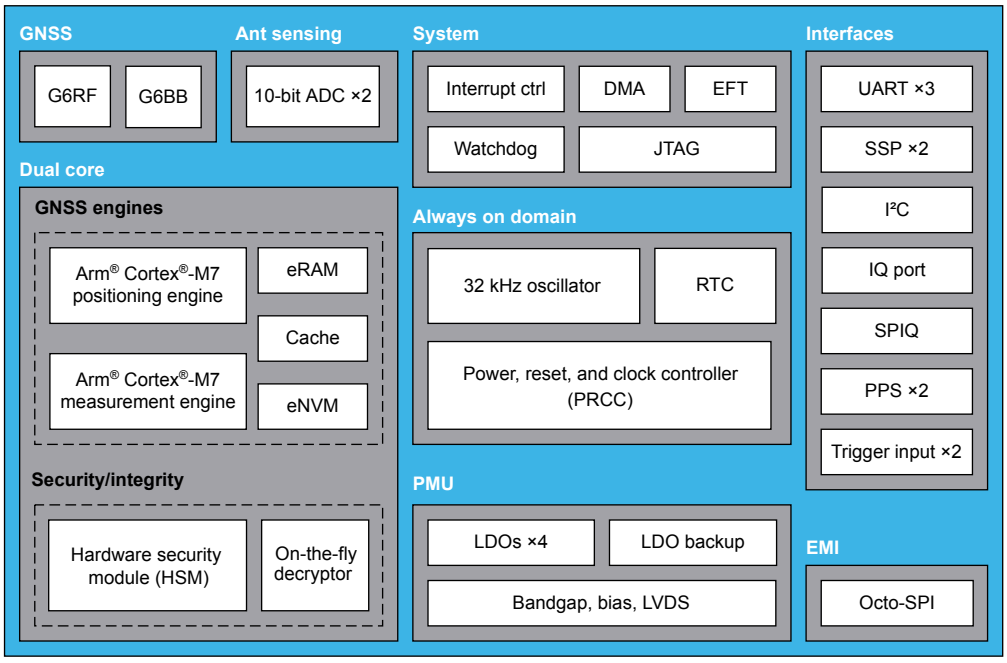
1.2 Block diagram

Figure 1. Block diagram



Revision history

Table 1. **Document revision history**

Date	Version	Changes
04-Feb-2025	1	Initial release.

Glossary

ADC Analog-to-digital converter

AEC Automotive Electronics Council. Also known as CDF-AEC for Chrysler-Delco-Ford Automotive Electronics Council. Shortened to AEC.

ASIL Automotive safety integrity level

It is a risk classification system defined by the ISO 26262 standard for the functional safety of road vehicles. There are four ASILs identified by ISO 26262—A, B, C, and D. ASIL A represents the lowest degree and ASIL D represents the highest degree of automotive hazard.

BeiDou Chinese navigation satellite-based radio navigation system

CBC Cipher block chaining

CDM Charged device model

DMA Direct memory access

DRAW Dead reckoning automotive way

DRUM Dead reckoning unplugged mode

ESD Electrostatic discharge

Galileo EU´s global navigation satellite system

GLONASS Russian satellite navigation system. Acronym for GLObalnaya NAvigatsionnaya Sputnikovaya Sistema (Russian). The role of the GLONASS satellite navigation system is similar to the GPS of the United States, the Galileo satellite positioning system of Europe, and the BeiDou satellite navigation system of China.

GNSS Global navigation satellite system

GPIO General-purpose input/output

GPS Global positioning system

HBM Human body model

HSM Hardware security module

HSSTP High-speed serial trace probe

IRNSS Indian regional navigation satellite system, with the operational name of Navigation with Indian constellation (NAVIC).

ISO International Organization for Standardization

I²C Inter-integrated circuit

JTAG Joint Test Action Group

LDO Low-dropout regulator

LEO Low Earth orbit

LVDS Low-voltage differential signaling

MIPS Microprocessor without interlocked pipeline stages

NAVIC Navigation with Indian constellation. The Indian regional navigation satellite system (IRNSS) is an autonomous regional satellite navigation system that provides accurate real-time positioning and timing services.

NVM Nonvolatile memory

OSNMA Open service navigation message authentication

P2P Peer-to-peer

PCB Printed-circuit board

PPP Precise point positioning

PPS Pulse per second

PVT Position-velocity-time

QFN Quad-flat no-leads

QZSS Quasi-zenith satellite system.

A Japanese satellite positioning system composed mainly of satellites in quasi-zenith orbits (QZO), but also of satellites in geostationary orbits (GEO).

RAM Random access memory

RTK Real-time kinematic

SBAS Satellite-based augmentation system. It provides services for improving the accuracy, integrity, and availability of basic GNSS signals.

SDK Software development kit

SPI Serial peripheral interface

SPIQ Queued serial peripheral interface

SSP Synchronous serial port

ST STMicroelectronics

UART Universal asynchronous receiver/transmitter