STA8089GA

Fully Integrated GPS/Galileo/Glonass/BeiDou/QZSS receiver

Data brief

VFQFPN56
(7x7x0.85mm)

Features

- STMicroelectronics® positioning receiver with 48 tracking channels and 2 fast acquisition channels supporting GPS, Galileo, Glonass, BeiDou and QZSS systems
- Pin to pin compatible with STA8088GA
- Single die standalone receiver embedding RF Front-End and low noise amplifier
- -162 dBm indoor sensitivity (tracking mode)
- Fast TTFF < 1 s in Hot start and 30 s in Cold Start
- High performance ARM946 MCU (up to 196 MHz)
- External SQI Flash interface
- 256 Kbyte embedded SRAM
- Real Time Clock (RTC) circuit
- 32-bit Watch-dog timer
- 2 UARTs
- 1 I^2C master/slave interface
- USB2.0 full speed (12 MHz) with integrated physical layer transceiver
- 2 Controller Area Network (CAN)
- 2 channels ADC (10 bits)
- Operating condition:
  - Main voltage regulator (V_{INL}): 1.8 V ± 5%
  - Backup voltage (V_{INB}): 1.6 V to 4.3 V
  - Digital voltage (V_{DD}): 1.0 V to 1.32 V
  - RF core voltage (V_{CC}): 1.2 V ± 10%
  - IO Ring Voltage (V_{ddIO}): 1.8 V ± 5% or 3.3 V ± 10%
- Package:
  - VFQFPN56 (7 x 7 x 0.85 mm) 0.4 mm pitch
- Ambient temperature range: -40/+85°C

Description

STA8089GA belongs to Teseo III family products.

STA8089GA is a single die standalone positioning receiver IC working on multiple constellations (GPS/Galileo/Glonass/BeiDou/QZSS).

STA8089GA is compliant with ST Automotive Grade qualification which includes in addition to AEC-Q100 requirements a set of production flow methodologies targeting zero defect per million.

STA8089GA, fulfilling high quality and service level requirements of the Automotive market, is the ideal solution for in-dash navigation and OEM telematics applications.

The device is offered with a complete GNSS firmware which performs all GNSS operations including tracking, acquisition, navigation and data output.

STA8089GA can run also TESEO-DRAW the STMicroelectronics dead reckoning firmware.

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1 Overview

STA8089GA is one of the part number of Teseo III STA8089x series.

STA8089GA is a highly integrated single-chip standalone GNSS receiver designed for positioning system applications.

STA8089GA embeds the new ST GNSS positioning engine capable of receiving signals from multiple satellite navigation systems, including the US GPS, European Galileo, Russia's GLONASS, Chinese BeiDou and Japan's QZSS.

The STA8089GA ability of tracking simultaneously the signals from multiple satellites regardless of their constellation, make this chip capable of delivering exceptional accuracy in urban canyons and in the environments where buildings and other obstructions make satellite visibility challenging.

The STA8089GA is backward compatible with STA8088GA, enabling fast customer application migration.

The STA8089GA combines a high performance ARM946 microprocessor with I/O capabilities and enhanced peripherals. It supports USB2.0 standard at full speed (12 Mbps) with on-chip PHY.

The chip embeds backup logic with real time clock.

The device is offered with a complete firmware performing all positioning operations including acquisition, tracking, navigation and data output.

STA8089GA can be offered also bundled with STMicroelectronis dead reckoning firmware called TESEO-DRAW; TESEO-DRAW firmware is a multi-sensors data fusion hub for Teseo family IC's.

The device powered with 1.8 V enables the on-chip voltage regulators to internally supply the RF front-end, core logic and the backup logic. The device can be directly powered with 1.2 V bypassing the embedded voltage regulators which will be put in power down mode.

I/O lines are compatible with 1.8 V and 3.3 V.

STA8089GA is compliant with ST Automotive Grade qualification which includes in addition to AEC-Q100 requirements a set of production flow methodologies targeting zero defect per million.

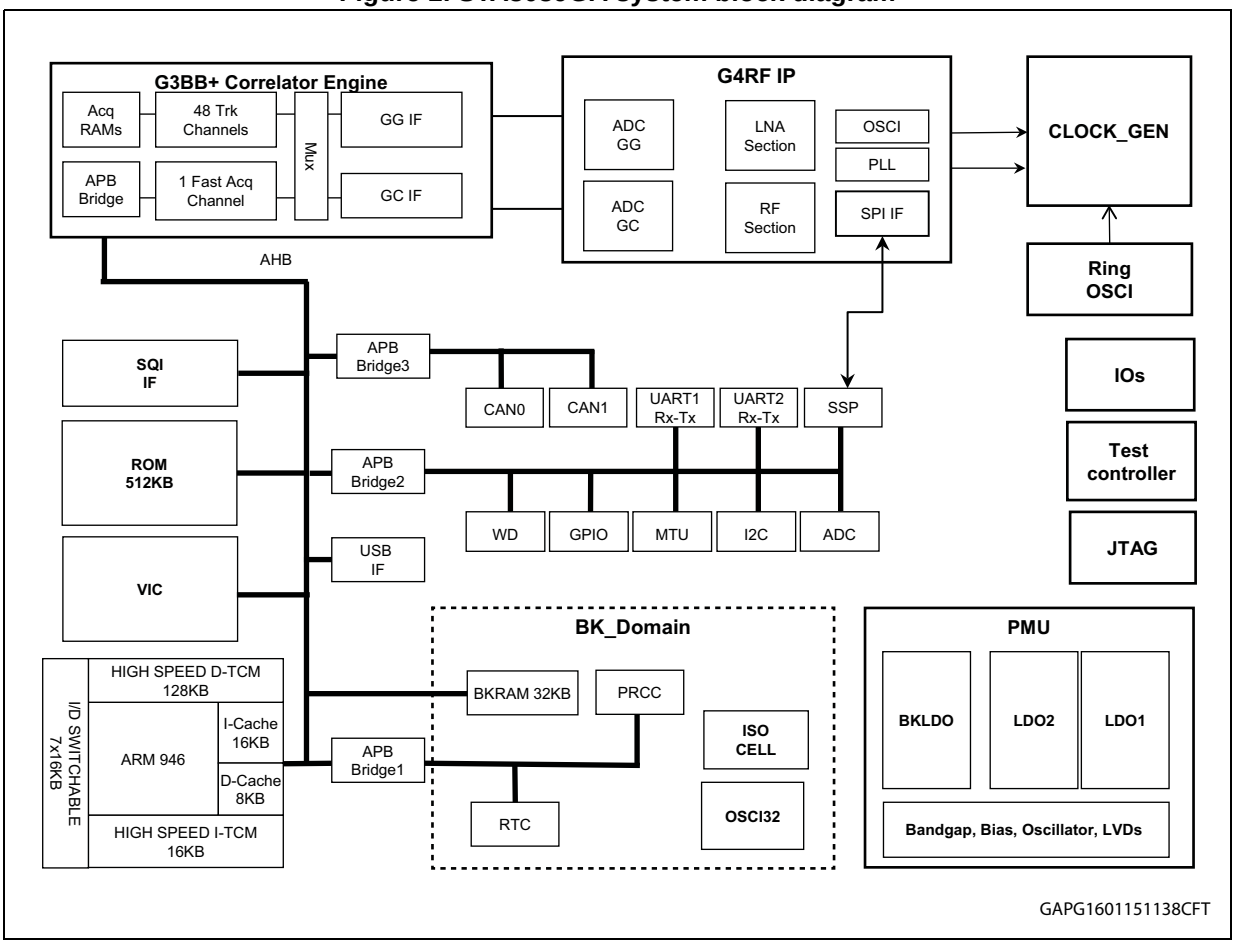
STA8089GA, fulfilling high quality and service level requirements of the Automotive market, is the ideal solution for in-dash navigation and OEM telematics applications.

The STA8089GA, using STMicroelectronics CMOSRF Technology, is housed in a VFQFPN56 (7 x 7 x 0.85 mm) package.

2 Pin description

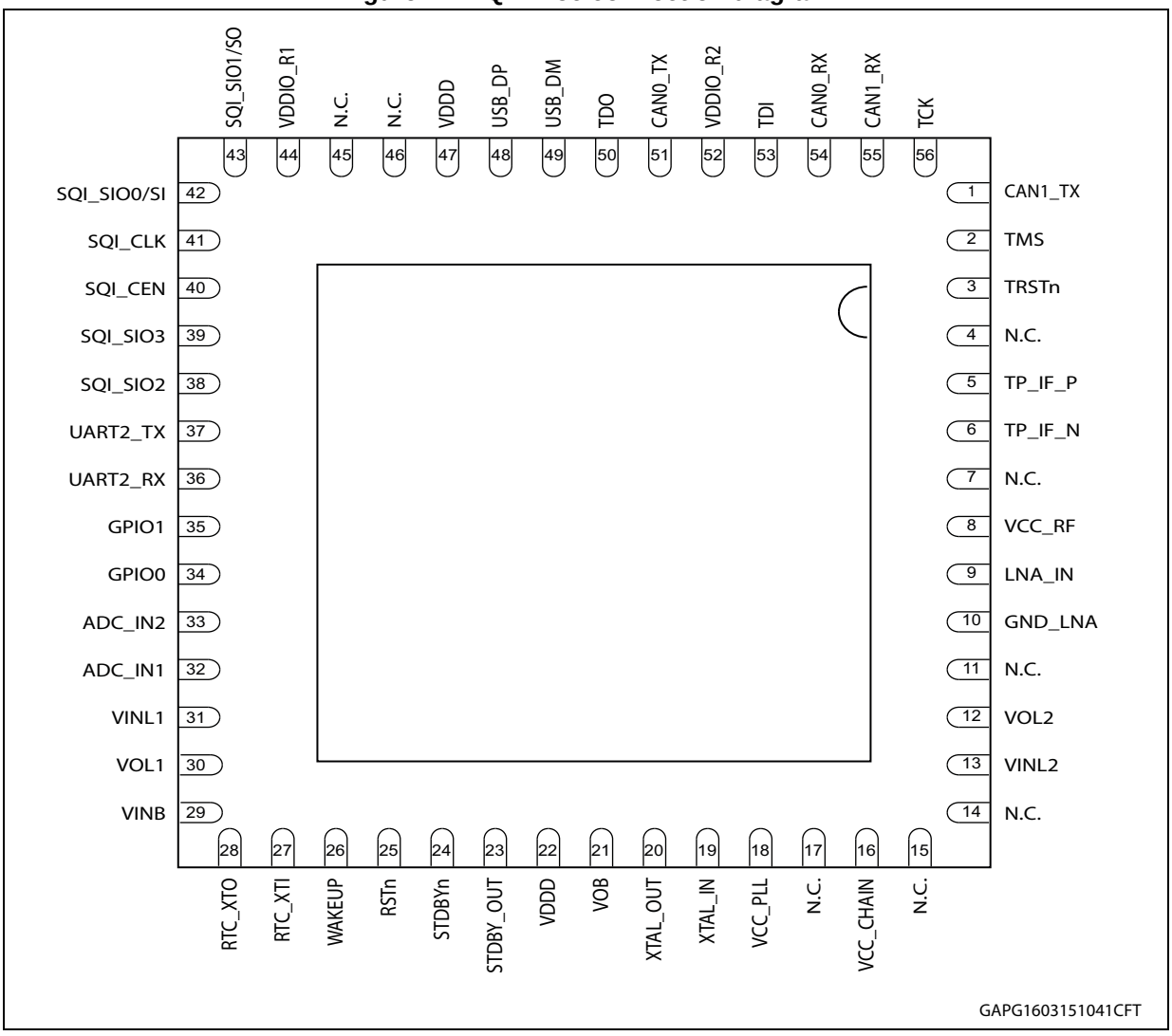
2.1 Block diagram

Figure 1. STA8089GA system block diagram



2.2 VFQFPN56 pin configuration

Figure 2. VFQFPN56 connection diagram



2.3 Power supply pins

Table 1. Power supply pins

Symbol	I/O voltage	I/O	Description	STA8089GA
VCC_CHAIN	1.2 V	PWR	Analog supply voltage for RF chain (1.2 V)	16
VCC_PLL	1.2 V	PWR	Analog supply voltage for PLL RF (1.2 V)	18
VCC_RF	1.2 V	PWR	Analog supply voltage for RF (1.2 V)	8
VDDD	1.1 V	PWR	Digital supply voltage. This value can be configured to 1.0 V, 1.1 V (default) or 1.2 V	22, 47
VDDIO_R1	1.8 V or 3.3 V	PWR	Digital supply voltage for I/O ring 1 (1.8 V or 3.3V)	44

Table 1. Power supply pins (continued)

Symbol	I/O voltage	I/O	Description	STA8089GA
VDDIO_R2	3.3 V	PWR	Digital supply voltage for I/O ring 2 (3.3 V)	52
VINB	1.6 V - 4.3 V	PWR	Backup LDO input supply voltage (1.6 V to 4.3 V)	29
VINL1	1.8 V	PWR	LDO1 and ADC input supply voltage	31
VINL2	1.6 V - 4.3 V	PWR	LDO2 input supply voltage (1.6 V to 4.3 V)	13
VOB	1.0 V	PWR	LDO backup output voltage (1.0 V)	21
VOL1	1.1 V	PWR	LDO1 output voltage (1.1 V; it can be also configured to 1.0 V or 1.2 V)	30
VOL2	1.2 V	PWR	LDO2 output voltage (1.2 V)	12
GND	GND	GND	Ground	EP
GND_LNA	GND	GND	Ground	10

2.4 Main function pins

Table 2. Main function pins

Symbol	I/O voltage	I/O	Description	STA8089GA
ADC_IN1	1.4 V – 0 V typ range	I	ADC Analog input [1]	32
ADC_IN2	1.4 V – 0 V typ range	I	ADC Analog input [2]	33
RSTn	1.0 V	I	Reset Input with Schmitt-Trigger characteristics and noise filter.	25
RTC_XTI	1.0 V (max)	I	Input of the 32 KHz oscillator amplifier circuit and input of the internal real time clock circuit.	27
RTC_XTO	1.0 V (max)	O	Output of the oscillator amplifier circuit.	28
STDBY_OUT	1.0 V	O	When low, indicates the chip is in Standby mode	23
STDBYn	1.0 V	I	When low, the chip is forced in Standby Mode - All pins in high impedance except the ones powered by Backup supply	24
WAKEUP	1.0 V	I	WAKEUP from STANDBY mode	26

2.5 Test/emulated dedicated pins

Table 3. Test/emulated dedicated pins

Symbol	I/O voltage	I/O	Description	STA8089GA
TCK	VDDIO_R2	I	JTAG Test Clock	56
TDI	VDDIO_R2	I	JTAG Test Data In	53
TDO	VDDIO_R2	O	JTAG Test Data Out	50
TMS	VDDIO_R2	I	JTAG Test Mode Select	2

Table 3. Test/emulated dedicated pins (continued)

Symbol	I/O voltage	I/O	Description	STA8089GA
TRSTn	1.0 V	I	JTAG Test Circuit Reset	3
TP_IF_N	1.2 V	O	Diff.Test Point for IF – Neg.	6
TP_IF_P	1.2 V	O	Diff.Test Point for IF – Pos.	5

2.6 Communication interface pins

Table 4. Communication interface pins

Symbol	I/O voltage	I/O	Alternative function	Function	Description	STA8089GA
SQI_CLK	VDDIO_R1	O	AF2 (default)	SQI_CLK	SQI Flash clock	41
		—	AF0, AF1, AF3	Reserved	Reserved	
SQI_CEN	VDDIO_R1	O	AF2 (default)	SQI_CEN	SQI Flash chip enable	40
		—	AF0, AF1, AF3	Reserved	Reserved	
SQI_SIO0/SI	VDDIO_R1	I/O	AF2 (default)	SQI_SIO0/SI	SQI Flash data IO 0 / ser. I/ BOOT2	42
		—	AF0, AF1, AF3	Reserved	Reserved	
SQI_SIO1/SO	VDDIO_R1	I/O	AF2 (default)	SQI_SIO1/SO	SQI Flash data IO 1 / ser. O	43
		—	AF0, AF1, AF3	Reserved	Reserved	
SQI_SIO2	VDDIO_R1	I/O	AF2 (default)	SQI_SIO2	SQI Flash data IO 2	38
		—	AF0, AF1, AF3	Reserved	Reserved	
SQI_SIO3	VDDIO_R1	I/O	AF2 (default)	SQI_SIO3	SQI Flash data IO 3 / BOOT1	39
		—	AF0, AF1, AF3	Reserved	Reserved	
CAN1_TX(1)	VDDIO_R2	O	AF0	I2C_CLK	I2C clock	1
		I/O	AF1	GPIO8	General purpose I/O #8	
		O	AF2 (default)	CAN1_TX(1)	CAN1 transmit data output	
		—	AF3	Reserved	Reserved	
CAN1_RX(1)	VDDIO_R2	I/O	AF0	I2C_SD	I2C serial data	55
		I/O	AF1	GPIO9	General purpose I/O #9	
		I/O	AF2 (default)	CAN1_RX	CAN1 receive data input	
		—	AF3	Reserved	Reserved	
CAN0_TX(1)	VDDIO_R2	O	AF0 (default)	CAN0_TX(1)	CAN0 transmit data output	51
		O	AF1	UART0_TX	UART0 Tx data	
		I/O	AF2	GPIO7	General purpose I/O #7	
		O	AF3	I2C_CLK	I2C clock	

Table 4. Communication interface pins (continued)

Symbol	I/O voltage	I/O	Alternative function	Function	Description	STA8089GA
CAN0_RX(1)	VDDIO_R2	I	AF0 (default)	CAN0_RX(1)	CAN0 receive data input	54
		I	AF1	UART0_RX	UART0 receive data input	
		I/O	AF2	T_{SENSE}	External temperature capture port	
		I/O	AF3	I2C_SD	I2C serial data	
UART2_RX	VDDIO_R1	I	AF0 (default)	UART2_RX	UART2 Rx data	36
		I/O	AF1	GPIO28	General purpose I/O #28	
		I/O	AF2	I2C_SD	I2C serial data	
		—	AF3	Reserved	Reserved	
UART2_TX	VDDIO_R1	O	AF0 (default)	UART2_TX	UART2 Tx data / BOOT0	37
		I/O	AF1	GPIO29	General purpose I/O #29	
		O	AF2	I2C_CLK	I2C clock	
		—	AF3	Reserved	Reserved	
GPIO0	VDDIO_R1	I/O	AF0 (default)	GPIO0	General purpose I/O #0	34
		I	AF1	PPS_IN	Pulse per second input	
		O	AF2	Timer_OCMPB	Extended Function Timer - Output Compare B	
		O	AF3	Mag_0 GC	Glonass and BeiDou 3-bit coding Output (MAG0)	
GPIO1	VDDIO_R1	I/O	AF0 (default)	GPIO1	General purpose I/O #1 / BOOT3	35
		—	AF1	Reserved	Reserved	
		O	AF2	PPS_OUT	Pulse per second output	
		I/O	AF3	Tsense	External temperature capture port	
USB_DM	VDDIO_R2	USB	AF0	USB_DM	USB D- signal	49
		I	AF1 (default)	UART1_RX	UART1 Rx data	
		I	AF2	CAN1_RX(1)	CAN1 receive data input	
		I/O	AF3	I2C_SD	I2C serial data	
USB_DP	VDDIO_R2	USB	AF0	USB_DP	USB D+ signal	48
		O	AF1 (default)	UART1_TX	UART1 Tx data	
		O	AF2	CAN1_TX(1)	CAN1 transmit data output	
		O	AF3	I2C_CLK	I2C clock	

1. Only for STA8089GA.

2.7 RF front-end pins

Table 5. RF front-end pins

Symbol	I/O voltage	I/O	Description	STA8089GA
LNA_IN	1.2V	I	Low Noise Amplifier Input	9
XTAL_IN	1.2V	I	Input Side of Crystal Oscillator or TCXO Input	19
XTAL_OUT	1.2V	O	Output Side of Crystal Oscillator	20

3 Package and packing information

3.1 ECOPACK® packages

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com.

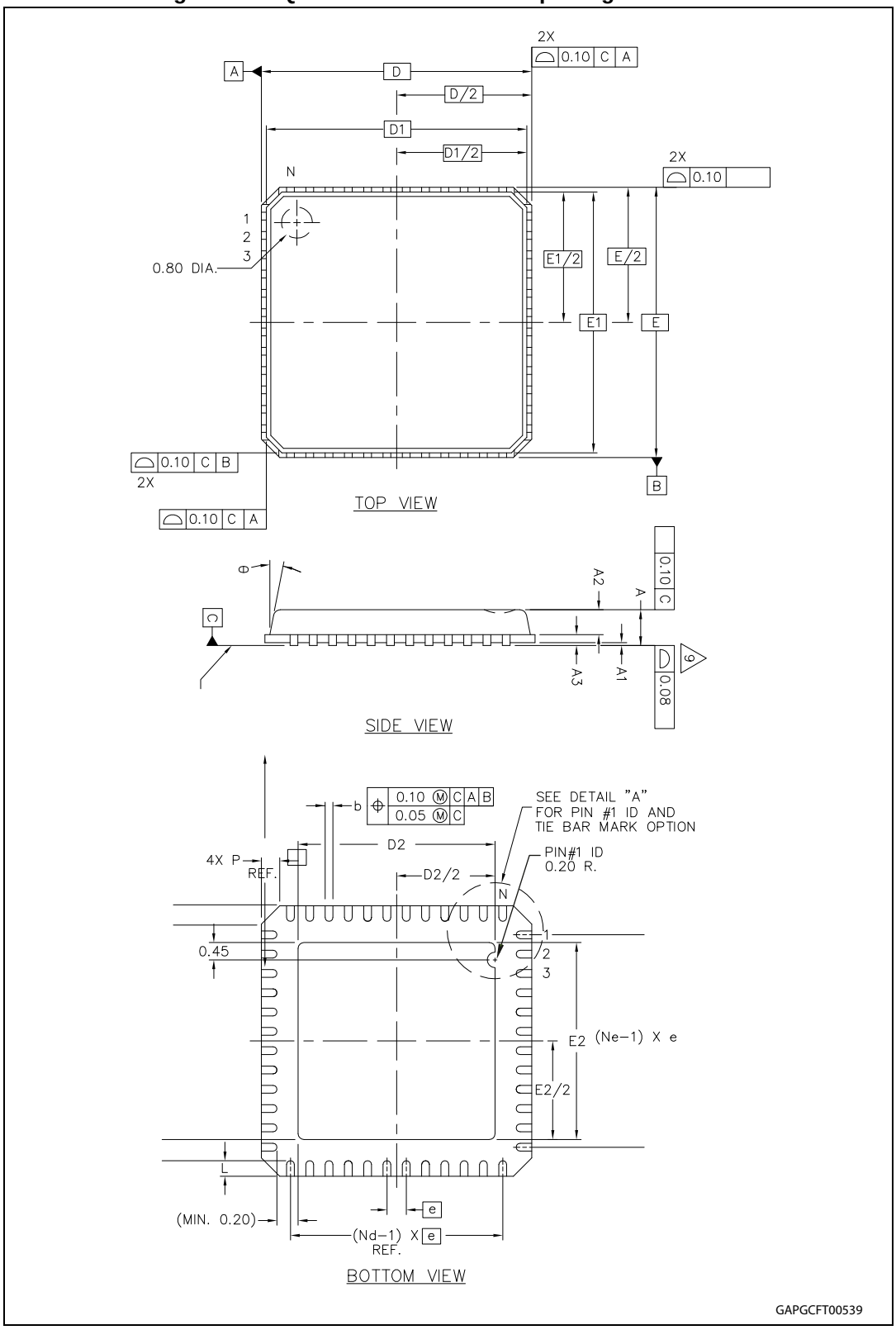
ECOPACK® is an ST trademark.

3.2 VFQFPN56 7 x 7 x 0.85 mm package information

Table 6. VFQFPN56 7 x 7 x 0.85 mm package dimensions

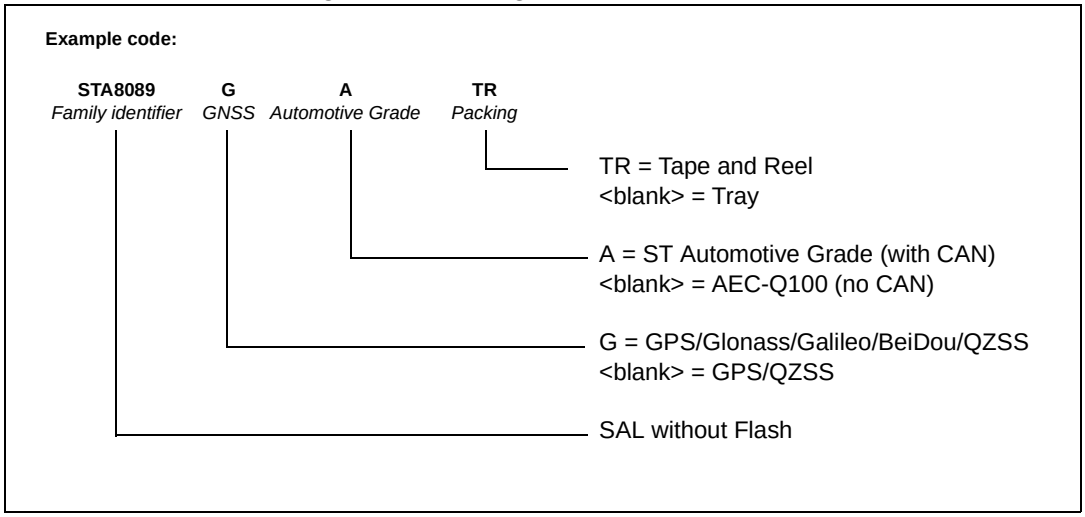
Symbol	Min.	Typ.	Max
Common dimensions			
A	0.80	0.85	0.90
A1	0	0.01	0.05
A2	0.60	0.65	0.70
A3		0.20 REF	
b	0.15	0.20	0.25
D		7.00 BSC	
D1		6.75 BSC	
D2	5.0	5.1	5.2
E		7.00 BSC	
E1		6.75 BSC	
E2	5.0	5.1	5.2
e		0.40 BSC	
θ	0°		12°
L	0.30	0.40	0.50
N		56	
Nd		14	
Ne		14	
P	0.24	0.42	0.60

Figure 3. VFQFPN56 7 x 7 x 0.85 mm package dimension



4 Ordering information

Figure 4. Ordering information scheme



5 Revision history

Table 7. Document revision history

Date	Revision	Changes
25-Mar-2015	1	Initial release.