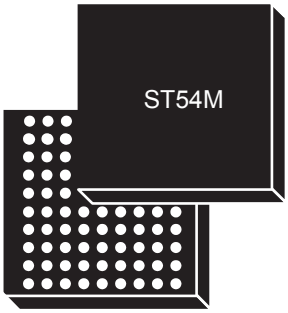
ST54M

Data brief

NFC controller and secure element system-on-chip



90 ball WLCSP

STSECURE

Product status link
ST54M

Features

- Single die integrating an NFC controller (contactless front-end - CLF) and a secure element (SE)
- Small package WLCSP90, ECOPACK-compliant

NFC controller

- Arm® Cortex®-M3 microcontroller
- 100% re-flashing capability for firmware update
- Enhanced active load modulation technology
- Step-up DC/DC for Tx drive up to 3 W
- Optimized for extremely small or metal frame antennas
- Optimized low-power consumption modes
- Selectable ultralow power hibernate state
- Battery voltage monitoring
- Proprietary in-frame synchronization (IFS) in card emulation (CE) to ensure stability in battery low and switched off modes
- System clock
  - Fractional-N PLL input range of 19.2 to 76.8 MHz
  - External crystal oscillator (27.12 MHz and 54.24 MHz)
- 32.768 kHz, 16 MHz and 32 MHz support for EMC tests
- Automatic wake-up via communication interfaces, GPIO, RF field or tag detection and power supply detection

RF communications

- Reader/writer mode
  - NFC Forum™ Type 1/2/3/4/5 tags
  - FeliCa™
  - ISO/IEC 15693
  - MIFARE®(MIFARE R/W mode feature availability is pending on license conditions. Contact your local ST representative for further information.)
- Card emulation mode
  - ISO/IEC 14443 Type A & B
  - FeliCa™
  - MIFARE®
  - Intelligent card switch
- Peer-to-peer mode
  - ISO/IEC 18092 - NFCIP-1 initiator and target

Communication interfaces

- CLF interfaces:
  - 1 I3C/I2C target interface: I3C up to 12.9 MHz, I2C supporting Standard, Fast, and Fast+ modes
  - 2 SWP master interfaces up to 1.695 Mbit/s
  - GPIOs
  - 1 UICC Class B and C power supply
- SE interfaces:
  - 2 I3C/I2C target interfaces: I3C up to 12.9 MHz, I2C supporting Standard, Fast, and Fast+ modes
  - 2 SPI target interfaces up to 26 MHz
  - 1 Class C ISO/IEC 7816-3 interface up to 20MHz (Class D ready)
  - GPIOs

Secure microcontroller

- Arm® Cortex® M35P 32-bit RISC core
- 4.5 Mbytes of flash memory
- 16-Kbyte memory cache
- 150 Kbytes of user RAM
- Selectable ultralow power hibernate and standby states
- Supports state-of-the-art secure element operating systems
- CC EAL5+/EAL6+ certification
- Hardware security-enhanced DES and AES
- KECCAK hardware accelerator for NTT ML-KEM & ML-DSA PQC algorithms
- MIFARE Classic® cryptography hardware accelerator
- NESCRYPT coprocessor for public key cryptography algorithm
- Supports embedded-SIM (eSIM) applications in compliance with the GSMA specification
- Secure ranging support in connection with an external UWB subsystem

Electrical characteristics

- Battery voltage support from 2.1 V to 5.1 V
- I/O dedicated voltage level (V_{PS_IO}): 1.2 V and 1.8 V compatibility
- Ambient operating temperature -30°C to + 85°C

Application

- Mobile devices
- Wearable devices
- Smartwatches
- Secure connected devices

1 Description

The ST54M is a single-die solution integrating a contactless front-end (ST54M_CLF) and a secure element (ST54M_SE). It is designed for integration in mobile devices and NFC-compliant products.

1.1 ST54M_CLF

The ST54M_CLF includes near-field communication (NFC) functions in the three operating modes: card emulation, reader/writer, and peer-to-peer communication. It is based on an advanced Arm® Cortex®-M3 32-bit microcontroller. The ST54M_CLF is designed to increase RF communication distances, ease NFC technology integration, and operate in efficient low power modes.

The ST54M_CLF is best in class in terms of RF output power, working up to 3 W thanks to an internal step-up DCDC converter. Maximum power can be safely used to communicate thanks to a dynamic control: when a card is close, power is automatically reduced to ensure interoperability and standard compliance. To go with this outstanding output power, demodulation sensitivity is optimized to maximize the communication distance with all types of cards.

The ST54M_CLF card emulation mode does not require any external oscillator nor reference clock source. Thanks to active load modulation and automatic adjustments based on field strength, communication distance is maximized, and interoperability is ensured.

The ST54M_CLF can operate in very low power modes, while detecting the presence of a reader, a card, or a tag beyond its rated communication distance. An improved field detection sensitivity and a stable and efficient low power card detection mechanism make this operation possible.

The ST54M_CLF exchanges data with the device application processor over the NCI 2.1 logical interface on top of the I3C/I2C connection. It features two external SWP master interfaces and one internal SWP master interface to control the embedded SE (ST54M_SE). Thanks to an enhanced power switch system, the ST54M_CLF manages its own power supply and that of the associated secure elements, including ST54M_SE and one UICC.

1.2 ST54M_SE

The ST54M_SE is a serial access microcontroller designed for secure mobile applications. It incorporates the most recent generation of Arm® processors for embedded secure systems. Their SecurCore® Cortex®-M35P 32-bit RISC core is built on the Cortex®-M33 core with additional security features to help protect against advanced forms of attack.

The ST54M_SE provides high-performance thanks to a fast Cortex®-M35P processor, crypto-accelerators, and improved flash memory operation. The Cortex®-M35P core and its cache memory bring great performance and excellent code density thanks to the Thumb®-2 instruction set.

Strong and multiple fault protection mechanisms ensure a guaranteed high-detection coverage that facilitates the development of highly secure software. This is achieved by using two CPUs in locked-step mode, error codes in sensitive memories and hardware logic.

The ST54M_SE features hardware accelerators for advanced cryptographic functions:

- The EDES peripheral provides a secure DES (Data encryption standard) algorithm implementation, while the NESCRYPT FAST cryptographic processor efficiently supports the public key algorithm.
- The AES peripheral ensures secure and fast AES algorithm implementation.
- The KECCAK peripheral supports NTT ML-KEM & ML-DSA PQC algorithms.

A comprehensive set of power-saving modes enables the design of efficient low-power applications.

The ST54M_SE platform offers a serial communication interface that is fully compatible with the ISO/IEC 7816-3 standard (T=0, T=1) up to 20MHz, and is intended for use in embedded SIM (eSIM) applications.

It includes a single-wire protocol (SWP) interface that internally connects to the ST54M_CLF.

Multiple ST54M_SE interfaces provide flexible connection to subsystems such as UWB companion device to manage CCC Digital Key Release 3.0 compliant and FiRa compliant secure ranging.

The MIFARE® RW mode feature availability depends on the license conditions. Contact your local ST representative for further information.

1.3 ST54M package

The ST54M is manufactured in an ECOPACK-compliant, 3.634 × 3.799 mm, 90-ball wafer-level chip-scale package (WLCSP). To meet integration needs, the WLCSP is available in two thicknesses, 0.33 mm and 0.55 mm. The WLCSP offers a more compact footprint, while minimizing die-to-PCB inductance and improving thermal performance.

In order to meet environmental requirements, ST offers the ST54M devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

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Revision history

Table 1. **Document revision history**

Date	Revision	Changes
01-Jun-2026	3	First public release.

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