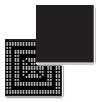
Stellar SR6 G7 line—32-bit Arm® Cortex®-R52+ automotive integration MCU 6× Cortex®-R52+ cores, 20.5 MB NVM (2× 19.5 MB “OTA X2”) 9.1 MB RAM, with embedded virtualization, safety, and security

FPBGA476

(21.3 × 21.3 mm)



FPBGA292

(17 × 17 mm)

Product status link	
Part number	**Package**
SR6G7C6	FPBGA476
SR6G7C4	FPBGA292

Features

- AEC-Q100
- SR6 integration *MCU*s:
  - Have superior real-time and safe performance (with highest *ASIL*-D capability)
  - Bring hardware-based virtualization technology to *MCU*s for simplified multiple software integrations at optimized performance
  - Have built-in fast and cost-effective *OTA* reprogramming capability (with built-in dual-image storage)
  - Offer high-speed security cryptographic services, for example for network authentication

Cores

- 6 × 32-bit Cortex®-R52+ cores (4 of them with checker cores, and 2 in split-lock configuration):
  - Configurable as either 6 cores (4 of them in lockstep configuration) or 5 cores (all of them in lockstep configuration)
  - Arm® v8-R compliant
  - Single precision floating-point unit (*FPU*)
  - New privilege level for real-time virtualization
  - 2 cores with Neon™ extensions (for example *SIMD*, dual precision FPU)
- 2 Cortex®-M4 multipurpose accelerators, both in lockstep configuration
- 4 *eDMA* engines in lockstep configuration

Memories

- Up to 20.5 MB on-chip nonvolatile memory (NVM):
  - PCM (phase-change memory) as nonvolatile memory
  - 19.5 MB code NVM, with embedded memory replication for OTA (over-the-air) reprogramming with up to 2× 19.5 MB
  - 1024 KB HSM-dedicated code NVM
- 640 KB data NVM (512 KB + 128 KB dedicated to HSM)
- Up to 9280 KB on-chip general-purpose SRAM

Security: 2nd generation hardware security module

- Cybersecurity: ISO/SAE 21434 compliance (refer to the cybersecurity reference manual for details)
- On-chip high-performance security module with full support for e-safety vehicle intrusion protected applications (EVITA)
- Symmetric and asymmetric cryptography processor
- High-performance lock-stepped AES-light security subsystem for fast ASIL-D cryptographic services

Safety: comprehensive new-generation ASIL-D safety concept

- New state-of-the-art safety measures at all levels of the architecture for most efficient implementation of ISO 26262 ASIL-D functionalities
- Complete hardware virtualization architecture built on Cortex®-R52+ new privilege mode (best-in-class software isolation, real-time support for multiple virtual machines/applications)

Device standby/low-power modes

- Versatile low-power modes
- Ultra-low power: standby mode for lowest quiescent current with optimized active subsystem (for example standby RAM) and wake-up capability
- Smart low-power: smart power mode with Cortex®-M4 subsystem, extended communications interfaces, and ADC peripheral

Peripheral, I/O, and communication interfaces

- 28 LINFlexD modules
- 2 dual-channel FlexRay controllers
- 10 queued serial peripheral interface (SPIQ) modules
- 2 DSPI with shifted PWM serialization support for lighting applications
- 2 I²C interfaces
- 2 SENT modules (15 channels each)
- 2 PSI5 modules (2 channels each)
- Enhanced analog-to-digital converter system with:
  - 8 separate 12-bit SAR analog converters (including one supervisor/safety ADC).
  - One 9-bit SAR analog converter for device standby/low-power mode
  - Interconnection with GTM timer for autonomous ADC/GTM subsystem operation
- Advanced timed I/O capability:
  - Generic timer module (GTM4154)
- Communication interfaces:
  - Two 10/100/1000 Mbit/s Ethernet controllers compliant with IEEE 802.3-2008: IPv4 and IPv6 checksum modules, AVB, VLAN, and EMC optimized SGMII
  - 19 modular controller area network (MCAN) modules, and 1 time-triggered controller area network (M_TTCAN), all supporting flexible data rate (ISO CAN FD®)

External memory interfaces

- 2 octo-SPI IPs to support HyperBus™ memory (flash/RAM) devices
- 1 SDMMC interface

1 Introduction

1.1 Document overview

This document provides a summary of the target specification and features of the SR6G7C6, SR6G7C4 devices. For detailed information, refer to the device Datasheet and device Reference manual.

Note: For information on the Cortex®-R52+ and Cortex®-M4 cores, refer to the technical reference manuals, available from the www.arm.com website.

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1.2 Description

Stellar integration MCUs have been designed to meet the requirements of domain controllers and ECUs with high integration requested in the architectures of connected updatable automated and electrified cars. They have superior real-time and safe performance (with highest ASIL-D capability). Bringing hardware-based virtualization technology to MCUs, they ease the development and integration of multiple source software onto the same hardware while maximizing the resulting software performance. They offer high-efficiency OTA reprogramming capability with fast new image download and activation at almost no memory overhead thanks to SR6 unique built-in dual-image storage tailored to OTA reprogramming needs. They also provide high-speed security cryptographic services, for instance for network authentication.

Table 1. SR6G7C6, SR6G7C4 overview

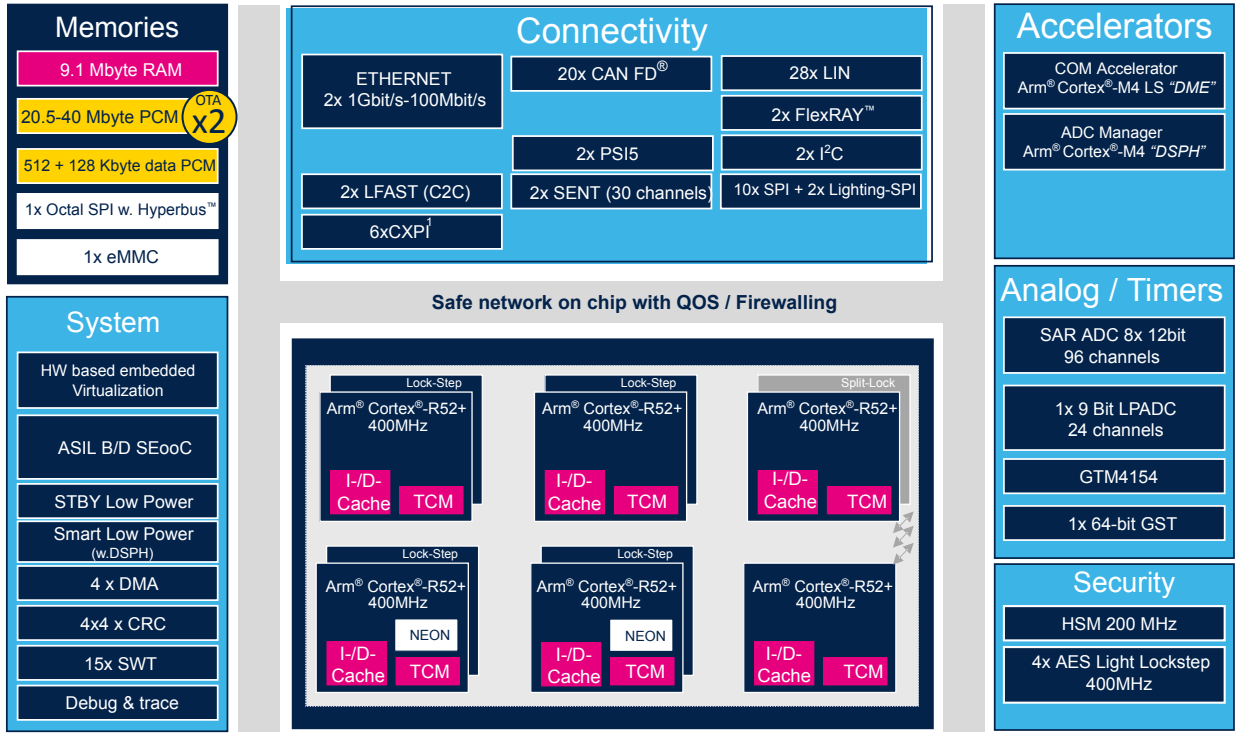
Feature		SR6G7C6, SR6G7C4
Cortex®-R52+ cores (+ checker cores)		6 cores (+4 checkers), configurable as 5 cores (+5 checkers)
Neon™ (with SIMD, dual precision floating point)		2
Cache (instruction/data) per core in Kbyte		32/32
Core memory protection unit (regions), several additional protection mechanisms in the architecture, for example: NOC firewalls	Hypervisor (EL2)	24
	OS (EL1)	24
Code NVM	Overall including HSM in Mbytes	20.5
	Cluster code NVM in Mbytes	19.5
	HSM code NVM in Kbytes	1024
Code NVM built-in memory replication for OTA reprogramming (not supported by HSM) in Mbytes		Up to 2× 19.5
Data NVM in Kbytes		640
RAM in Kbytes		9280
Hardware security module (HSM) - 2nd generation		Yes
AES-Light (cryptographic services)		4
Arm® Cortex®-M4	Multipurpose accelerator in lockstep (DSPH)	1
	Multi-purpose accelerator in lockstep (DME)	1
Standby and smart power modes		Yes
eDMA engines (number of channels, more channels through muxes/channel)	Engine	4
	Channel	3× 32 1× 64

Feature		SR6G7C6, SR6G7C4
Audio over Ethernet enhancements: • Ethernet controller with AVB support • Media clock recovery (optional: integrated audio PLL) • Integrated interchip sound (I²S)/time-division multiplexed (TDM) interfaces • Optional: integrated sample rate converters		No
I²S with TDM		No
LIN and UART (LINFlexD)		28
CAN_FD		20
CAN_XL		No
SPIQ (with LVDS channel)		10 (0)
SENT	Unit	2
	Channel/unit	15
I²C		2
DSPI		2
PSI5	Unit	2
	Channel/unit	2 channels
FlexRay™ (dual channel)		2
Gigabit ethernet IEEE 802.3-2008 compliant	Total	2
	With MII, RMII, RGMII, and SGMII	1
	With RMII and SGMII	1
Flexible and safe Ethernet switch (FLEX_SGS) with L2/L2+ routing features: • IEEE 802.3 • IEEE 802.1Qav-2009 (forwarding and queuing) • IEEE 802.1AS-2011 (time synchronization) • IEEE 802.1Qbv-2015 (time-aware shaper) • IEEE 1588 PTP (with pulse-per-second output) • IEEE 1722 AVBTP (with media clock generation and recovery)		No
PCI Express® (PCIe®) Gen2		No
SIPI/LFAST interprocessor bus		2
Generic timer modules (GTM4)		GTM4154
High-resolution timer		No
12-bit SAR analog converters		8
9-bit SAR analog converters for low-power modes		1
Octo-SPI (support HyperBus™ memory devices)		Yes
SDMMC interface		Yes
Debug port	Main debug port (JTAG+SWD)	Yes
	Secondary debug port (SWD)	Yes
High-speed off-chip trace lane (multi GBit/s, Aurora™ protocol)		4
Max temperature (target)	Junction temperature	150 °C
Packages	FPBGA476	X
	FPBGA292	X

1.3 Block diagram

The figure below shows the top-level block diagram.

Figure 1. Block diagram



1. *Emulated by GTM.*

Revision history

Table 2. Document revision history

Date	Version	Changes
01-Jun-2021	1	Initial ST Restricted release.
12-Aug-2021	2	Second ST Restricted release.
21-Jun-2022	3	Initial public release.
24-Jun-2022	4	Figure 1. Block diagram: replaced Cortex®-R52 by Cortex®-R52+.
23-Sep-2022	5	In the whole document, minor editorial changes. • document title: updated RAM size from 8.9 to 9.1 MB • Security: 2nd generation hardware security module: added cybersecurity compliance. • Peripheral, I/O, and communication interfaces: – updated "12 separate 12-bit SAR..." to "8 separate 12-bit SAR... – removed bullet "High-resolution timer..." • Section 1.1: Document overview: added "SR6G7x" in the first sentence • Table 1. SR6G7C6, SR6G7C4 overview: – "Arm®Cortex®-M4, Multi-purpose accelerator (DSPH)" line: added in lockstep – set "CAN-XL" to "No" – set "High-resolution timer" "SR6G7x" column to "No" – set "16-bit sigma-delta analog converters (units with DSPL)" "SR6G7x" column to "No" – "12-bit SAR analog converters": changed 12 to 8 – set "9-bit SAR analog comparators" "SR6G7x" column to "No"
18-Oct-2024	6	• Section Features updated • Section 1.2: Description updated • Glossary added
22-Oct-2024	7	Section Features first bullet point updated.

Glossary

ADC Analog-to-digital converter

AEC Automotive Electronics Council. Also known as CDF-AEC for Chrysler-Delco-Ford Automotive Electronics Council. Shortened to AEC.

AES Advanced encryption standard. Cryptographic algorithm.

ASIL Automotive safety integrity level

It is a risk classification system defined by the ISO 26262 standard for the functional safety of road vehicles. There are four ASILs identified by ISO 26262—A, B, C, and D. ASIL A represents the lowest degree and ASIL D represents the highest degree of automotive hazard.

AVB Audio-video bridging

BCS Boot code sector

BSC Basic (dimension)

CAN Controller area network

CAN FD® Controller area network flexible data rate

CBC Cipher block chaining

CDM Charged device model

CFB Cipher feedback

CGM Clock generation module

CMAC Cipher-based message authentication code

CMD Command

CMOS Complementary metal-oxide-semiconductor

COL Collision detect

Asynchronous receiver signal of the media-independent interface (MII).

CPHA Clock phase bit. Selects the clock phase.

CPOL Clock polarity bit. Selects the clock polarity.

CPU Central processing unit

CRC Cyclic redundancy check

CRS Carrier sense

Asynchronous receiver signal of the media-independent interface (MII).

CTI Arm® CoreSight™ cross-trigger interface

CTM Cross-trigger matrix

CTR Counter mode

CXPI Clock extension peripheral interface

DAC Digital-to-analog converter

DC Direct current

DCF Device configuration format

DDR Double data rate

DMA Direct memory access

DNL Differential nonlinearity

DS Default speed

DSPI Deserial serial peripheral interface

DTR Double transfer rate

eDMA Enhanced direct memory access

EMC Electromagnetic compatibility

EVITA e-safety vehicle intrusion protected applications

FCCU Fault collection and control unit

FPBGA Fine-pitch-ball-grid-array

FPU Floating-point unit

GB Gigabyte

GPIO General-purpose input/output

GTM Generic timer module

HSM Hardware security module

HSSTP High-speed serial trace probe

I/O Input/output

IEC International Electrotechnical Commission

IEEE Institute of Electrical and Electronics Engineers

IPv4 Internet protocol version 4

IPv6 Internet protocol version 6

ISO International Organization for Standardization

I²C Inter-integrated circuit

JEDEC Joint Electron Device Engineering Council

JTAG Joint Test Action Group

KB Kilobyte

LFAST LVDS fast asynchronous serial transmit interface

LIN Local interconnect network

LVDS Low-voltage differential signaling

M_TTCAN Time-triggered controller area network

MB Megabyte

MCAN Modular controller area network

MCU Microcontroller unit

MEMU Memory error management unit

MII Media-independent interface

MSC Microsecond channel

NoC Network on chip

NVM Nonvolatile memory

OS Operating system

OTA Over the air

PHY Physical layer

PLL Phase-locked loop

PSI5 Peripheral sensor interface (PSI5). An interface for automotive sensor applications.

PWM Pulse-width modulation

RAM Random access memory

RMII Reduced media-independent interface

SAR Successive approximation register

SDMMC Secure digital and MultiMediaCard

SENT Single-edge nibble transmission for automotive applications

SeooC Safety element out of context

SGMII Serial gigabit media-independent interface

SIMD Single-instruction multiple data

SIPI Serial interprocessor interface

SPI Serial peripheral interface

SPIQ Queued serial peripheral interface

SRAM Static random-access memory

SRC Sample rate converter

ST STMicroelectronics

STLA Signal tap logic analyzer

SWD Secondary debug port

UART Universal asynchronous receiver/transmitter

VLAN Virtual local area network