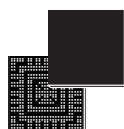


Stellar SR6 G6 line—32-bit Arm® Cortex®-R52+ automotive integration MCU
4× Cortex®-R52+ cores, 31 MB xMemory, 3.8 MB RAM,
with embedded virtualization, safety, and security



FPBGA476
(21.3 × 21.3 mm)



FPBGA292
(17 × 17 mm)



Features

Highlights

- AEC-Q100 qualified
- SR6 integration MCUs:
 - Have superior real-time and safe performance (with highest ASIL-D capability)
 - Bring hardware-based virtualization technology to MCUs for simplified multiple software integrations at optimized performance
 - Have built-in no downtime OTA reprogramming capability (with built-in dual-image mechanism)
 - Offer high-speed security cryptographic services, for example for network authentication

Cores and accelerators

- 4 × 32-bit Cortex®-R52+ cores (2 of them with checker cores, and 2 in split-lock configuration):
 - Configurable as either 4 cores (2 of them in lockstep configuration) or 3 cores (all of them in lockstep configuration)
 - Arm® v8-R compliant
 - Single precision floating-point unit (FPU)
 - New privilege level for real-time virtualization
 - Up to 500 MHz
 - 1 core with Neon™ extensions (for example SIMD, dual precision FPU)
- 2 Cortex®-M4 multipurpose accelerators running at up to 200 MHz, both in lockstep configuration
- 4 eDMA engines in lockstep configuration
- Ethernet switch: L2+ Ethernet switch with 2× 1 GB ports, 2× MACSEC, QoS, AVB, and TSN

Memories

- xMemory: up to 31 MB extensible on-chip nonvolatile memory (NVM) depending on ordered part number:
 - PCM (phase-change memory) as nonvolatile memory
 - Up to 30 MB code NVM, with A/B swap OTA mechanism (up to 2× 15 MB)
 - 1024 KB HSM-dedicated code NVM, with A/B swap OTA mechanism (2× 512 KB)
- 384 KB data NVM (256 KB + 128 KB dedicated to HSM)
- Up to 3840 KB on-chip general-purpose SRAM

Product summary	
Part number	Package
SR6G6C6	FPBGA476
SR6G6C4	FPBGA292

Security: 2nd generation hardware security module

- Cybersecurity: ISO/SAE 21434 compliance (refer to the cybersecurity reference manual for details)
- On-chip high-performance security module with full support for e-safety vehicle intrusion protected applications (EVITA)
- Symmetric and asymmetric cryptography processor
- High-performance lock-stepped AES-light security subsystem for fast ASIL-D cryptographic services
- Two MACsec accelerators integrated on each Ethernet link

Safety: comprehensive new-generation ASIL-D safety concept

- New state-of-the-art safety measures at all levels of the architecture for most efficient implementation of ISO 26262 ASIL-D functionalities
- Complete hardware virtualization architecture built on Cortex®-R52+ new privilege mode (best-in-class software isolation, real-time support for multiple virtual machines/applications)

Device standby/low-power modes

- Versatile low-power modes
- Ultra-low power: standby mode for lowest quiescent current with optimized active subsystem (for example standby RAM) and wake-up capability
- Smart low-power: smart power mode with Cortex®-M4 subsystem, extended communications interfaces, and ADC peripheral

Peripheral, I/O, and communication interfaces

- 24 LINFlexD modules
- 1 dual-channel FlexRay controller
- 10 queued serial peripheral interface (SPIQ) modules
- 2 DSPI with shifted PWM serialization support for lighting applications
- 6 I²C interfaces
- Enhanced audio support that enables audio over Ethernet:
 - Ethernet controller with AVB support
 - Medial clock recovery with integrated audio PLL
 - Two integrated interchip sound (I²S)/time-division multiplexed (TDM) interfaces
 - Integrated sample rate converters (6 channels on each I²S interface)
- 2 SENT modules (4 channels each)
- 2 PSI5 modules (2 channels each)
- 1 peripheral component interconnect express (PCIe) Gen2 controller
 - Gen2 PHY: Gen1 (2.5 GT/s), Gen2 (5.0 GT/s)
 - Gen3 MAC
 - 2 lanes
 - Configurable controller with one or two lanes
- Enhanced analog-to-digital converter system with:
 - 4 separate 12-bit SAR analog converters (including one supervisor/safety ADC).
 - 1× 9-bit SAR analog converter for device standby/low-power mode
- Advanced timed I/O capability:
 - Generic timer module (GTM4184)

- Communication interfaces:
 - Two 10/100/1000 Mbit/s Ethernet controllers compliant with IEEE 802.3-2008: IPv4 and IPv6 checksum modules, AVB, VLAN, and EMC optimized SGMII
 - Two 10 Mbit/s Ethernet controllers compliant with 10BASE-T1S and the OPEN Alliance 3-pin (OA3p) interface
 - 15 modular controller area network (MCAN) modules, and 1 time-triggered controller area network (M_TTCAN), all supporting flexible data rate (ISO CAN FD[®])
 - 2 CAN XL[®] interfaces

External memory interfaces

- 2 octo-SPI IPs to support HyperBus[™] memory (flash/RAM) devices
- 1 SDMMC interface

1 Introduction

1.1 Document overview

This document provides a summary of the target specification and features of the SR6G6 devices. For detailed information, refer to the device Datasheet and device Reference manual.

Note: For information on the Cortex®-R52+ and Cortex®-M4 cores, refer to the technical reference manuals, available from the www.arm.com website.

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1.2 Description

Stellar integration MCUs have been designed to meet the requirements of domain controllers and ECUs with high integration requested in the architectures of connected, updatable, automated, and electrified cars. They have superior real-time and safe performance (with highest ASIL-D capability). Bringing hardware-based virtualization technology to MCUs, they ease the development and integration of multiple source software onto the same hardware while maximizing the resulting software performance. They offer high-efficiency OTA reprogramming capability with fast new image download and activation. They also provide high-speed security cryptographic services, for instance for network authentication.

Table 1. SR6G6 overview

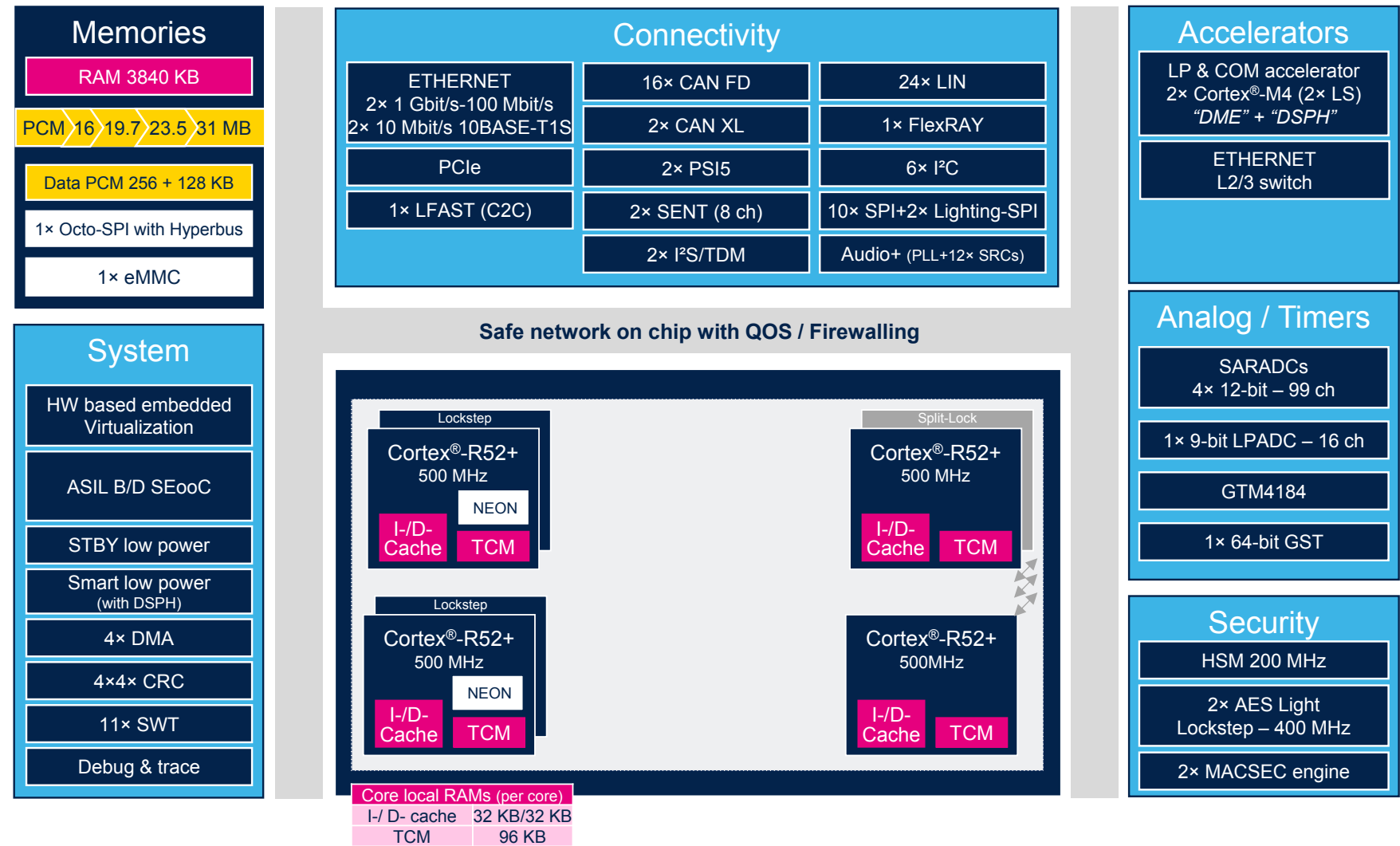
Feature		SR6G6
Cortex®-R52+ cores (+ checker cores)		4 cores (+2 checkers), configurable as 3 cores (+3 checkers)
Neon™ (with SIMD, dual precision floating point)		1
Cache (instruction/data) per core in Kbyte		32/32
Core memory protection unit (regions), several additional protection mechanisms in the architecture, for example: NOC firewalls	Hypervisor (EL2)	24
	OS (EL1)	24
Code NVM	Overall including HSM in Mbytes	16 MB extensible to: 19.75 MB, 23.5 MB or 31 MB (depending on ordered part number)
	Cluster code NVM in Mbytes	30 (depending on ordered part number)
	HSM code NVM in Kbytes	1024
Data NVM in Kbytes		384
RAM in Kbytes		3840
Hardware security module (HSM) - 2 nd generation		Yes
AES-Light (cryptographic services)		4
Arm® Cortex®-M4	Multipurpose accelerator in lockstep (DSPH)	1
	Multi-purpose accelerator in lockstep (DME)	1
Standby and smart power modes		Yes
eDMA engines (number of channels, more channels through muxes/channel)	Engine	4
	Channel	3× 32 1× 64
Audio over Ethernet enhancements: • Ethernet controller with AVB support • Media clock recovery (optional: integrated audio PLL) • Integrated interchip sound (I²S)/time-division multiplexed (TDM) interfaces • Optional: integrated sample rate converters		Yes with integrated audio PLL 2× SRC (6 channels each)

Feature		SR6G6
I ² S with TDM		2
LIN and UART (LINFlexD)		24
CAN_FD		16
CAN_XL		1
SPIQ (with LVDS channel)		10 (0)
SENT	Unit	2
	Channel/unit	15
I ² C		6
DSPI		2
PSI5	Unit	2
	Channel/unit	2 channels
FlexRay™ (dual channel)		1
10/100/1000 Mbit/s Ethernet IEEE 802.3-2008 compliant	Total	2
	With MII, RMII, RGMII, and SGMII	1
	With RMII and SGMII	1
10BASE-T1S Ethernet MAC and PHY with OA3p, the OPEN Alliance 3-pin interface (for 10BASE-T1S transceivers)		2
Line-rate media access control security (MACsec) accelerators		2
Flexible and safe Ethernet switch (FLEX_SGS) with L2/L2+ routing features		Yes
PCI Express® (PCIe®) Gen2		2 lanes
SIPI/LFAST interprocessor bus		1
Generic timer modules GTM4184		Yes
High-resolution timer		No
12-bit SAR analog converters		4
9-bit SAR analog converters for low-power modes		1
Octo-SPI (support HyperBus™ memory devices)		Yes
SDMMC interface		Yes
Debug port	Main debug port (JTAG+SWD)	Yes
	Secondary debug port (SWD)	Yes
High-speed off-chip trace lane (multi Gbit/s, Aurora™ protocol)		2
Maximum temperature (target)	Junction temperature	150°C
Packages	FPBGA257	X
	FPBGA292	X

1.3 Block diagram

The figure below shows the top-level block diagram.

Figure 1. Block diagram



1. Emulated by GTM.



2 Ordering information

Table 2. Ordering information scheme

Example:	SR6	G6	C6	XM	XXXXX	0	R
Device family							
SR6: "Stellar" SR6 family							
Serie / line							
G6: SR6 G series, G6 line							
Package							
C4: FPBGA292							
C6: FPBGA476							
Memory size							
XM: xMemory configuration, extensible from 16 MB to 31 MB							
A0: 16 MB fixed memory configuration							
Device options							
C52FX: default:							
Others: reserved							
Reserved							
Packing							
Y: Tray							
R: Tape and reel (pin 1 top right)							

Revision history

Table 3. Document revision history

Date	Revision	Changes
18-Oct-2024	1	Initial release.
20-Nov-2025	2	<ul style="list-style-type: none"> In the whole document minor editorial changes Updated document title Section Features: updated <ul style="list-style-type: none"> Highlights: added section title Cores and accelerators: updated Memories: updated Table 1. SR6G6 overview: <ul style="list-style-type: none"> Code NVM, Flexible and safe Ethernet: updated Code NVM built-in memory... removed Figure 1. Block diagram: updated Section 2: Ordering information: added Glossary: <ul style="list-style-type: none"> ASIL, NVM, SWD: updated definition xMemory: added

Glossary

ADC Analog-to-digital converter

AEC Automotive Electronics Council. Also known as CDF-AEC for Chrysler-Delco-Ford Automotive Electronics Council. Shortened to AEC.

AES Advanced encryption standard. Cryptographic algorithm.

ASIL Automotive safety integrity level - a risk classification system defined by the ISO 26262 standard for the functional safety of road vehicles; there are four ASILs identified by ISO 26262 — A, B, C, and D, from the lowest to the highest degree of automotive hazard

AVB Audio-video bridging

AVTP Audio-video transport protocol

BCS Boot code sector

BSC Basic (dimension)

CAN Controller area network

CAN FD[®] Controller area network flexible data rate

CAN XL[®] Controller area network extra long

CBC Cipher block chaining

CDM Charged device model

CFB Cipher feedback

CGM Clock generation module

CMAC Cipher-based message authentication code

CMD Command

CMOS Complementary metal-oxide-semiconductor

COL Collision detect

Asynchronous receiver signal of the media-independent interface (MII).

CPHA Clock phase bit. Selects the clock phase.

CPOL Clock polarity bit. Selects the clock polarity.

CPU Central processing unit

CRC Cyclic redundancy check

CRS Carrier sense

Asynchronous receiver signal of the media-independent interface (MII).

CTI Arm[®] CoreSight[™] cross-trigger interface

CTM Cross-trigger matrix

CTR Counter mode

CXPI Clock extension peripheral interface

DAC Digital-to-analog converter

DC Direct current

DCF Device configuration format

DDR Double data rate

DMA Direct memory access

DME Data movement engine

DNL Differential nonlinearity

DS Default speed

DSPI Deserial serial peripheral interface

DTR Double transfer rate

eDMA Enhanced direct memory access

EMC Electromagnetic compatibility

EVITA e-safety vehicle intrusion protected applications

FCCU Fault collection and control unit

FLEX_SGS Flexible safe gateway/switch

FPBGA Fine-pitch-ball-grid-array

FPU Floating-point unit	MCU Microcontroller unit
GB Gigabyte	MEMU Memory error management unit
GPIO General-purpose input/output	MII Media-independent interface
GTM Generic timer module	MSC Microsecond channel
HSM Hardware security module	NoC Network-on-chip
HSSTP High-speed serial trace probe	NVM Nonvolatile memory - a memory that retains its contents even when powered down, such as flash memory or EEPROM
I/O Input/output	OA3p OPEN Alliance 3-pin (interface)
IEC International Electrotechnical Commission	OS Operating system
IEEE Institute of Electrical and Electronics Engineers	OTA Over the air
IPv4 Internet protocol version 4	PCIe® Peripheral component interconnect express
IPv6 Internet protocol version 6	PHY Physical layer
ISO International Organization for Standardization	PLL Phase-locked loop
I²C Inter-integrated circuit	PSI5 Peripheral sensor interface (PSI5). An interface for automotive sensor applications.
I²S Integrated interchip sound	PTP Precision time protocol
JEDEC Joint Electron Device Engineering Council	PWM Pulse-width modulation
JTAG Joint Test Action Group	RAM Random access memory
KB Kilobyte	RGMII Reduced gigabit media-independent interface
LFAST LVDS fast asynchronous serial transmit interface	RMII Reduced media-independent interface
LIN Local interconnect network	SAR Successive approximation register
LVDS Low-voltage differential signaling	SDMMC Secure digital and MultiMediaCard
M_TTCAN Time-triggered controller area network	SENT Single-edge nibble transmission for automotive applications
MAC Media access control	SeooC Safety element out of context
MACsec Media access control security	SGMII Serial gigabit media-independent interface
MB Megabyte	SIMD Single-instruction multiple data
MCAN Modular controller area network	

SIPI Serial interprocessor interface

SPI Serial peripheral interface

SPIQ Queued serial peripheral interface

SRAM Static random-access memory

SRC Sample rate converter

ST STMicroelectronics

STLA Signal tap logic analyzer

SWD Serial wire debug

TDM Time-division multiplexed or multiplexing

UART Universal asynchronous receiver/transmitter

VLAN Virtual local area network

xMemory Extensible embedded non volatile memory

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