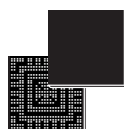




Stellar SR6 G5 line—32-bit Arm® Cortex®-R52+ automotive integration MCU  
4 × Cortex®-R52+ cores, 17 MB xMemory, 3.8 MB RAM,  
with embedded virtualization, safety, and security



FPBGA476  
(21.3 × 21.3 mm)



FPBGA348  
(17 × 17 mm)



FPBGA292  
(17 × 17 mm)



## Features

### Highlights

- AEC-Q100 qualified
- SR6 integration MCUs:
  - Have superior real-time and safe performance (with highest ASIL-D capability)
  - Bring hardware-based virtualization technology to MCUs for simplified multiple software integrations at optimized performance
  - Have built-in no downtime OTA reprogramming capability (with built-in dual-image mechanism)
  - Offer high-speed security cryptographic services, for example for network authentication



### Cores and accelerators

- 4 × 32-bit Cortex®-R52+ cores (2 of them with checker cores, and 2 in split-lock configuration):
  - Configurable as either 4 cores (2 of them in lockstep configuration) or 3 cores (all of them in lockstep configuration)
  - Arm® v8-R compliant
  - Single precision floating-point unit (FPU)
  - New privilege level for real-time virtualization
  - Up to 500 MHz
  - All cores with Arm® Neon™ architecture extension (dual-precision floating-point SIMD unit)
- 2 Cortex®-M4 multipurpose accelerators running at up to 200 MHz, both in lockstep configuration
- 4 eDMA engines in lockstep configuration
- Ethernet switch:
  - 3 external gigabit (GB) ports with line-rate MACsec
  - 6 data + 1 host internal virtualized ports
  - Time-sensitive networking
  - Audio-video transport protocol (AVTP)
  - Media clock recovery/generation
  - L2 forwarding, L2+ routing
  - ASIL-B target

### Product status link

| Part number | Package  |
|-------------|----------|
| SR6G5C6     | FPBGA476 |
| SR6G5C5     | FPBGA348 |
| SR6G5C4     | FPBGA292 |

### Neural processing unit

- Neural ART Accelerator 11
- Energy-efficient NPU capable of accelerating a wide range of neural network models

## Memories

- *xMemory*: up to 17 MB extensible on-chip nonvolatile memory (NVM) depending on ordered part number:
  - PCM (phase-change memory) as nonvolatile memory
  - Up to 16 MB code NVM, with A/B swap OTA mechanism (up to 2× 8 MB)
  - 1024 KB HSM-dedicated code NVM, with A/B swap OTA mechanism (2× 512 KB)
- 384 KB data NVM (256 KB + 128 KB dedicated to HSM)
- Up to 3840 KB on-chip general-purpose SRAM

## Cybersecurity

- Compliant with ISO/SAE 21434 processes
- Secure JTAG life cycle management
- Hardware security module (HSM)
  - NIST SP 800-90B and AIS31 PTG.2-compliant true random number generator (TRNG)
  - Fully isolated 200 MHz security subsystem with dedicated CPU, RAM, NVM, and cryptographic engines
  - Hardware acceleration for cryptographic algorithms including AES-256, RSA-4096, ECC-521, SHA-2, and SHA-3
  - Post-quantum cryptography (PQC) ready with a hash engine accelerating LMS, ML-KEM, and ML-DSA
  - Hardware acceleration for SM2, SM3, and SM4
- Low-latency cryptographic acceleration
  - Lockstep AES-Light accelerator for deterministic, low-latency MAC services
- Secure networking
  - Dedicated line-rate MACsec engine on every Gbit/s Ethernet interface

## Safety: comprehensive new-generation ASIL-D safety concept

- New state-of-the-art safety measures at all levels of the architecture for most efficient implementation of ISO 26262 ASIL-D functionalities
- Complete hardware virtualization architecture built on Cortex®-R52+ new privilege mode (best-in-class software isolation, real-time support for multiple virtual machines/applications)

## Device standby/low-power modes

- Versatile low-power modes
- Ultralow power: standby mode for lowest quiescent current with optimized active subsystem (for example standby RAM) and wake-up capability
- Smart low power: smart power mode with Cortex®-M4 subsystem, extended communications interfaces, and ADC peripheral

## Peripheral, I/O, and communication interfaces

- 24 LINFlexD modules
- 1 dual-channel FlexRay controller
- 15 queued serial peripheral interface (SPIQ) modules
- 2 DSPI with shifted PWM serialization support for lighting applications
- 6 I<sup>2</sup>C interfaces
- Enhanced audio support that enables audio over Ethernet:
  - Ethernet controller with AVB support
  - Media clock recovery with integrated audio PLL
  - Two integrated interchip sound (I<sup>2</sup>S)/time-division multiplexed (TDM) interfaces
  - Integrated sample rate converters (6 channels on each I<sup>2</sup>S interface)

- 2 SENT modules (4 channels each)
- 2 PSI5 modules (2 channels each)
- Enhanced analog-to-digital converter system with:
  - 4 separate 12-bit SAR analog converters (including one supervisor/safety ADC).
  - 1× 9-bit SAR analog converter for device standby/low-power mode
- Advanced timed I/O capability:
  - Generic timer module (GTM4184)
- Communication interfaces:
  - 3 × 10/100/1000 Mbit/s Ethernet controllers compliant with IEEE 802.3-2008 (IPv4 and IPv6 checksum modules, AVB, and VLAN), 2 of which with EMC-optimized SGMII
  - Three 10 Mbit/s Ethernet controllers compliant with 10BASE-T1S and the OPEN Alliance 3-pin (OA3p) interface (optional, depending on the ordered part number)
  - 15 M\_CAN modules and 1 M\_TTCAN module, all 16 supporting CAN classic and CAN FD®
  - 2 XS\_CAN modules supporting CAN classic, CAN FD®, and CAN XL®

#### External memory interfaces

- 2 octo-SPI IP blocks to support HyperBus™ memory (flash/RAM) devices
- 1 SDMMC interface

# 1 Introduction

## 1.1 Document overview

This document provides a summary of the target specification and features of the SR6G5 devices. For detailed information, refer to the device datasheet and reference manual.

The SR6G5 devices are based on Arm® cores with Arm® CoreSight™ and Neon™ technology. For information on the Arm®-Cortex®-R52+ and Arm® Cortex®-M4 cores, refer to the technical reference manuals, available from the [www.arm.com](http://www.arm.com) website.

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## 1.2 Description

Stellar integration MCUs are designed to meet the requirements of domain controllers and ECUs with high integration, as required in the architectures of connected, updatable, automated, and electrified cars. They have superior real-time and safe performance (with the highest ASIL-D capability). Bringing hardware-based virtualization technology to MCUs, they ease the development and integration of multiple-source software on the same hardware while maximizing the resulting software performance. They offer high-efficiency OTA reprogramming capability with fast new image download and activation. They also provide high-speed security cryptographic services, for instance for network authentication.

**Table 1. SR6G5 overview**

| Feature                                                                                                                         |                                             | SR6G5                                                        |
|---------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------|--------------------------------------------------------------|
| Cortex®-R52+ cores (+ checker cores)                                                                                            |                                             | 4 cores (+2 checkers), configurable as 3 cores (+3 checkers) |
| Neon™ (with SIMD, dual precision floating point)                                                                                |                                             | 4                                                            |
| Cache (instruction/data) per core in Kbyte                                                                                      |                                             | 32/32                                                        |
| Core memory protection unit (regions), several additional protection mechanisms in the architecture, for example: NoC firewalls | Hypervisor (EL2)                            | 24                                                           |
|                                                                                                                                 | OS (EL1)                                    | 24                                                           |
| Code NVM                                                                                                                        | Overall including HSM in Mbytes             | Up to 17 MB xMemory (depending on the ordered part number)   |
|                                                                                                                                 | Cluster code NVM in Mbytes                  | Up to 16 MB xMemory (depending on the ordered part number)   |
|                                                                                                                                 | HSM code NVM in Kbytes                      | 1024                                                         |
| Data NVM in Kbytes                                                                                                              |                                             | 384                                                          |
| RAM in Kbytes                                                                                                                   |                                             | 3840                                                         |
| Hardware security module (HSM) - 2 <sup>nd</sup> generation                                                                     |                                             | Yes                                                          |
| AES-Light (cryptographic services)                                                                                              |                                             | 4                                                            |
| Arm® Cortex®-M4                                                                                                                 | Multipurpose accelerator (DSPH)             | 1                                                            |
|                                                                                                                                 | Multi-purpose accelerator in lockstep (DME) | 1                                                            |
| Standby and smart power modes                                                                                                   |                                             | Yes                                                          |

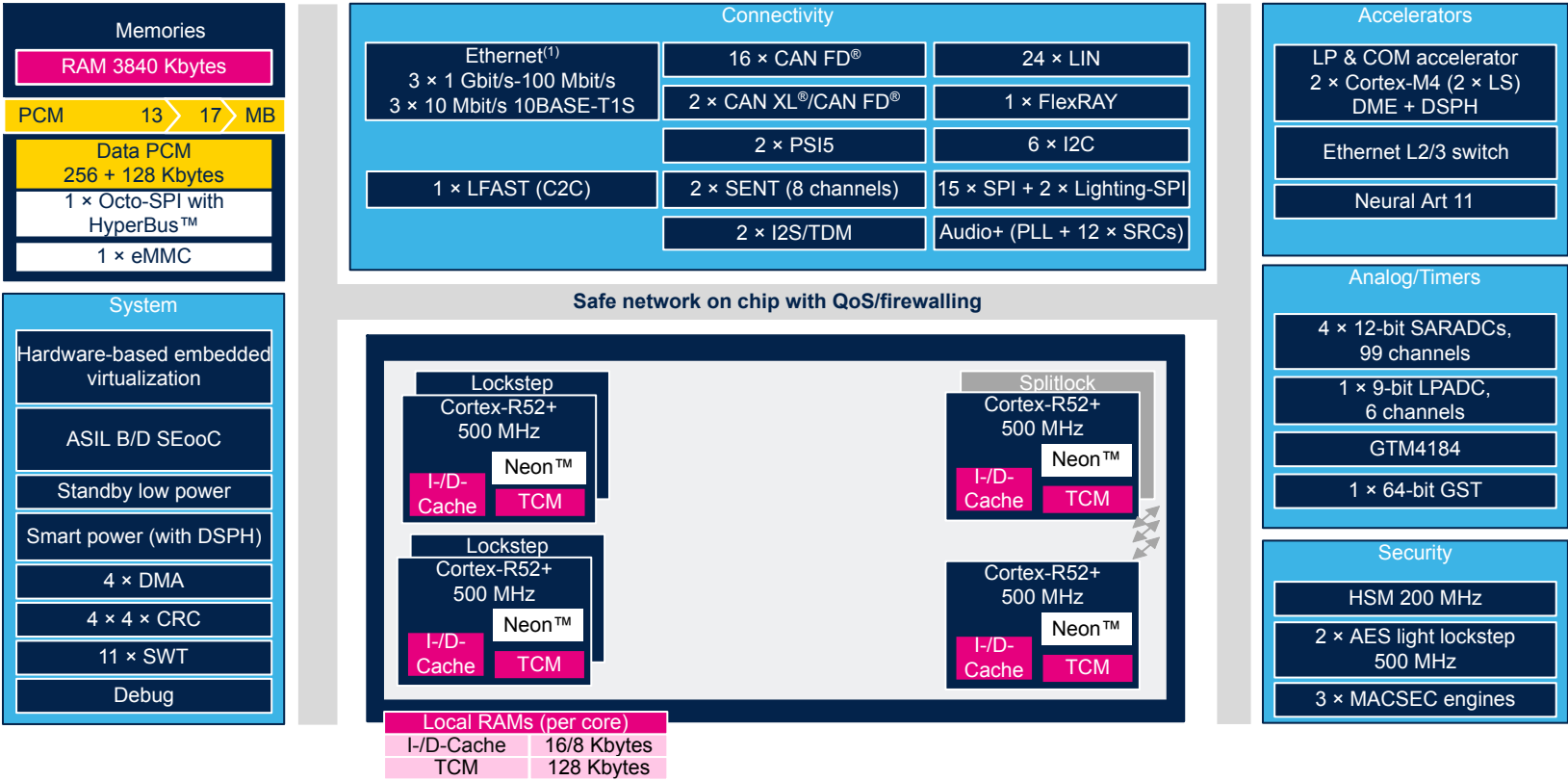
| Feature                                                                                                                                                                                                                                                                                                                                      |                                                                      | SR6G5                                                      |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------|------------------------------------------------------------|
| eDMA engines (number of channels, more channels through muxes/channel)                                                                                                                                                                                                                                                                       | Engine                                                               | 4                                                          |
|                                                                                                                                                                                                                                                                                                                                              | Channel                                                              | 3 × 32<br>1 × 64                                           |
| Audio over Ethernet enhancements: <ul style="list-style-type: none"> <li>Ethernet controller with AVB support</li> <li>Media clock recovery (optional: integrated audio PLL)</li> <li>Integrated interchip sound (I<sup>2</sup>S)/time-division multiplexed (TDM) interfaces</li> <li>Optional: integrated sample rate converters</li> </ul> |                                                                      | Yes with integrated audio PLL<br>2 × SRC (6 channels each) |
| I <sup>2</sup> S with TDM                                                                                                                                                                                                                                                                                                                    |                                                                      | 2                                                          |
| LIN and UART (LINFlexD)                                                                                                                                                                                                                                                                                                                      |                                                                      | 24                                                         |
| CAN_FD                                                                                                                                                                                                                                                                                                                                       |                                                                      | 18 (2 shared with CAN_XL)                                  |
| CAN_XL                                                                                                                                                                                                                                                                                                                                       |                                                                      | 2 (shared with CAN FD)                                     |
| SPIQ (with LVDS channel)                                                                                                                                                                                                                                                                                                                     |                                                                      | 15 (0)                                                     |
| SENT                                                                                                                                                                                                                                                                                                                                         | Unit                                                                 | 2                                                          |
|                                                                                                                                                                                                                                                                                                                                              | Channel/unit                                                         | 15                                                         |
| I <sup>2</sup> C                                                                                                                                                                                                                                                                                                                             |                                                                      | 6                                                          |
| DSPI                                                                                                                                                                                                                                                                                                                                         |                                                                      | 2                                                          |
| PSI5                                                                                                                                                                                                                                                                                                                                         | Unit                                                                 | 2                                                          |
|                                                                                                                                                                                                                                                                                                                                              | Channel/unit                                                         | 2 channels                                                 |
| FlexRay™ (dual channel)                                                                                                                                                                                                                                                                                                                      |                                                                      | 1                                                          |
| 10/100/1000 Mbit/s Ethernet compliant with IEEE 802.3-2008                                                                                                                                                                                                                                                                                   | Total                                                                | 3                                                          |
|                                                                                                                                                                                                                                                                                                                                              | With MII, RMII, RGMII, and SGMII, and 10BASE-T1S/OA3p <sup>(1)</sup> | 1                                                          |
|                                                                                                                                                                                                                                                                                                                                              | With RMII, SGMII, and 10BASE-T1S/OA3p <sup>(1)</sup>                 | 1                                                          |
|                                                                                                                                                                                                                                                                                                                                              | With SGMII and 10BASE-T1S/OA3p <sup>(1)</sup>                        | 1                                                          |
| Line-rate media access control security (MACsec) accelerators                                                                                                                                                                                                                                                                                |                                                                      | 3                                                          |
| Flexible and safe Ethernet switch (FLEX_SGS) with L2/L2+ routing features                                                                                                                                                                                                                                                                    |                                                                      | Yes                                                        |
| SIPI/LFAST interprocessor bus                                                                                                                                                                                                                                                                                                                |                                                                      | 1                                                          |
| Generic timer modules GTM4184                                                                                                                                                                                                                                                                                                                |                                                                      | Yes                                                        |
| High-resolution timer                                                                                                                                                                                                                                                                                                                        |                                                                      | No                                                         |
| 12-bit SAR analog converters                                                                                                                                                                                                                                                                                                                 |                                                                      | 4                                                          |
| 9-bit SAR analog converters for low-power modes                                                                                                                                                                                                                                                                                              |                                                                      | 1                                                          |
| Octo-SPI (support HyperBus™ memory devices)                                                                                                                                                                                                                                                                                                  |                                                                      | Yes                                                        |
| SDMMC interface                                                                                                                                                                                                                                                                                                                              |                                                                      | Yes                                                        |
| Debug port                                                                                                                                                                                                                                                                                                                                   | Main debug port (JTAG+SWD)                                           | Yes                                                        |
|                                                                                                                                                                                                                                                                                                                                              | Secondary debug port (SWD)                                           | Yes                                                        |
| High-speed off-chip trace lane (multi Gbit/s, Aurora™ protocol)                                                                                                                                                                                                                                                                              |                                                                      | No                                                         |
| Maximum temperature (target)                                                                                                                                                                                                                                                                                                                 | Junction temperature                                                 | 150°C                                                      |
| Packages                                                                                                                                                                                                                                                                                                                                     | FPBGA476                                                             | X                                                          |
|                                                                                                                                                                                                                                                                                                                                              | FPBGA348                                                             | X                                                          |
|                                                                                                                                                                                                                                                                                                                                              | FPBGA292                                                             | X                                                          |

1. Optional (depending on the ordered part number).

### 1.3 Block diagram

The figure below shows the top-level block diagram.

Figure 1. Block diagram



1. 10 Mbit/s Ethernet available on a specific part number and pending validation.

## 2 Ordering information

Table 2. Ordering information scheme

|                                                           |     |    |    |    |       |   |   |
|-----------------------------------------------------------|-----|----|----|----|-------|---|---|
| Example:                                                  | SR6 | G5 | C4 | XM | C52FX | 0 | R |
| <b>Device family</b>                                      |     |    |    |    |       |   |   |
| SR6: "Stellar" SR6 family                                 |     |    |    |    |       |   |   |
| <b>Serie / line</b>                                       |     |    |    |    |       |   |   |
| G5: SR6 G series, G5 line                                 |     |    |    |    |       |   |   |
| <b>Package</b>                                            |     |    |    |    |       |   |   |
| C4: FPBGA292                                              |     |    |    |    |       |   |   |
| C5: FPBGA348                                              |     |    |    |    |       |   |   |
| C6: FPBGA476                                              |     |    |    |    |       |   |   |
| <b>Memory size</b>                                        |     |    |    |    |       |   |   |
| XM: xMemory configuration, extensible from 13 MB to 17 MB |     |    |    |    |       |   |   |
| 95: 13 MB fixed memory configuration                      |     |    |    |    |       |   |   |
| <b>Device options</b>                                     |     |    |    |    |       |   |   |
| C52FX: default, without 10BASE-T1S                        |     |    |    |    |       |   |   |
| C52EX: with 10BASE-T1S                                    |     |    |    |    |       |   |   |
| Others: reserved                                          |     |    |    |    |       |   |   |
| <b>Reserved</b>                                           |     |    |    |    |       |   |   |
| <b>Packing</b>                                            |     |    |    |    |       |   |   |
| Y: Tray                                                   |     |    |    |    |       |   |   |
| R: Tape and reel (pin 1 top right)                        |     |    |    |    |       |   |   |

## Revision history

**Table 3. Document revision history**

| Date        | Revision | Changes          |
|-------------|----------|------------------|
| 16-Oct-2026 | 1        | Initial release. |

## Glossary

**ADC** Analog-to-digital converter

**AEC** Automotive Electronics Council. Also known as CDF-AEC for Chrysler-Delco-Ford Automotive Electronics Council. Shortened to AEC.

**AES** Advanced encryption standard. Cryptographic algorithm.

**ASIL** Automotive safety integrity level - a risk classification system defined by the ISO 26262 standard for the functional safety of road vehicles; there are four ASILs identified by ISO 26262 — A, B, C, and D, from the lowest to the highest degree of automotive hazard

**AVB** Audio-video bridging

**AVTP** Audio-video transport protocol

**CAN** Controller area network

**CAN FD<sup>®</sup>** Controller area network flexible data rate

**CPU** Central processing unit

**CRC** Cyclic redundancy check

**DMA** Direct memory access

**DME** Data movement engine

**DS** Default speed

**DSPI** Deserial serial peripheral interface

**eDMA** Enhanced direct memory access

**EMC** Electromagnetic compatibility

**EVITA** e-safety vehicle intrusion protected applications

**FLEX\_SGS** Flexible safe gateway/switch

**FPBGA** Fine-pitch-ball-grid-array

**FPU** Floating-point unit

**GB** Gigabyte

**GTM** Generic timer module

**HSM** Hardware security module

**HSSTP** High-speed serial trace probe

**I/O** Input/output

**I<sup>2</sup>C** Inter-integrated circuit

**IEEE** Institute of Electrical and Electronics Engineers

**IPv4** Internet protocol version 4

**IPv6** Internet protocol version 6

**ISO** International Organization for Standardization

**I<sup>2</sup>S** Integrated interchip sound

**JEDEC** Joint Electron Device Engineering Council

**JTAG** Joint Test Action Group

**KB** Kilobyte

**LFAST** LVDS fast asynchronous serial transmit interface

**LIN** Local interconnect network

**LVDS** Low-voltage differential signaling

**M\_TTCAN** Time-triggered controller area network

**MAC** Media access control

**MACsec** Media access control security

**MB** Megabyte

**MCAN** Modular controller area network

**MCU** Microcontroller unit

**MII** Media-independent interface

**NoC** Network-on-chip

**NPU** Neural processing unit

**NVM** Nonvolatile memory - a memory that retains its contents even when powered down, such as flash memory, PCM, OTP memory, or EEPROM

**OA3p** OPEN Alliance 3-pin (interface)

**OS** Operating system

**OTA** Over the air

**PHY** Physical layer

**PLL** Phase-locked loop

**PSI5** Peripheral sensor interface (PSI5). An interface for automotive sensor applications.

**PWM** Pulse-width modulation

**RAM** Random access memory

**RGMII** Reduced gigabit media-independent interface

**RMII** Reduced media-independent interface

**SAR** Successive approximation register

**SDMMC** Secure digital and MultiMediaCard

**SENT** Single-edge nibble transmission for automotive applications

**SeooC** Safety element out of context

**SGMII** Serial gigabit media-independent interface

**SIMD** Single-instruction multiple data

**SIPI** Serial interprocessor interface

**SPI** Serial peripheral interface

**SPIQ** Queued serial peripheral interface

**SRAM** Static random-access memory

**SRC** Sample rate converter

**ST** STMicroelectronics

**SWD** Serial wire debug

**TDM** Time-division multiplexed or multiplexing

**UART** Universal asynchronous receiver/transmitter

**VLAN** Virtual local area network

**xMemory** Extensible embedded nonvolatile memory

**XS\_CAN** Controller area network extra small

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