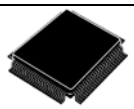
SPC58NE84E7, SPC58NE84C3

32-bit Power Architecture® microcontroller for automotive ASIL-D applications

Data brief - preliminary data

LFBGA292 (17 x 17 x 1.7 mm)



eLQFP176 (24 x 24 x 1.4 mm)

Features

- Two 32-bit Power Architecture® VLE compliant CPU core (e200z4d), dual issue, one of them being paired in lockstep
  - Single-precision floating point operations
  - 8 kB I-Cache and 4 kB D-Cache
  - 16 kB local instruction SRAM and 64 kB local data SRAM
- One 32-bit Power Architecture® VLE compliant CPU core (e200z4d), dual issue, paired in lockstep
  - Single-precision floating point operations
  - Lightweight Signal Processing Auxiliary Processing Unit (LSP APU) instruction support for digital signal processing (DSP)
  - 8 kB I-Cache
  - 16 kB local instruction SRAM and 32 kB local data SRAM
- 6320 kB on-chip flash memory
  - Supporting EEPROM emulation (256 kB)
  - 2 Flash Controller supporting true Read-While-Read Flash access (RWR)
- 608 kB on-chip general-purpose SRAM (+160 kB data RAM included in the CPUs)
- Multi-channel direct memory access controller (eDMA) with 96 channels, paired in lock-step
- Dual phase-locked loops, including one frequency-modulated
- Hardware Security Module (HSM) to provide robust integrity checking of flash memory
- Generic Timer Module (GTM)
  - Intelligent complex timer module
  - 144 channels (40 inputs/104 outputs)
  - 5 programmable fine grain multi-threaded cores
  - 61 kB of dedicated SRAM
  - Hardware support for engine control, motor control and safety related applications
- Enhanced analog-to-digital converter system with:
  - 5 separate 12-bit SAR analog converters, 46 channels, 1.5 µs conversion time, TUE ±4 LSB
  - 3 separate 10-bit SAR analog converters, 16 channels, 1.0µs conversion time, TUE ±2 LSB
  - 6 separate 16-bit Sigma-Delta analog converters, 20 channels
- 10 Deserial Serial Peripheral Interface (DSPI) modules, 18 LIN and UART communication interface (LINFlexD) modules, including 2 Micro Second Bus (MSB) channels
- 7 Modular Controller Area Network (M_CAN), all ISO CAN-FD compliant, and 1 Time-Triggered Controller Area Network (M_TTCAN)
- Dual-channel FlexRay controller, 128 channels
- 15 SENT, 2 PSI5, 1 PSI5-S Hardware Sensor Interfaces
- Boot Assist Module (BAM) through UART/LIN & CAN
- Nexus development interface (NDI) per IEEEISTO 5001-2003 standard, with partial support for 2010 standard.
- Device and board test support per Joint Test Action Group (JTAG) (IEEE 1149.1)
- Three Supply Controller options
  - Dual Supply Controller, 5 V or 3.3 V supply voltage for I/Os, 1.2 V supply voltage for core logic (eLQFP176/LFBGA292)
  - 5 V or 3.3 V on-chip Linear Voltage Regulator with external Ballast (LFBGA292)
  - 5 V DC-DC Voltage Regulator (eLQFP176 / LFBGA292)
- Designed for eLQFP176 0.5 mm pitch, LFBGA292 0.8 mm pitch

Contents

1 Introduction

1.1 Document overview

This document provides an overview of the SPC58NExx family microcontroller unit (MCU).

1.2 Description

SPC58NExx family is the first member of the new SPC58NExx family of 32-bit Flash Automotive MCUs offering a hardware based solution able to answer both ISO26262 ASIL-D compliant and high-performance real-time system requirements for mid/high-end powertrain applications.

Note: This document is preliminary and subject to any change without notification.

1.3 SPC58NExx family system benefits

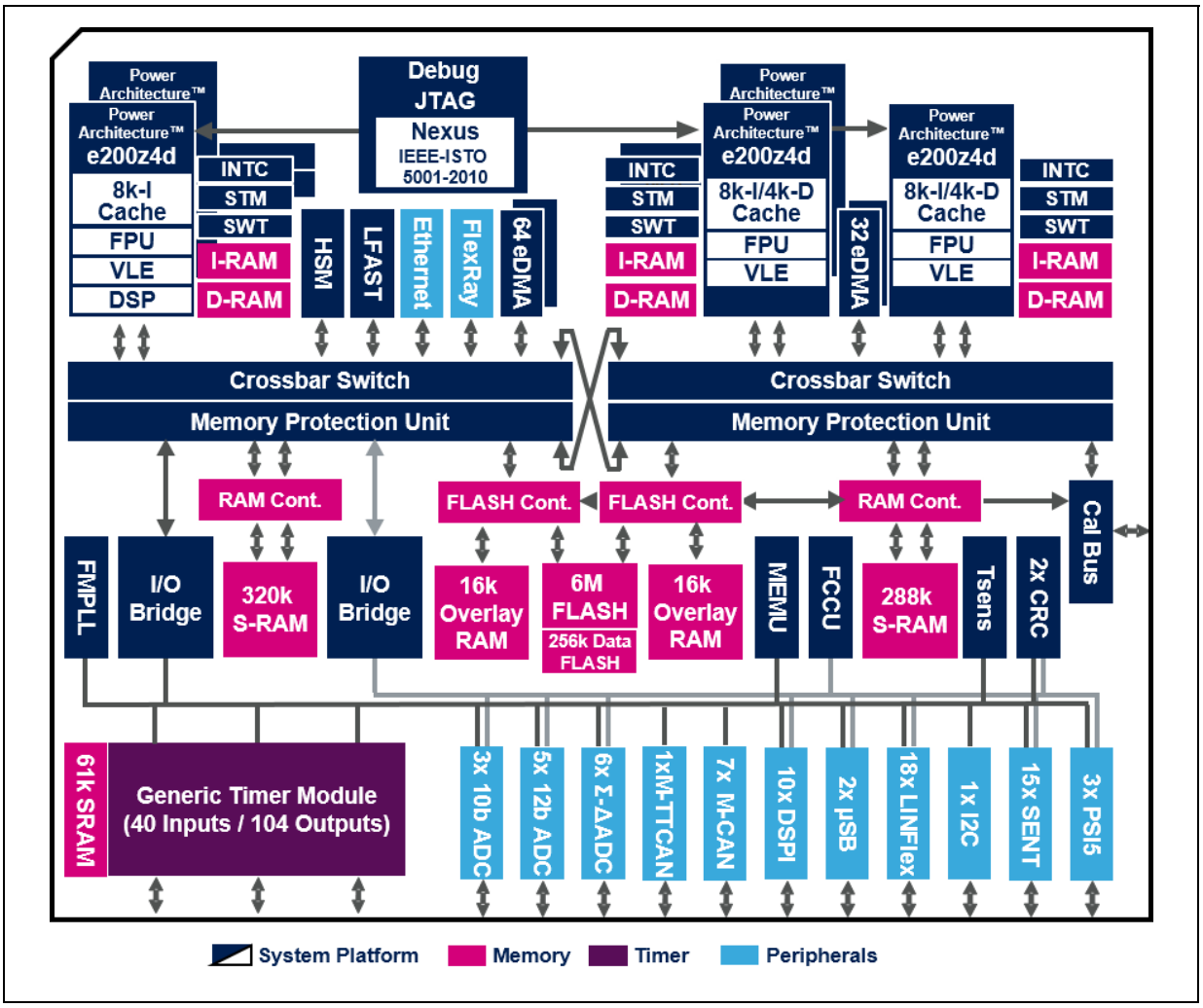
The SPC58NExx family system benefits are the followings:

- Optimized platform architecture (dedicated multi-cores, local memories, true Read-While-Read Flash access (RWR), etc) for best-in-class system performance MCU
- True ASIL-D Safety Element out of Context (SEooC) concept relying on HW measures for reduced SW overhead
- Generic Timer Module (GTM) optimized for Powertrain use while minimizing CPU load
- ISO CAN-FD Hardware Security Module (HSM)
- Hardware Sensor Interface (SENT and PSI5)
- Enhanced communication (LFAST, Ethernet, Micro Second Bus (µSB), etc)
- Increased high dynamic signals acquisition through SD-ADC
- Innovative built-in concept allowing on-chip emulation with production-compatible package (176-pin QFP and 292-pin BGA)

2 Block diagram

Figure 1 shows the top-level block diagram.

Figure 1. SPC58NExx family block diagram



3 ECOPACK®

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

4 Revision history

Table 1. Document revision history

Date	Revision	Changes
15-Apr-2015	1	Initial release.