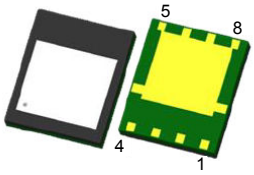
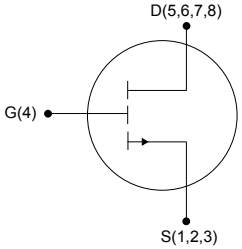
SGT1D5R10MEA

Data brief

100 V, 1.1 mΩ typ., 474 A, e-mode PowerGaN transistor



En-FCLGA 5x6



G4D5678S123

Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D	Series
SGT1D5R10MEA	100 V	1.5 mΩ	474 A	G-HEMT

- Enhancement mode normally off transistor
- Very high switching speed
- High power management capability
- Extremely low capacitances
- Zero reverse recovery charge

Applications

- DC-DC converters
- Motor driver
- Solar system MPPT

Description

The SGT1D5R10MEA is a 100 V, 474 A e-mode PowerGaN transistor. The resulting device provides extremely low conduction losses, high current capability and ultra-fast switching operation to enable high power density and unbeatable efficiency performances.

Product status link
SGT1D5R10MEA

Product summary	
Order code	SGT1D5R10MEA
Marking	1D5R10M
Package	En-FCLGA 5x6
Packing	Tape and reel

1 Electrical ratings

T_C = 25 °C unless otherwise specified.

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	100	V
V_{GS}	Gate-source voltage	-4 to 6	V
I_D	Drain current (continuous) at T_C = 25 °C	474	A
	Drain current (continuous) at T_C = 100 °C	300	
I_{DM}	Pulse drain current (V_{GS} = 5 V, T_J = 25 °C, t_p = 100 µs)	980	A
P_{TOT}	Total power dissipation at T_C = 25 °C	658	W
T_{stg}	Storage temperature range	-55 to 150	°C
T_J	Operating junction temperature range	-40 to 150	°C

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	0.2	°C/W
R_{thJA} (1)	Thermal resistance, junction-to-ambient	38.1	°C/W

1. *When mounted on a standard 1 inch² area of FR-4 PCB with 2-oz copper.*

2 Electrical characteristics

T_C = 25 °C unless otherwise specified.

Table 3. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{DSS}	Drain-source leakage current	V_{GS} = 0 V, V_{DS} = 100 V		2.5	200	µA
		V_{GS} = 0 V, V_{DS} = 100 V, T_J = 125 °C		500		
I_{GSS}	Gate-source leakage current	V_{DS} = 0 V, V_{GS} = 6 V		2	200	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 19 mA	0.9	1.1	2.1	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 5 V, I_D = 2.5 A		1.1	1.5	mΩ

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{GS} = 0 V, V_{DS} = 50 V	-	2350	-	pF
C_{oss}	Output capacitance		-	1010	-	pF
C_{rss}	Reverse transfer capacitance		-	14	-	pF
$C_{o(er)}$ (1)	Equivalent output capacitance energy related	V_{GS} = 0 V, V_{DS} = 50 V	-	1415	-	pF
$C_{o(tr)}$ (2)	Equivalent output capacitance time related		-	2000	-	pF
R_g	Intrinsic gate resistance	f = 5 MHz, I_D = 0 A	-	0.73	-	Ω
V_{plat}	Gate plateau voltage	V_{GS} = 5 V, V_{DS} = 50 V, I_D = 50 A	-	1.9	-	V
Q_g	Total gate charge	V_{GS} = 5 V, V_{DS} = 50 V, I_D = 50 A	-	19	-	nC
Q_{gs}	Gate-source charge		-	4.2	-	nC
Q_{gd}	Gate-drain charge		-	3	-	nC
$Q_{gs(th)}$	Gate charge at treshold		-	2.4	-	nC
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V, V_{DS} = 50 V	-	0	-	nC
Q_{oss}	Output charge		-	100	-	nC

1. *$C_{o(er)}$ is a constant capacitance value that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to the stated value.*
2. *$C_{o(tr)}$ is a constant capacitance value that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to the stated value.*

Table 5. Reverse conduction

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{SD}	Source-drain reverse voltage	V_{GS} = 0 V, I_{SD} = 50 A	-	1.8	-	V

Revision history

Table 6. **Document revision history**

Date	Revision	Changes
08-Oct-2025	1	First release.

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