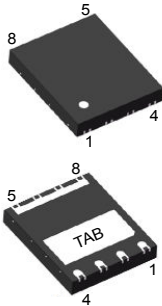
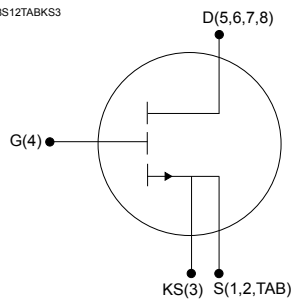


700 V, 101 mΩ typ., 16 A, e-mode PowerGaN transistor



**PowerFLAT 5x6 HV
for PowerGaN**

G4D5678S12TABKS3



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D	Series
SGT130R70FDC	700 V	130 mΩ	16 A	G-HEMT

- Enhancement mode normally off transistor
- Very high switching speed
- High power management capability
- Extremely low capacitances
- Zero reverse recovery charge
- ESD safeguard

Applications

- AC-DC converters
- DC-DC converters
- USB type-C PD adapters and quick chargers
- Wireless charging

Description

The **SGT130R70FDC** is a 700 V, 16 A e-mode PowerGaN transistor. The resulting device provides extremely low conduction losses, high current capability and ultra-fast switching operation to enable high power density and unbeatable efficiency performances.

Product status link

[SGT130R70FDC](#)

Product summary

Order code	SGT130R70FDC
Marking	130R70F
Package	PowerFLAT 5x6 HV for PowerGaN
Packing	Tape and reel

1 Electrical ratings

$T_C = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	700 ⁽¹⁾	V
	Drain-source voltage (transient, $t_p < 200\text{ }\mu\text{s}$)	800	
V_{GS}	Gate-source voltage	-6 to 7	V
I_D	Drain current (continuous)	16 ⁽²⁾	A
I_{DM}	Pulse drain current ($t_p = 10\text{ }\mu\text{s}$)	32	A
P_{TOT}	Total power dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	84	W
T_{stg}	Storage temperature range	-55 to 150	$^{\circ}\text{C}$
T_J	Operating junction temperature range		$^{\circ}\text{C}$

1. Recommended continuous maximum bus voltage during switching operations should not exceed 450 V.
2. Limited by design.

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	1.46	$^{\circ}\text{C}/\text{W}$
R_{thJA} ⁽¹⁾	Thermal resistance, junction-to-ambient	69.81	$^{\circ}\text{C}/\text{W}$

1. When mounted on a standard 1 inch² area of FR-4 PCB with 2-oz copper.

2 Electrical characteristics

$T_C = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

Table 3. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{DSS}	Drain-source leakage current	$V_{GS} = 0\text{ V}, V_{DS} = 700\text{ V}$		0.6	37.5	μA
		$V_{GS} = 0\text{ V}, V_{DS} = 700\text{ V}, T_J = 150\text{ }^{\circ}\text{C}$		4		
I_{GSS}	Gate-source leakage current	$V_{DS} = 0\text{ V}, V_{GS} = 6\text{ V}$		40		μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 14.3\text{ mA}$	1.2	1.7	2.5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 6\text{ V}, I_D = 5\text{ A}$		101	130	$\text{m}\Omega$
		$V_{GS} = 6\text{ V}, I_D = 5\text{ A}, T_J = 150\text{ }^{\circ}\text{C}$		230		

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{GS} = 0\text{ V}, V_{DS} = 400\text{ V}, f = 100\text{ kHz}$	-	101	-	pF
C_{oss}	Output capacitance		-	36.5	-	pF
C_{rss}	Reverse transfer capacitance		-	0.4	-	pF
$C_{o(er)}^{(1)}$	Equivalent output capacitance energy related	$V_{GS} = 0\text{ V}, V_{DS} = 0\text{ to }400\text{ V}$	-	49	-	pF
$C_{o(tr)}^{(2)}$	Equivalent output capacitance time related		-	65	-	pF
R_g	Intrinsic gate resistance	$f = 5\text{ MHz}, I_D = 0\text{ A}$	-	7	-	Ω
V_{plat}	Gate plateau voltage	$V_{DS} = 400\text{ V}, I_D = 5\text{ A}$	-	2.1	-	V
Q_g	Total gate charge	$V_{GS} = 0\text{ to }6\text{ V}, V_{DS} = 400\text{ V}, I_D = 5\text{ A}$	-	2.65	-	nC
Q_{gs}	Gate-source charge		-	0.22	-	nC
Q_{gd}	Gate-drain charge		-	1.02	-	nC
Q_{rr}	Reverse recovery charge	$V_{GS} = 0\text{ V}, V_{DS} = 400\text{ V}$	-	0	-	nC
Q_{oss}	Output charge		-	25.5	-	nC

- $C_{o(er)}$ is a constant capacitance value that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to the stated value.
- $C_{o(tr)}$ is a constant capacitance value that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to the stated value.

Table 5. Reverse conduction

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{SD}	Source-drain reverse voltage	$V_{GS} = 0\text{ V}, I_{SD} = 5\text{ A}$	-	2.4	-	V

Revision history

Table 6. Document revision history

Date	Revision	Changes
08-Oct-2025	1	First release.

IMPORTANT NOTICE – READ CAREFULLY

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice.

In the event of any conflict between the provisions of this document and the provisions of any contractual arrangement in force between the purchasers and ST, the provisions of such contractual arrangement shall prevail.

The purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgment.

The purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of the purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

If the purchasers identify an ST product that meets their functional and performance requirements but that is not designated for the purchasers' market segment, the purchasers shall contact ST for more information.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, refer to www.st.com/trademarks. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2025 STMicroelectronics – All rights reserved