L9965TE

Data brief

Automotive SPI to isolated SPI transceiver

Features

- AEC-Q100 qualified
  - Temperature grade 1: –40°C to +125°C operating temperature range
  - HBM ESD classification level 2
  - CDM ESD classification level C4B
- Full ISO26262 compliant, ASIL-D systems ready, documentation available
- Automatic wake-up of BMS/BMU MCU and PMIC from SHUTDOWN/SLEEP in case of fault detected in the chain
- Single or dual channel p/n in the same package for ring connection
- Up to 59 devices in chain supported
- Cable lengths verified up to 10 meters
- 10 MHz 4-wire SPI interface
- 4 Mbps 2-wire vertical interface (VIF)
- Supports both transformer and capacitive isolation
- Compressed burst data read for enhanced communication speed over the whole chain
- Broadcast write command to configure and control all devices in the chain (or a subset)
- Very Low EMI susceptibility and emissions
- Compatible with 3.3 V and 5 V logics
- Supply voltage from 6 to 24 V

Application

- Automotive battery monitoring systems 
- Energy storage systems
- UPS

Table 1. Ordering information

Order code	Package	Packing
L9965TE-TR	LQFP32 7x7 mm	Tape and reel
L9965TSE-TR		Tape and reel

Description

L9965TE and L9965TSE are bidirectional SPI transceivers that, in a BMS system, allow communication between isolated devices into different voltage domains through a twisted-pair connection. The devices belong to the L9965 chipset family for high-voltage battery management systems monitoring and control.

1 Overview

In a high-voltage battery management system, the master microcontroller accesses the cells monitor and the pack current monitor devices for diagnostics and control purposes. Since the different BMS ICs are located into different voltage domains, it is required isolated communication between each other.

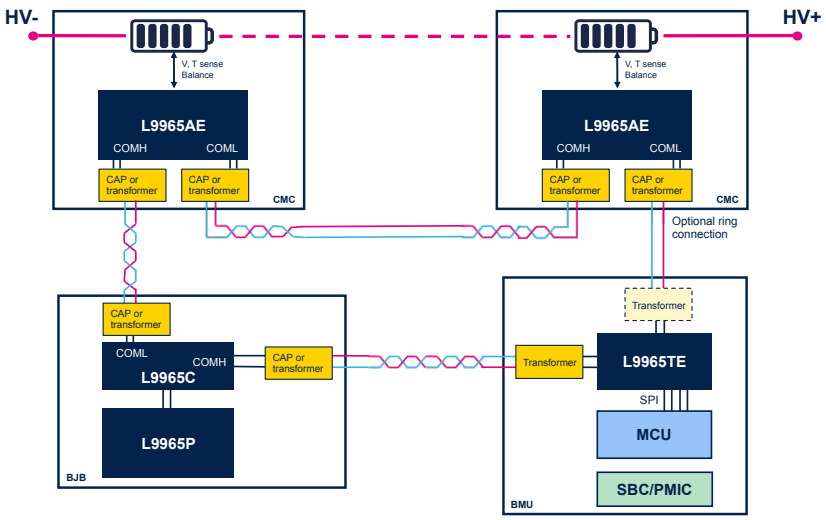
The L9965TE/L9965TSE allows isolated daisy chain connection through a simple two-wire protocol in L9965x-based HV BMS applications. It converts data from a standard 4-wire SPI protocol to a 2-wire proprietary protocol (and vice versa), supporting the signals isolation by capacitors or transformers.

All the devices in the daisy chain recognize the protocol and can be addressed in read-write mode by a single transceiver. Ring connection can be implemented by the dual-channel device L9965TE.

L9965TE/L9965TSE implements two physical communication interfaces:

- SPI target interface: This interface is used by the controller MCU to configure and send commands to L9965TE/L9965TSE and, through it, to all the devices in the chain.
- Isolated vertical interface (VIF): This interface is typically used to connect BMS daisy-chained devices L9965AE/C to L9965TE/L9965TSE and to each other on the VIF bus.

Figure 1. L9965TE in a L9965x-based BMS system



The L9965TE/L9965TSE manages periodic wake-up of the devices in the chain for diagnostic purposes, and it is sensitive to fault tones from the devices in the chain when in low-power mode. It implements a set of commands to optimize the communication over the chain:

- Broadcast command, to write and configure all devices in the chain (or a subset)
- Burst and compressed burst read, to enable high data rate transmission from all devices in the chain with negligible impact on the power consumption
- Go-to-sleep command, to move all devices in the chain in low-power mode
- FAULT/WAKEUP tone, to wake-up the chain for normal operation or faults signaling
- CYCLIC WAKEUP tone, to trigger periodic diagnostic execution in the devices in the chain.

These functionalities are implemented using different functional states, to optimize system power consumption:

- NORMAL: full operation mode
- CYCLIC WAKEUP/CYCLIC COUNT: low-power modes to send a periodic tone and trigger cyclic diagnostics in the chained devices during low-power operation. In these states, the device is sensitive to wake-up tones both from the VIF in case of fault and from the SPI by the MCU
- DEEP SLEEP: Ultralow power state for managing long inactivity periods. In this state, the device is sensitive to wake-up tones both from the VIF in case of fault and from the SPI by the MCU.

Revision history

Table 2. **Document revision history**

Date	Version	Changes
28-Apr-2026	1	Initial release.

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