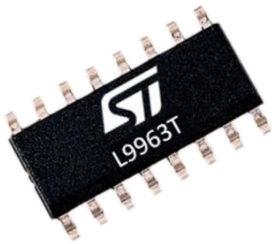
L9963T

Data brief

Automotive general purpose SPI to isolated SPI transceiver



Features

- AEC-Q100 qualified
- Full ISO26262 compliant, ASIL-D systems ready
- Compatible with both 3.3 V and 5 V logics
- Supports both XFMR and Capacitive isolation
- 10 MHz SPI peripheral for SPI Slave operation. Configuratble SPI frequency (250 kHz to 8 MHz) for SPI Master operation
- 333 kbps and 2.66 Mbps Vertical InterFace (VIF) for isolated SPI communication
- Low standby current

Application

- Automotive: 48 V and high-voltage systems
- Backup energy storage systems and UPS
- Industrial communication networks
- Portable and semi-portable equipment
- Remote sensors

Description

L9963T is a general purpose SPI to isolated SPI transceiver intended to create a communication bridge between devices located into different voltage domains.

L9963T is able to transfer communication data incoming from a classical 4-wire based SPI interface to a 2-wire isolated interface (and viceversa).

The transceiver supports both transformer and capacitive isolation, since the isolated signal generated according a propetary protocol is suitable to be transmitted over both decoupling circuitries.

The device can be configured either as Slave or as Master of the SPI bus and supports any protocol made of SPI frames 8 to 64 bit long. The transceiver manages the transfer of the information without performing any protocol check.

SPI peripheral can work up to 10 MHz when configured as Slave. SPI clock frequency can be programmed among (250 kHz; 1 MHz; 4 MHz; 8 MHz) when configured as Master.

Isolated SPI peripheral features two different operating modes: slow @333 kbps and fast @2.66 Mbps.

The asynchronicity between the two sides is internally managed, allowing all possible configuration frequencies on both peripherals to be used in application.

L9963T features an internal queue of 3 slots for the frames received on the SPI port and a queue of 20 slots for the ones received on the isolated SPI side. This allows buffering and decoupling the two different clock domains.

The device is natively compatible with L9963 isolated SPI, allowing its usage in the BMS applications.

L9963T is compatible with both 3.3 V and 5 V logics.

Product status link
L9963T

Product label
SUSTAINABLE TECHNOLOGY

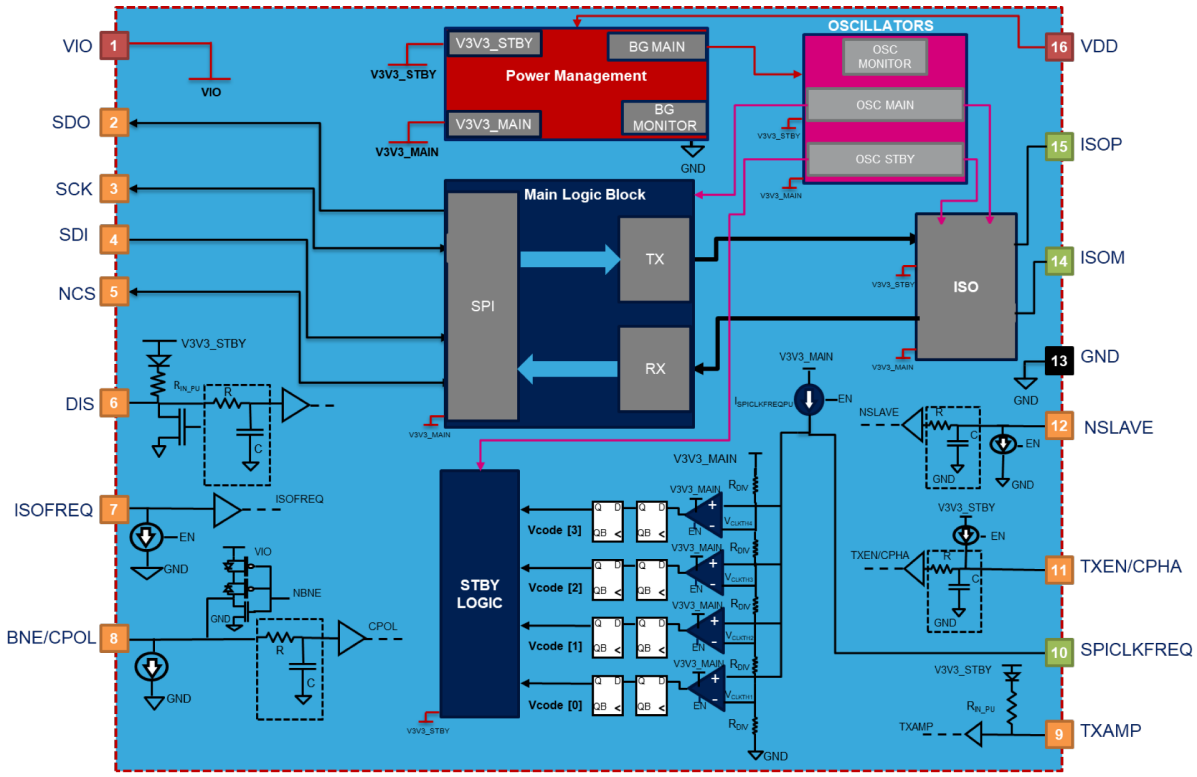
Product summary

Order code	Package	Packing
L9963T	SO16N	Tube
L9963T-TR		Tape&Reel

1 Block diagram and pin description

1.1 Block diagram

Figure 1. **Block diagram**



1.2 Pin description

Figure 2. **Pin connection diagram (top view)**

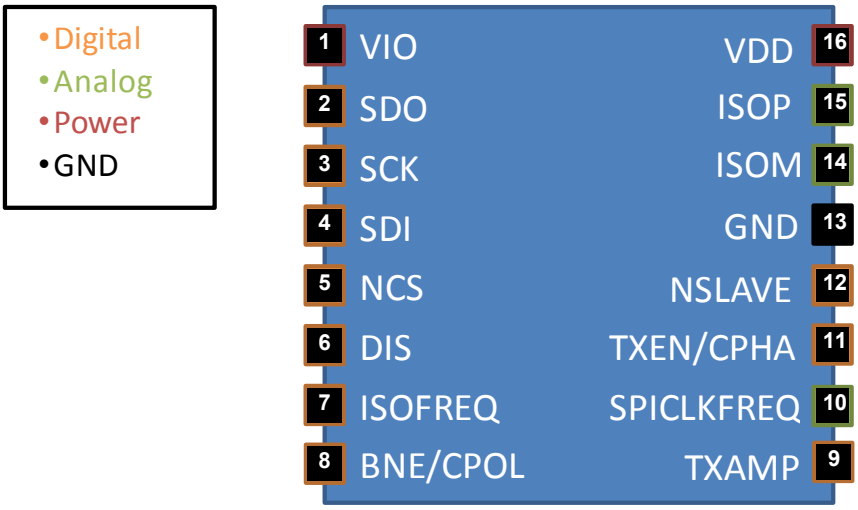


Table 1. Pin list description

Pin#	Type		Local/ Global	Active	Description
POWER					
VDD	Power		Local	-	5V supply input for internal logic and isolated SPI
VIO	Power		Local	-	Digital Output Buffer Supply. Connect either to 5 V or to 3.3 V supply.
GND	Ground		Local	-	Device Ground
SPI					
SDO	Digital Output (Push-Pull)		Local	-	SPI Serial Data Output. Needs external pullup/pulldown resistor to define inactive level.
SCK	Digital Input/ Output (Push-Pull)	NSLAVE = 0 → Digital Input NSLAVE = 1 → Digital Output	Local	-	SPI Serial Clock. Internally pulled down with 100 kΩ
SDI	Digital Input		Local	-	SPI Serial Data Input. Internally pulled down with a 100 kΩ resistor for safety purposes.
NCS	Digital Input/ Output (Push-Pull)	NSLAVE = 0 → Digital Input NSLAVE = 1 → Digital Output	Local	-	SPI Chip Select. Internally pulled up with a 100 kΩ resistor for safety purposes.
BNE/CPOL	NSLAVE = 0 → BNE Digital Output (Push-Pull)		Local	High	SDO Buffer Not Empty flag. It is set high when at least one frame is in the RX buffer. It is set low when RX buffer is empty. When L9963T is configured as Slave, connect this pin to MCU GPIO for interrupt/polling based communication.
	NSLAVE = 1 → CPOL Digital Input		Local	-	SPI Clock Polarity selection input. Latched during Trimming & Config Latch. Connect either to VDD (CPOL = 1) or to GND (CPOL = 0). Internally pulled down (active). Input filtered with RC filter having $f_{CUT\_DIG\_IN}$ cut frequency.
NSLAVE	Digital Input		Local	-	SPI Slave/Master selection. Latched during Trimming & Config Latch Connect to GND to select Slave operation. Connect to VDD to select Master operation. Internally pulled down (active). Input filtered with RC filter having $f_{CUT\_DIG\_IN}$ cut frequency.
TXEN/CPHA	NSLAVE = 0 → TXEN Digital Input		Local	High	Transmitter enable signal. Set high to enable the TX activity. Pull down to disable TX. Any data received on the SDI line while TXEN is low will be discarded and not stored into TX buffer. Internally pulled up (active). Input filtered with RC filter having $f_{CUT\_DIG\_IN}$ cut frequency.

Pin#	Type	Local/ Global	Active	Description
TXEN/CPHA	NSLAVE = 0 → CPHA Digital Input	Local	-	SPI Clock Phase selection input. Latched during Trimming & Config Latch. Connect either to VDD (CPHA = 1) or to GND (CPHA = 0). Internally pulled up (active). Input filtered with RC filter having $f_{CUT\_DIG\_IN}$ cut frequency.
SPICLKFREQ	Analog Input	Local	-	SPI Master Clock selection. Latched during Trimming & Config Latch. Leave open to set minimum frequency. Connect a pulldown resistor to set a higher frequency. Input filtered with RC filter having $f_{CUT\_DIG\_IN}$ cut frequency.
ISOLATED SPI				
ISOP	Analog Input/Output	Global	-	Isolated SPI Positive terminal
ISOM	Analog Input/Output	Global	-	Isolated SPI Negative terminal
TXAMP	Digital Input	Local	-	Isolated SPI TX amplitude selection. Set low to select low amplitude/low threshold. Set high to select high amplitude/high threshold. Internally pulled up with a 100 kΩ resistor.
ISOFREQ	Digital Input	Local	-	Isolated SPI operating frequency selection. Pull high to set high frequency. Pull down to set low frequency. Internally pulled down (active).
DISABLE				
DIS	Digital Input/Output (Open Drain)	Local	High	Transceiver Disable Input. Pull it up with external resistor connected to VIO. When DIS is high, L9963 enters in low power mode. When DIS is low, L9963T is enabled and working in Normal mode. It can be either pulled-down by the MCU to enable the unit, or pulled down internally when a wakeup condition occurs, in order to interrupt the MCU. Pin is internally pulled up with 100 kΩ resistor. Input filtered with RC filter having $f_{CUT\_DIG\_IN}$ cut frequency.

2 Product electrical and thermal ratings

2.1 Supply ranges

Figure 3 lists the product power supply ranges:

- Within the range of functionality the part operates as specified and without parameter deviations. All the functionalities and the electrical parameters are guaranteed.
- If either the upper or the lower limited operating range is reached, the device may not operate properly. Only a limited set of functionalities and electrical parameters are guaranteed. However, neither damage nor parameter deviation occurs, and the device will operate properly once returned to the range of functionality.
- If AMR are violated, permanent damage or parametric deviation may occur.

Figure 3. Supply ranges

Note: all voltages are related to the potential at substrate ground GND.

2.2 Operating range

Table 2. Pin operating range

Pin	Condition	Min	Typ	Max	Unit
VDD	Supply pin	4.5	-	5.5	V
VIO	Digital Output Buffers supply pin	3.0	-	5.5	V
DIS, ISOFREQ, BNE/CPOL, TXAMP, TXEN/CPHA, NSLAVE	Digital I/Os	0	-	VIO	V
|ISOP + ISOM| / 2	Isolated SPI Common Mode Voltage	1	1.2	1.4	V
|ISOP – ISOM|	Isolated SPI Differential Voltage	0	-	2.5	V
SDO, SCK, SDI, NCS	SPI pins	0	-	VIO	V
SPICLKFREQ	Analog Input	0	-	VDD	V

Note: all voltages are related to the potential at substrate ground GND.

2.3 Absolute maximum rating

Table 3. Absolute maximum rating

Symbol	Parameter	Min	typ	Max	Unit
VIO, VDD	Supply Input Voltage	-0.3	-	6.5	V
BNE/CPOL, NSLAVE, DIS, TXEN/CPHA, ISOFREQ, TXAMP	Digital I/Os	-0.3	-	6.5	V
ISOP, ISOM	Analog I/Oson isolated SPI side	-0.3	-	6.5	V
SDO, SCK, SDI, NCS	Serial Peripheral Interface Communicati on Ports	-0.3	-	VIO + 0.3	V
SPICLKFRQ	Analog Input for SPI clock frequency selection	-0.3	-	6.5	V

Note: Note: all voltages are related to the potential at substrate ground GND.

2.4 ESD protection

Table 4. ESD protection

Item	Condition	Min	Typ	Max	Unit
All pins Except Isolated Communication Terminals and Global pins(1)	HBM(2)	-2	-	2	KV
Isolated Communication Terminals(1)(2) and Global pins versus all GND connected		-4	-	4	KV
All pins except Corner Pins	CDM(3)	-500	-	500	V
Corner Pins		-750	-	750	V
All pins	Latch up(4)	-100	-	100	mA

1. *Tested per AEC-Q100-002.*
2. *Isolated Communication Terminals: ISOP, ISOM.*
3. *Tested per AEC-Q100-011.*
4. *Tested per AEC-Q100-004, Class-2, Level-A.*

Note: pins are all GND connected together.

2.5 Temperature ranges and thermal data

Table 5. Temperature ranges and thermal data

Symbol	Parameter	Min	Typ	Max	Unit
T_{amb}	Operating and testing temperature (ECU environment)	-40	-	105	°C
T_j	Junction temperature for all parameters	-40	-	125	°C
T_{stg}	Storage temperature	-65	-	125	°C
$R_{THj\text{-}amb}$	Thermal resistance junction-to-ambient	-	-	90	°C/W

3 Communication scenarios

The following section lists the different communication scenarios where L9963T can be exploited.

3.1 Dual access ring

The dual access ring topology allows for a higher communication integrity level, guaranteeing recovery upon single open failure on communication wires. It requires 2 SPI peripherals on the MCU, an additional transceiver unit and another transformer on the MASTER PCB.

Figure 4. Distributed BMS in dual access ring topology

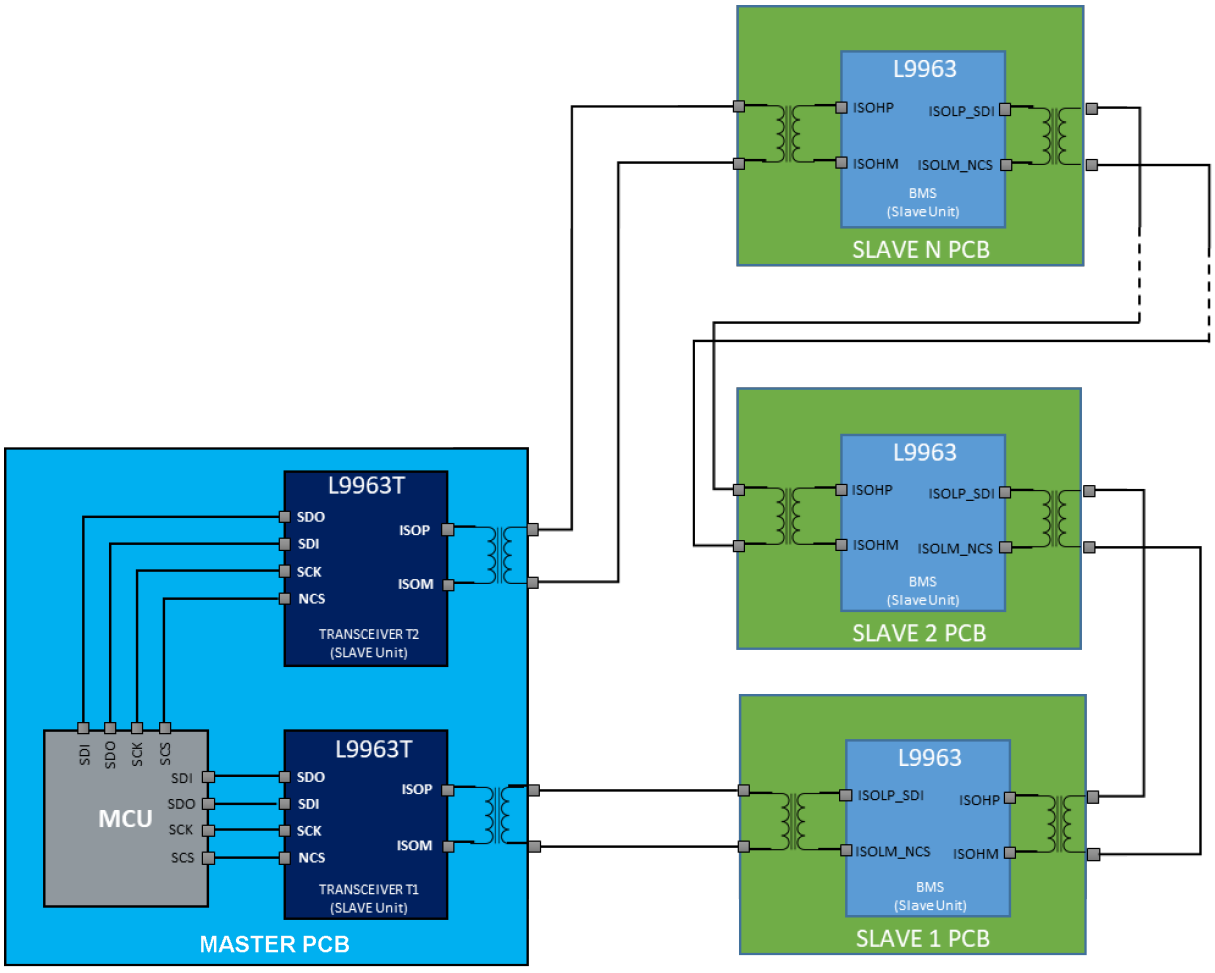
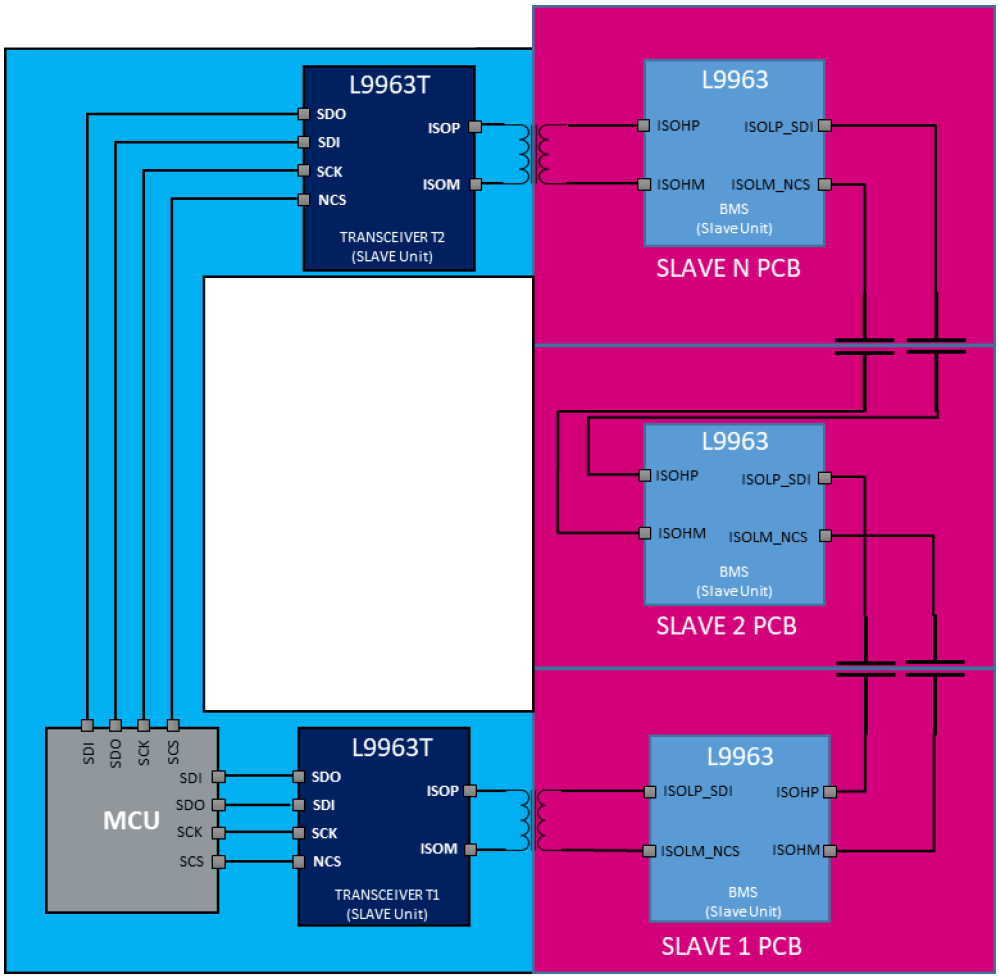


Figure 5. **Centralized BMS in dual access ring topology**

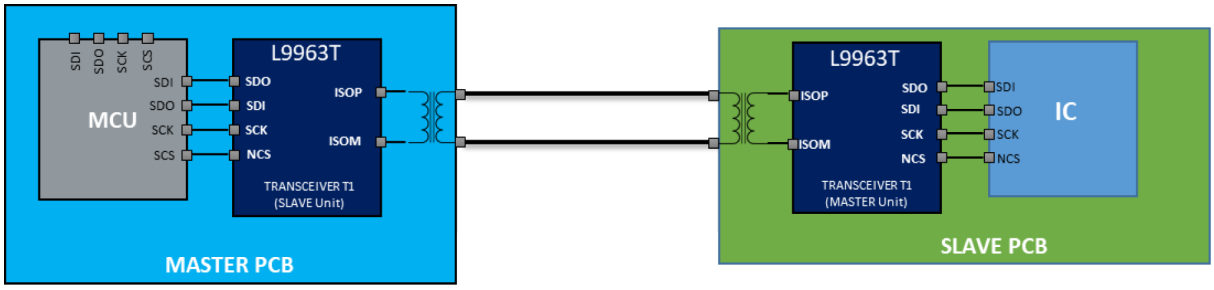


3.2 Generic application

Figure 6 represents a generic application scenario where a master MCU communicates with a generic slave IC located on a different PCB. Communication occurs via two L9963T:

- An L9963T configured as slave translates the SPI frames of the MCU to isolated SPI signals.
- The second L9963T on the right side is configured as SPI Master (NSLAVE = 1) pushing the frames to the slave IC, and sending the information backward.

Figure 6. **Generic application**



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 SO16N (10x4x1.2.5 mm) package information

Figure 7. **SO16N (10x4x1.2.5 mm) package outline**

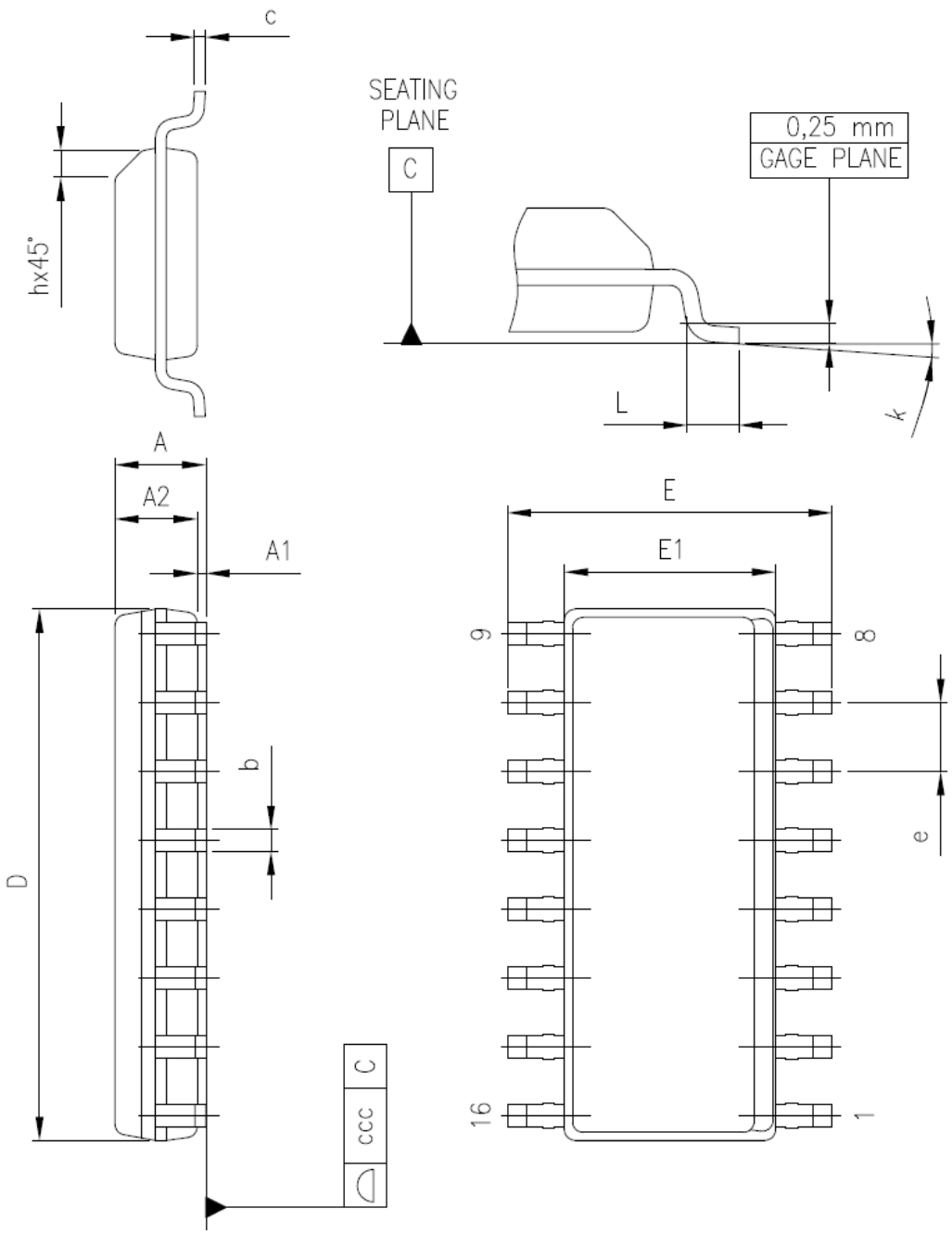


Table 6. SO16N (10x4x1.2.5 mm) package mechanical data

Symbol	Dimensions in mm		
	Min.	Typ.	Max.
A	-	-	1.75
A1	0.10	-	0.25
A2	1.35	-	0.51
b	0.31	-	0.27
c	0.17	-	0.25
D(1)(2)	9.80	9.90	10.00
E	5.80	6.00	6.20
E1(3)	3.80	3.90	4.00
e	-	1.27	-
h	0.25	-	0.50
L	0.40	-	1.27
k	0	-64	8
ccc	-	-	0.10

1. *Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm in total (both side).*
2. *Dimensions referred to the bottom side of the package.*
3. *Dimension "E1" does not include interlead flash or protrusions. Interlead flash, or protrusions or shall not exceed 0.25 mm per side.*

Revision history

Table 7. **Document revision history**

Date	Version	Changes
02-Nov-2020	1	Initial release.

Contents

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