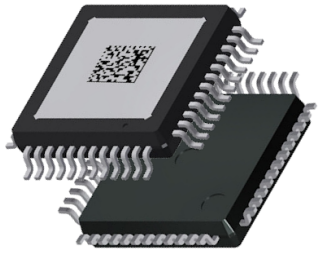
HFDA80P

Data brief

4-channel digital input class-D automotive audio amplifier with Hi-Fi audio quality, in-play diagnostics, 2 MHz switching frequency and parallel mode feature



LQFP48L exposed pad up (7x7x1.4 mm)

Product status link
HFDA80P

Product summary		
Order code	**Package**	**Packing**
HFDA80P-F2Y	LQFP48L 7x7x1.4 mm	Tray
HFDA80P-F2T		Tape and reel

Features

- AEC-Q100 qualified
- Supply operating range: 4.5 V–18 V
- EMI compliance evaluated according to CISPR25
- Class-D BTL outputs
- Integrated 112 dB D/A conversion
- Battery load dump compatible (40 V)
- Reduced size and cost of output LC thanks to 2 MHz switching PWM
- I^2S and TDM digital input (up to 16 channels TDM)
- Selectable input sample rate frequency (44.1/48/96/192 kHz)
- Multiple load configurations:
  - Able to drive 4 Ω and 2 Ω speaker loads
  - Able to drive low impedance load up to 1 Ω in parallel mode
- MOSFET power outputs allowing high output power capability:
  - Typ. 4x29 W on 4 Ω at 14.4 V, 1 kHz, THD = 10%
  - Typ. 4x22.5 W on 4 Ω at 14.4 V, 1 kHz, THD = 1%
  - Typ. 4x47.5 W on 2 Ω at 14.4 V, 1 kHz, THD = 10%
  - Typ. 4x35.5 W on 2 Ω at 14.4 V, 1 kHz, THD = 1%
- Outstanding audio performances
  - THD 0.015% typ. at 1 W 1 kHz on 4 Ω loads
  - Output noise 27 µV typ. A-weighted
  - Crosstalk 100 dB typ. at 1 W 1 kHz on 4 Ω loads
  - PSRR 80 dB typ. at 1 W 1 kHz on 4 Ω loads
- Fast turn-on and very low latency for high-speed audio processing applications
- Very low latency for noise cancelling application
- I²C full configurability with channel independent mute/play/gain selection/ diagnostic
- 4 I²C addresses
- Full diagnostic matrix with info available both on I²C and CD/DIAG pin:
  - 4 thermal warnings
  - Independent by-channel DC and AC load detection diagnostic with selectable threshold
  - Startup diagnostic for shorts to VCC/GND
  - OCP protection with configurable OCP limit (2 selectable)
  - Input offset detector
  - Free-running diagnostics
    - Output current offset detector
    - DC/AC diagnostic
    - Including open-load in play detection
- Parallel mode

- MOSFET power outputs in parallel mode allowing high output power capability:
  - Typ. 2x91 W on 2 Ω at 18 V, 1 kHz, THD = 10%
  - Typ. 2x71 W on 2 Ω at 18 V, 1 kHz, THD = 1%
  - Typ. 2x120 W on 1 Ω at 16 V, 1 kHz, THD = 10%
  - Typ. 2x87 W/1 Ω at 16 V, 1 kHz, THD = 1%
- Synchronization output pin
- Immune to pop/tick noise at turn on/off, battery variations, during diagnostic
- Legacy (backup mode without I²C control)
- Integrated short circuit protections
- ESD integrated protections (2 kV HBM, 500 V / 750 V corner CDM)
- LQFP48L exposed pad up package

Description

The HFDA80P is a new STMicroelectronics class-D audio amplifier, specifically designed for automotive applications in the latest BCD technology.

The HFDA80P integrates advanced solutions for an excellent GSM noise immunity combined with the advantages of 2 MHz switching PWM class-D output stages. This configuration allows outstanding audio performance while designing a compact and inexpensive application.

The HFDA80P supports wide band applications up to 40 kHz, with extremely low level of noise and low THD.

Moreover, it features a broad diagnostics matrix, to support the most demanding OEM requirements in terms of speaker control and system robustness/reliability. The HFDA80P supports start/stop cranking down to 4.5 V and is housed in a very compact and thin LQFP48L 7x7x1.4 mm package, making it suitable for any level of automotive application.

1 Block diagram and pin description

Figure 1. **Block diagram**

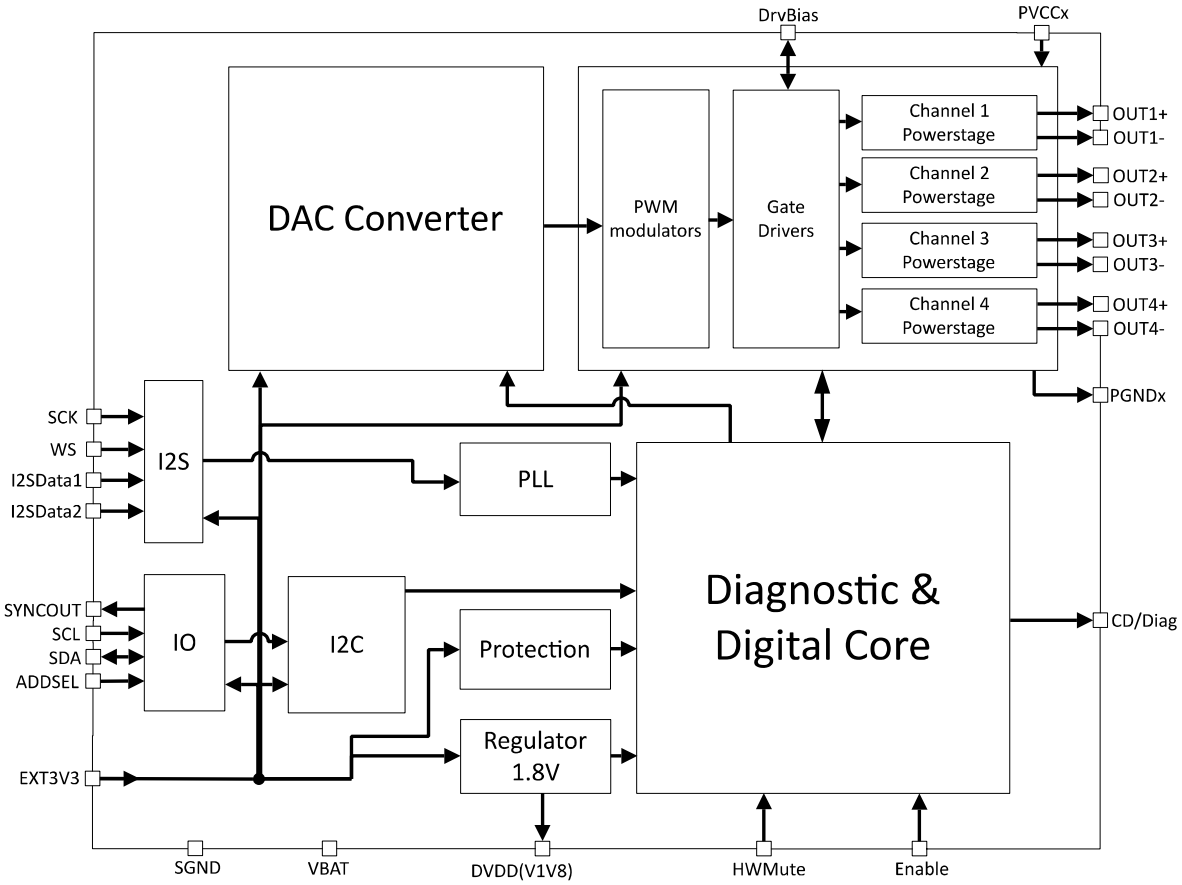


Figure 2. **Pin connection diagram (top view on left, bottom view on right)**

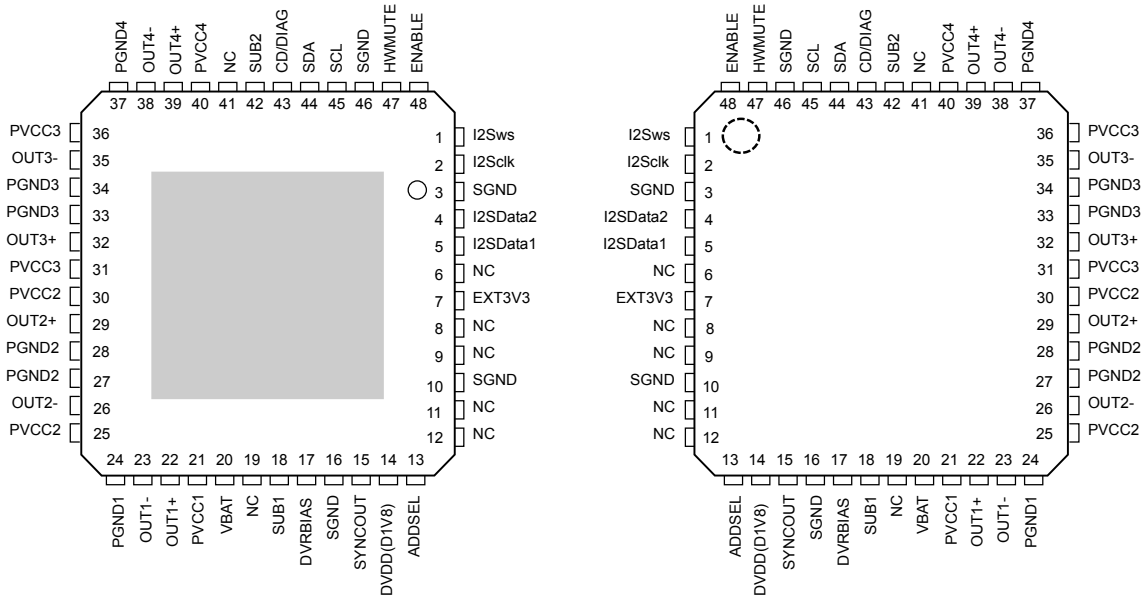


Table 1. Pins list description

#	Pin	Function	Definition	Internal structure
1	I2Sws	I2S/TDM sync input	Input	-
2	I2Sclk	I2S/TDM clock input	Input	-
3	SGND	Signal ground	Supply	-
4	I2SData2	I2S/TDM data input 2	Input	-
5	I2SData1	I2S/TDM data input 1	Input	-
6	NC	Not connected	-	-
7	EXT3V3	Auxiliary external 3.3 V supply	Supply	-
8	NC	Not connected	-	-
9	NC	Not connected	-	-
10	SGND	Signal ground	Supply	-
11	NC	Not connected	-	-
12	NC	Not connected	-	-
13	ADDSEL	Address selection	Input	-
14	DVDD(D1V8)	Digital power supply	Supply internal reference	-
15	SYNCOUT	Synchronization clock out	Output	Push-pull
16	SGND	Signal ground	Supply	-
17	DRVBIAS	Gate driver bias	Supply internal reference	-
18	SUB1	Die substrate pin	Supply	-
19	NC	Not connected	-	-
20	VBAT	Battery voltage pin	Supply	-
21	PVCC1	Channel 1, power supply	Supply	-
22	OUT1+	Channel 1, half-bridge plus, output	Output	-
23	OUT1-	Channel 1, half-bridge minus, output	Output	-
24	PGND1	Channel 1, power ground	Supply	-
25	PVCC2	Channel 2, power supply	Supply	-
26	OUT2-	Channel 2, half-bridge minus, output	Output	-
27	PGND2	Channel 2, power ground	Supply	-
28	PGND2	Channel 2, power ground	Supply	-
29	OUT2+	Channel 2, half-bridge plus, output	Output	-
30	PVCC2	Channel 2, power supply	Supply	-
31	PVCC3	Channel 3, power supply	Supply	-
32	OUT3+	Channel 3, half-bridge plus, output	Output	-
33	PGND3	Channel 3, power ground	Supply	-
34	PGND3	Channel 3, power ground	Supply	-
35	OUT3-	Channel 3, half-bridge minus, output	Output	-
36	PVCC3	Channel 3, power supply	Supply	-
37	PGND4	Channel 4, power ground	Supply	-
38	OUT4-	Channel 4, half-bridge minus, output	Output	-
39	OUT4+	Channel 4, half-bridge plus, output	Output	-
40	PVCC4	Channel 4, power supply	Supply	-

#	Pin	Function	Definition	Internal structure
41	NC	Not connected	-	-
42	SUB2	Die substrate pin	Supply	-
43	CD/DIAG	Clipping detector and diagnostic output	Output	Open-drain
44	SDA	I²C data	Input/Output	Open-drain
45	SCL	I²C clock	Input	-
46	SGND	Signal ground	Supply	-
47	HWMUTE	Hardware mute	Input	Internal pull-up
48	ENABLE	Enable	Input	-

1.1 Application diagram

Figure 3. Application diagram

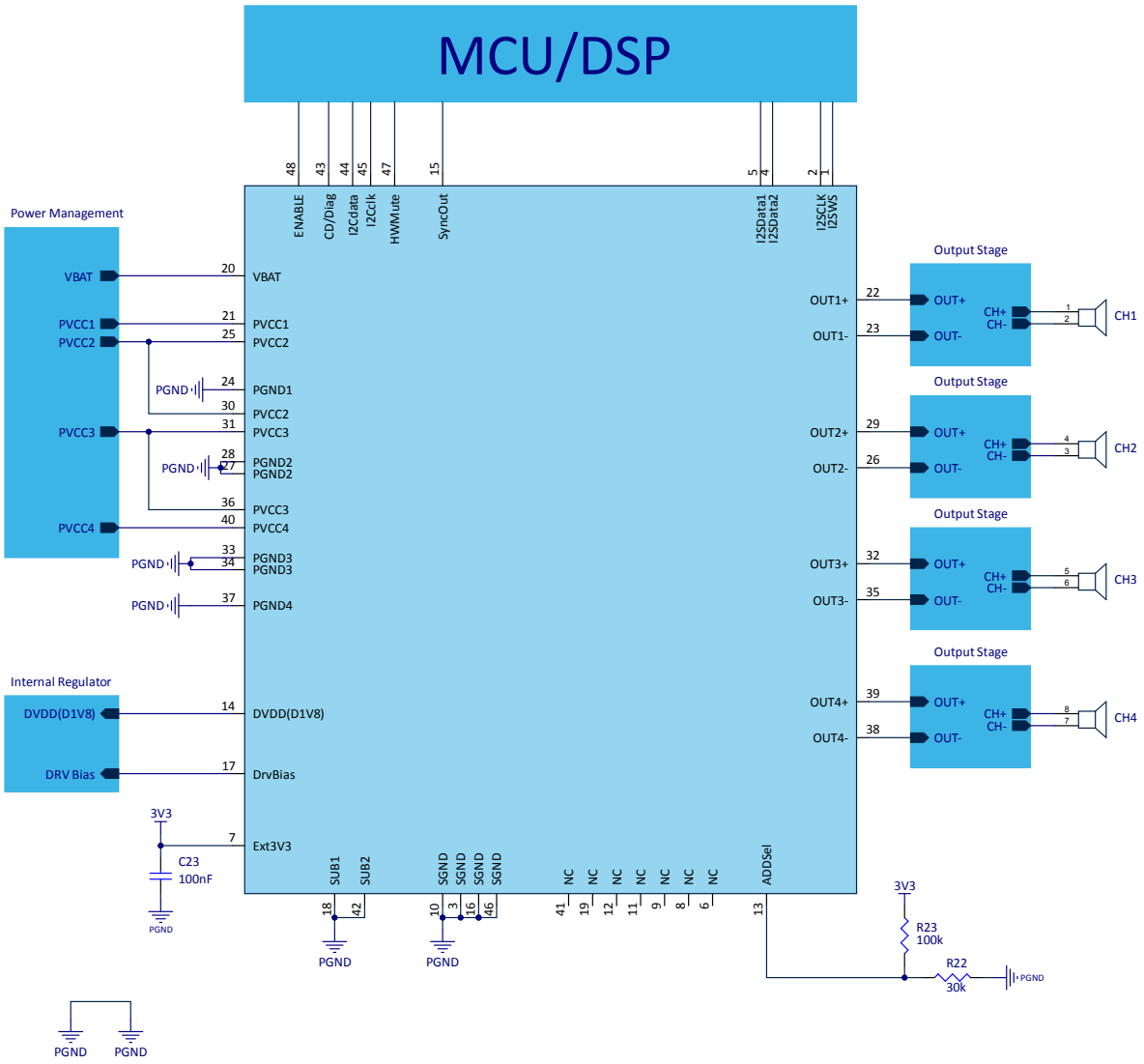
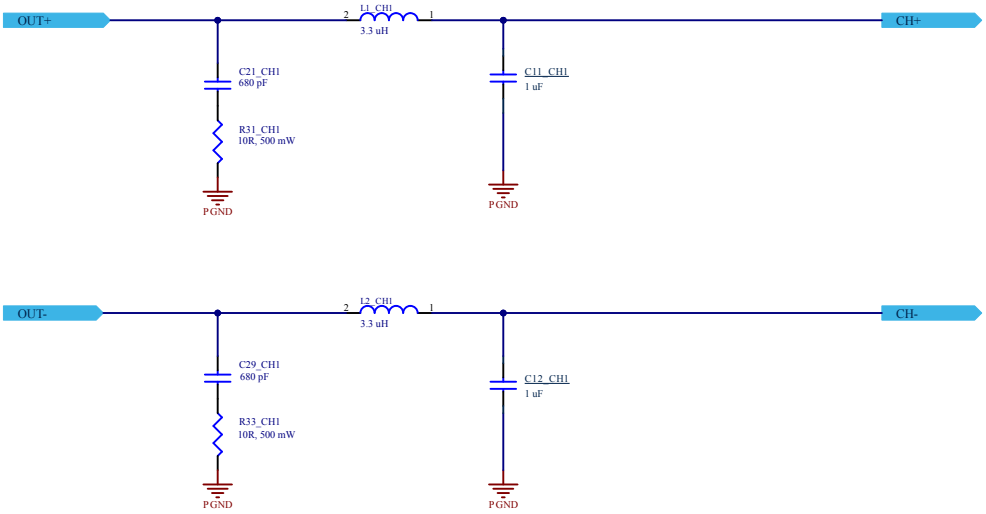


Figure 4. Output stage



Note: The Figure 4. Output stage reports the output stage filter of a channel as a reference. The others follow the same configuration. The snubber network (C21_CH1, C29_CH1, R31_CH1 e R33_CH1) must be necessarily connected to the master channels for the parallel configurations (channel 1 for the case where channel 1 and channel 2 work in parallel, channel 3 for the case where channel 3 and channel 4 work in parallel).

Figure 5. Power supply filter

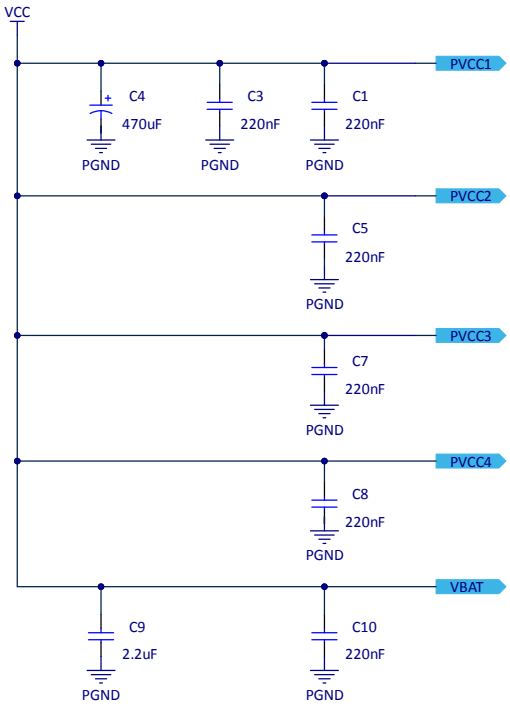


Figure 6. Internal regulator

2 Electrical specifications

2.1 Absolute maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CCmax}	DC supply pins [VBAT, PVCC(x)]	-0.3 to 40	V
$OUT_{(x)}{}^{+}$, $OUT_{(x)}{}^{-}$	Output ± pin	-0.3 to 25	V
DRVBIAS	Gate driver bias pin(1)	-0.3 to 20	V
EXT3V3	Voltage on EXT3V3 pin	-0.3 to 4.6	V
$I2C_{data}$, $I2C_{clk}$	I²C bus pins [SDA, SCL]	-0.3 to 4.6	V
$I2S_{data1}$, $I2S_{data2}$, $I2S_{clk}$, $I2S_{ws}$	I²C bus pins [I2SData1, I2SData2, I2Sclk, I2Sws]	-0.3 to 4.6	V
SYNCOUT	Synchronization pin	-0.3 to 4.6	V
ADDSEL	Address selection pin	-0.3 to 4.6	V
ENABLE	Enable pin	-0.3 to 4.6	V
CD/DIAG	Clipping detector and diagnostic pin	-0.3 to 4.6	V
HWMUTE	Hardware mute pin	-0.3 to 4.6	V
DVDD(D1V8)	Digital power supply pin(1)	-0.3 to 2.5	V
GND_{max}	Voltage difference between ground pins [SGND, $PGND_{(x)}$, $SUB_{(x)}$]	-0.3 to 0.3	V
T_A	Ambient operating temperature	-40 to 125	°C
T_{stg}, T_J	Storage and junction temperature	-55 to 150	°C
ESD_{HBM}	ESD protection HBM (2)	2000	V
ESD_{CDM}	ESD protection CDM standard (2)	500	V
	ESD protection CDM corner (2)	750	V

1. *Internal circuit output pin: not to be controlled externally.*
2. *Definition according to the international standard.*

2.2 Maximum operating voltage

Table 3. Maximum operating voltage

Symbol	Parameter	Value	Unit
EXT3V3	EXT3V3 pin voltage supply	3.3 + 5%	V
$I2C_{data}$, $I2C_{clk}$	I²C bus pins voltage [SDA, SCL]	EXT3V3	V
$I2S_{data1}$, $I2S_{data2}$, $I2S_{clk}$, $I2S_{ws}$	I²C bus pins [I2SData1, I2SData2, I2Sclk, I2Sws]	EXT3V3	V
SYNCOUT	Synchronization pin voltage	EXT3V3	V
ADDSEL	Address selection pin voltage	EXT3V3	V
ENABLE	Enable pin voltage	EXT3V3	V
CD/DIAG	CD/DIAG pin voltage	EXT3V3	V
HWMUTE	Hardware mute voltage	EXT3V3	V

2.3 Thermal data

Table 4. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case (1)	2.05	°C/W

1. *By simulation with top cold plate as per JEDEC best practice guidelines (JESD51) in contact with package top side (e-pad). Ambient temperature set to 85 °C.*

3 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

3.1 LQFP48L (7x7x1.4 mm exp. pad up) package information

Figure 7. LQFP48L (7x7x1.4 mm exp. pad up) package outline

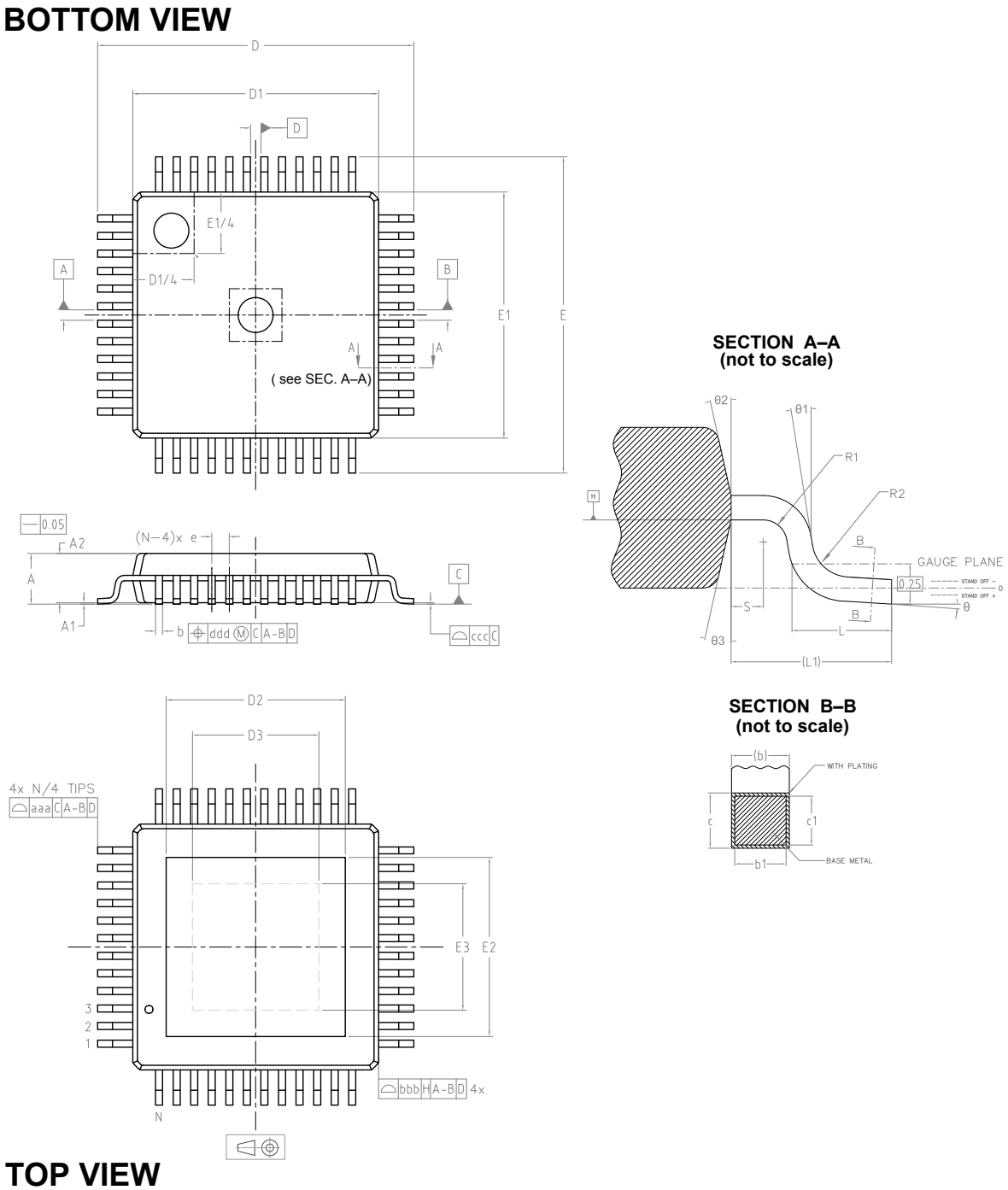


Table 5. **LQFP48L (7x7x1.4 mm exp. pad up) package mechanical data**

Symbol	Dimensions in mm		
	Min.	Typ.	Max.
Θ	0°	3.5°	7°
Θ1	0°	-	-
Θ2	10°	12°	14°
Θ3	10°	12°	14°
A	-	-	1.49
A1	-0.03	-	0.05
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
b1	0.17	0.20	0.23
c	0.09	-	0.20
c1	0.09	-	0.16
D	9.00 BSC		
D1	7.00 BSC		
D2	-	-	5.60
D3	3.90	-	-
e	0.50 BSC		
E	9.00 BSC		
E1	7.00 BSC		
E2	-	-	5.60
E3	3.90	-	-
L	0.45	0.60	0.75
L1	1.00 REF		
N	48		
R1	0.08	-	-
R2	0.08	-	0.20
S	0.20	-	-
Tolerance of form and position			
aaa	0.20		
bbb	0.20		
ccc	0.08		
ddd	0.08		

Revision history

Table 6. **Document revision history**

Date	Revision	Changes
19-Jan-2026	1	Initial release.

Contents

List of tables

List of figures

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