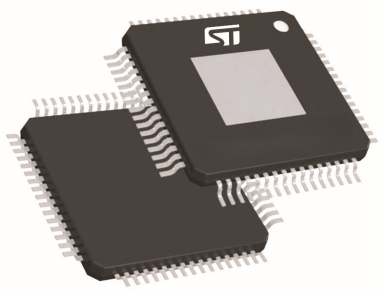
FDA902HP

Data brief

2-channel 40 V class-D digital input automotive power amplifier with diagnostics features and low voltage



LQFP64
(exposed pad up)

Product status link
FDA902HP

Product summary		
Order code	**Package**	**Packing**
FDA902HP-VYY	LQFP64 (exp. pad up)	Tray
FDA902HP-VYT		Tape and reel

Features

- AEC-Q100 qualified
- Integrated 110 dB D/A conversion
- I²S and TDM digital input (3.3/1.8 V)
- Input sampling frequency: 44.1 kHz, 48 kHz, 96 kHz, 192 kHz
- Full I²C bus driving (3.3/1.8 V) with 8 different I²C bus addresses
- EMI control for FM/AM compatibility
- EMI compliance evaluated following normative CISPR25 (class V)
- Low radiation function (LRF)
- Very low quiescent current
- Output low-pass filter included in the feedback allowing outstanding audio performances
- Wide operating supply range: target 5.5 V–40 V
- Supply voltage monitoring on I²C
- 60 dB S/N load current monitor
- MOSFET power outputs able to deliver 10 A peak pulse
- MOSFET power outputs providing high output power capability under stepped up voltage:
  - 2 x 170 Wrms (typ.) on 4 Ω at 40 V, 1 kHz THD = 1%
- Operation under standard car battery with high output power:
  - 2 x 23 Wrms (typ.) on 4 Ω at 14.4 V, 1 kHz THD = 1%
  - 2 x 37 Wrms (typ.) on 2 Ω at 14.4 V, 1 kHz THD = 1%
- Possibility to drive 2 Ω loads on 2 channels up to 25 V:
  - 2 x 110 Wrms (typ.) on 2 Ω at 25.5 V, 1 kHz THD = 1%
- Parallel mode
  - 1 Ω up to 25.5 V
  - 2 Ω up to 40 V
- Independent channel operation
- I²C bus diagnostics:
  - Short to V_{CC}/GND diagnostics (including soft shorts up to 1 kΩ)
  - DC load diagnostics
  - AC load diagnostics
- Digital impedance-meter (DIM)
- Integrated fault protection
- Input and output offset detector
- Clipping detector
- Legacy mode ('no I²C' mode)
- Short circuit and ESD integrated protections
- Package: LQFP64 exposed pad up

Description

The FDA902HP is a dual bridge class-D amplifier, designed in the most advanced BCD technology expressly intended for car radio applications.

The FDA902HP integrates a high performance D/A converter together with powerful MOSFET outputs in class-D, to get an outstanding efficiency compared to the standard class AB amplifiers.

Thanks to the high-voltage MOSFET output stages it can operate both under standard car battery (6–18 V) and under boosted power supplies (up to 40 V) to deliver the highest possible power with an integrated solution.

The feedback loop includes the output LC low-pass filter, allowing superior frequency response linearity and lower distortion independently from the inductor and quality of the inductors and capacitors.

The FDA902HP is fully configurable through I²C bus interface and integrates a complete diagnostics array especially intended for automotive applications.

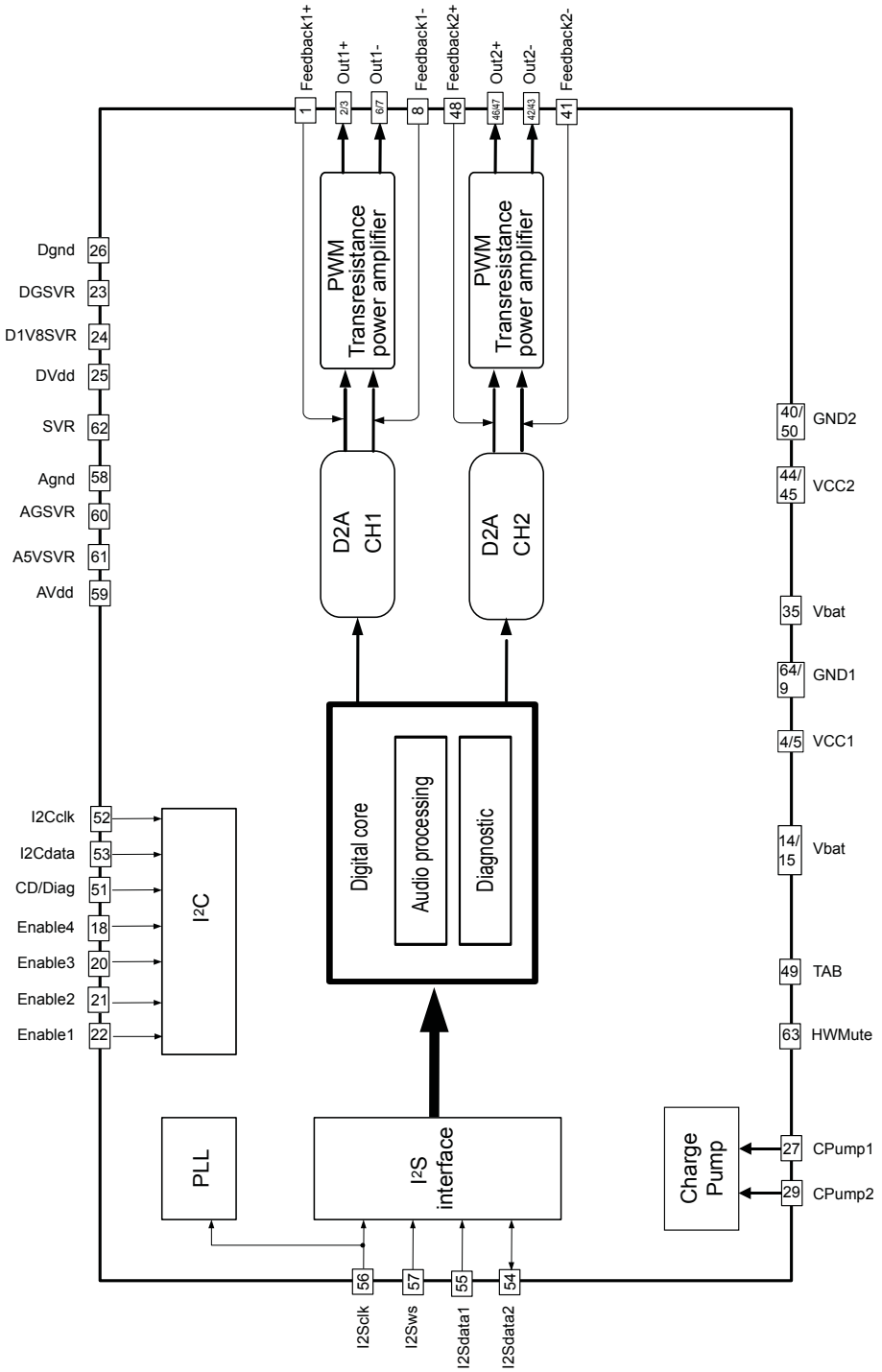
Thanks to the solutions implemented to solve EMI problems, the device is intended to be used in a standard single DIN car-radio enclosure, even when equipped with a tuner.

Moreover, FDA902HP is able to operate with a power supply as low as 5.5 V, thus supporting the most recent low voltage levels specified by car-makers (for example, for 'start-stop' compatibility).

1 Block diagram and pins description

1.1 Block diagram

Figure 1. **Block diagram**



1.2 Pins description

Figure 2. **Pins connection diagram**

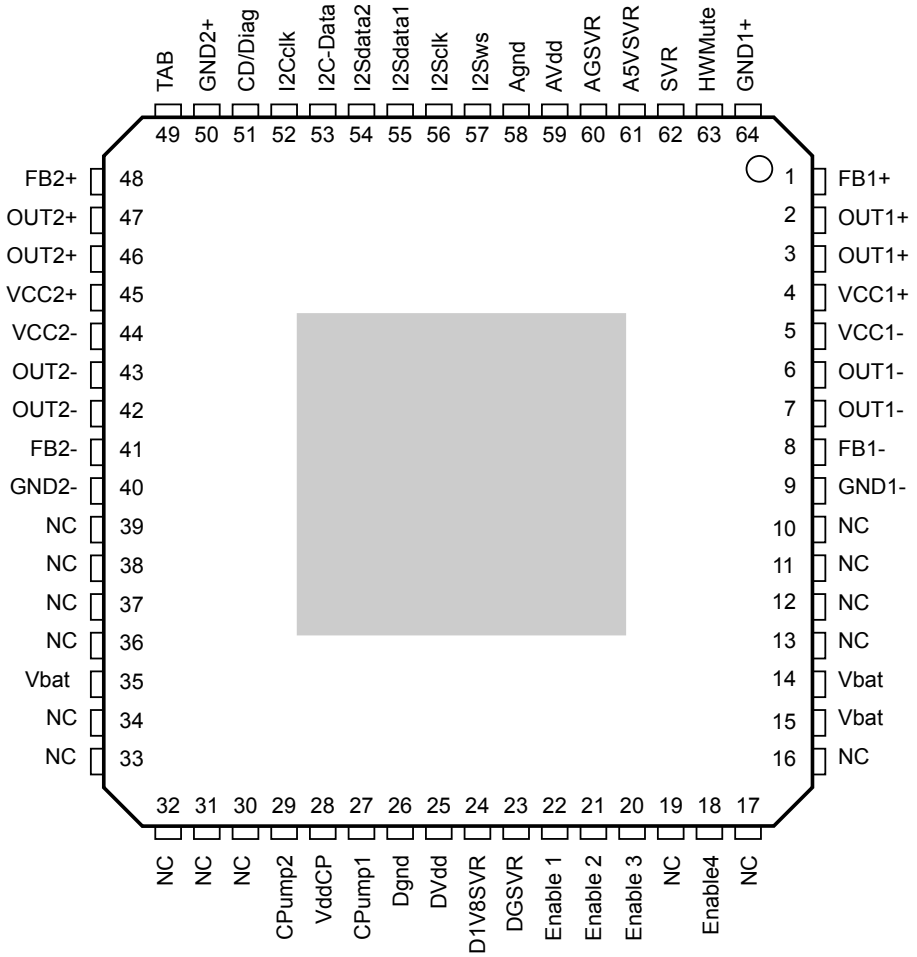


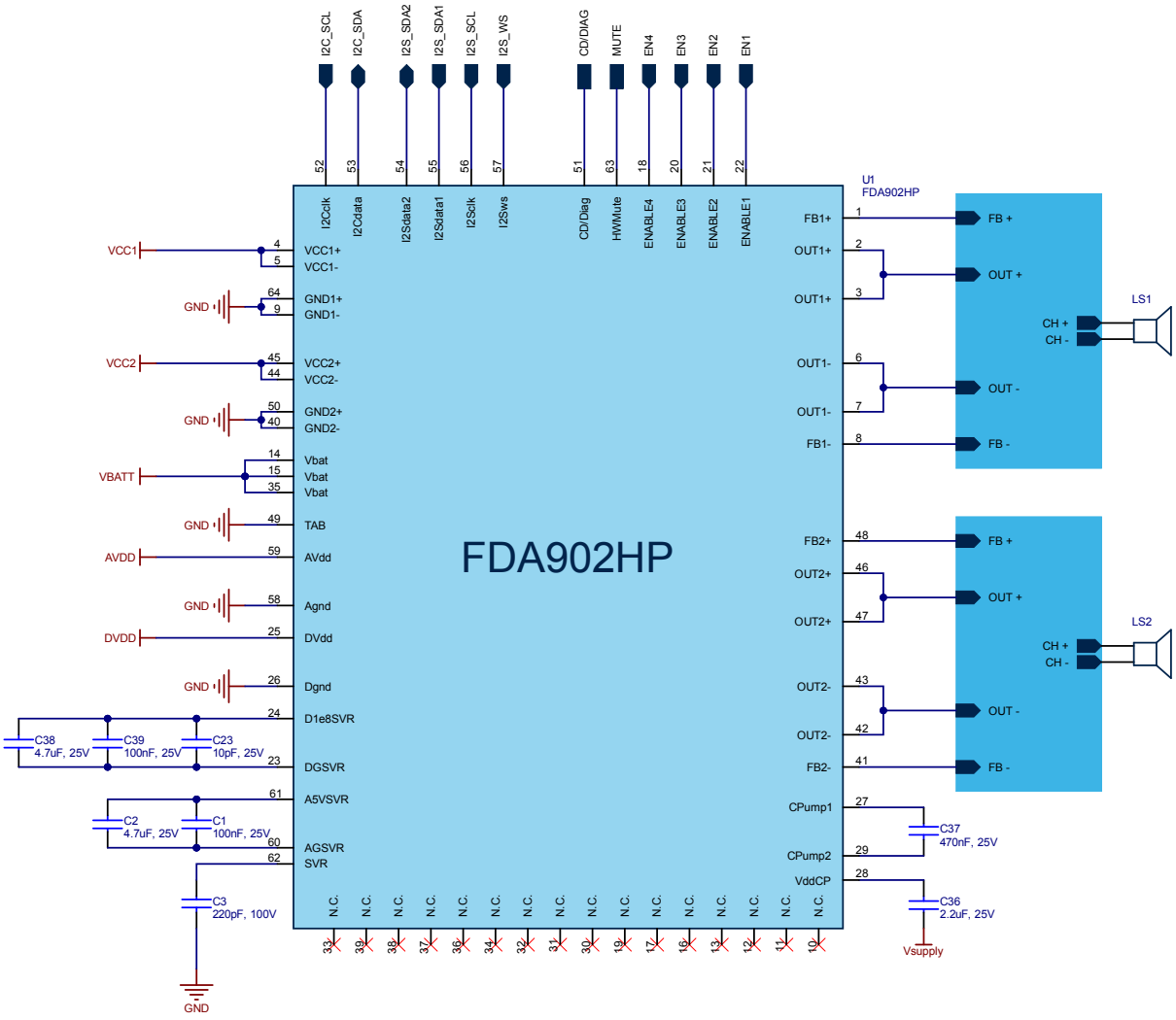
Table 1. **Pins list description**

N#	Pin	Function
1	FB1+	Channel 1, half bridge plus, feedback
2	OUT1+	Channel 1, half bridge plus, output
3	OUT1+	Channel 1, half bridge plus, output
4	VCC1+	Channel 1, half bridge plus, boosted power supply
5	VCC1-	Channel 1, half bridge minus, boosted power supply
6	OUT1-	Channel 1, half bridge minus, output
7	OUT1-	Channel 1, half bridge minus, output
8	FB1-	Channel 1, half bridge minus, feedback
9	GND1-	Channel 1, half bridge minus, power ground
10-13	N.C.	Not connected
14	Vbat	Main battery voltage
15	Vbat	Main battery voltage
16-17	N.C.	Not connected
18	Enable4	Chip enable 4

N#	Pin	Function
19	N.C.	Not connected
20	Enable3	Chip enable 3
21	Enable2	Chip enable 2
22	Enable1	Chip enable 1
23	DGSVR	Negative analog supply V(SVR) - 0.9 V (internally generated)
24	D1V8SVR	Positive digital supply V(SVR) + 0.9 V (internally generated)
25	DVdd	Digital supply
26	Dgnd	Digital ground
27	CPump1	Charge pump pin1
28	VddCP	Charge pump output voltage
29	CPump2	Charge pump pin2
30-34	N.C.	Not connected
35	Vbat	Main battery voltage
36-39	N.C.	Not connected
40	GND2-	Channel 2, half bridge minus, power ground
41	FB2-	Channel 2, half bridge minus, feedback
42	OUT2-	Channel 2, half bridge minus, output
43	OUT2-	Channel 2, half bridge minus, output
44	VCC2-	Channel 2, half bridge minus, boosted power supply
45	VCC2+	Channel 2, half bridge plus, boosted power supply
46	OUT2+	Channel 2, half bridge plus, output
47	OUT2+	Channel 2, half bridge plus, output
48	FB2+	Channel 2, half bridge plus, feedback
49	TAB	Device slug connection
50	GND2+	Channel 2, half bridge plus, power ground
51	CD/Diag	Clip detector / diagnostic pin (output, open drain)
52	I2CClk	I²C clock
53	I2C-Data	I²C data input
54	I²Sdata2	I²S/TDM data 2 (data input, NOT used in TDM mode)
55	I²Sdata1	I²S/TDM data 1(data input)
56	I²Sclk	I²S/TDM clock
57	I²Sws	I²S/TDM ws (frame sync input)
58	Agnd	Analog ground
59	AVdd	Analog supply
60	AGSVR	Negative analog supply V(SVR) - 2.5 V (internally generated)
61	A5VSVR	Positive analog supply V(SVR) + 2.5 V (internally generated)
62	SVR	Supply voltage ripple rejection capacitor
63	HWMute	Hardware mute pin
64	GND1+	Channel 1, half bridge plus, power ground

2 Application diagram

Figure 3. **Application diagram**



The figure here below is referred to the channel 2, but the same external components are also used for the channel 1.

Figure 4. Output stage

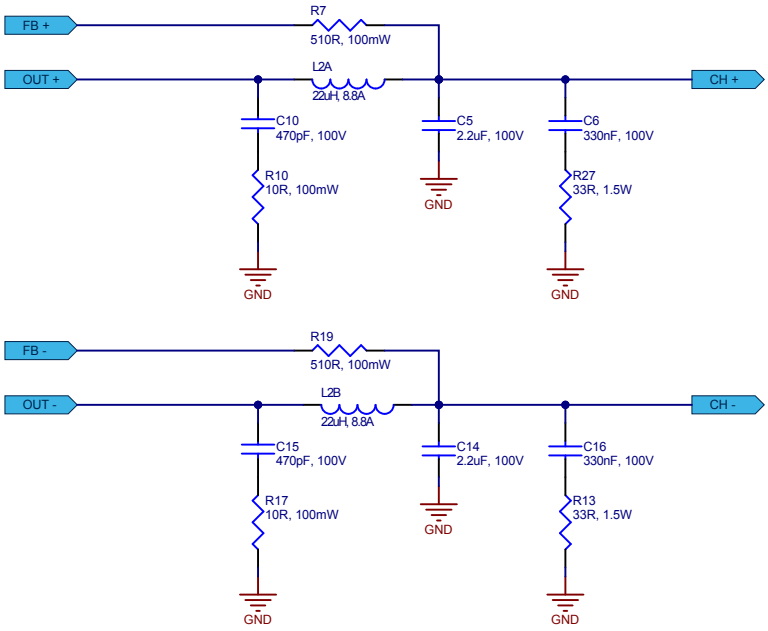
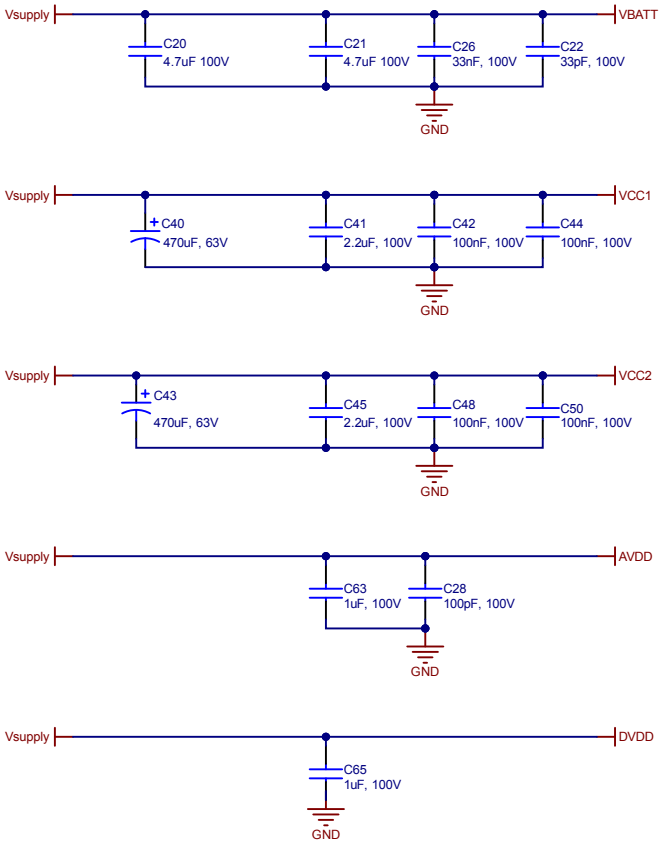


Figure 5. Power supply filter



3 Electrical specifications

3.1 Absolute maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
VCC_{max} [VCC1+, VCC1-, VCC2+, VCC2-, AVdd, DVdd, V_{bat}]	DC supply voltage	-0.3 to 50(1)	V
	Transient supply voltage (for t = 50 ms) not operating ramp time ≥ 2 ms	57	V
GND_{max} [GND1+, GND1-, GND2+, GND2-, Agnd, Dgnd]	Ground pin voltage difference	-0.3 to 0.3	V
V_{i2c} [I2Cdata, I2Cclk]	I²C bus pins voltage	-0.3 to 5.5	V
V_{i2s} [I2Sclk, I2Sws, I2Sdata1, I2Sdata2]	I²S bus pins voltage	-0.3 to 5.5	V
V_{enable} [Enable1, Enable2, Enable3, Enable4]	Enable pins voltage	-0.3 to 5.5	V
V_{CD} [CD/Diag]	CD/DIAG pin	-0.3 to 5.5	V
Vmute [HWmute]	Hardware mute pin voltage	-0.3 to 5.5	V
I_O	Output current (repetitive f > 10 Hz)	Internally limited	A
T_{stg}, T_J	Storage and junction temperature	-55 to 150	°C
T_A	Ambient temperature	-40 to 105	°C
ESDHBM	ESD protection HBM(2)	2000	V
ESDCDM	ESD protection CDM(2)	500	V

1. *Refer to the Load possibilities and operating range for I²C configuration of operating supply range.*
2. *Conforming to ESD international standard.*

3.2 Maximum operating voltage

Table 3. Maximum operating voltage

Symbol	Parameter	Typ.	Unit
VCC_{max} [VCC1+, VCC1-, VCC2+, VCC2-, AVdd, DVdd, V_{bat}]	DC supply voltage	40	V
VI2C [I2Cdata, I2Cclk]	I²C bus pins voltage	3.6	V
VI2S [I2Sclk, I2Sws, I2Sdata1, I2Sdata2]	I²S bus pins voltage	3.6	V
Vmute [HWmute]	Hardware mute pin voltage	5.3	V
Enable [Enable1, Enable2, Enable3, Enable4]	Enable pins voltage	3.6	V
VCD [CD/Diag]	CD/DIAG pin voltage	3.6	V

3.3 Thermal data

Table 4. Thermal data

Symbol	Parameter	Typ.	Unit
R_{thJC}(1)	Thermal resistance, junction-to-case	1.15	°C/W

1. *Thermal resistance junction to top case as per standard Jedec JESD51-12.01 with package top side (e-pad side) in ideal contact with a cold plate (infinite heat sink like).*

4 General introduction

The FDA902HP is a fully digital single chip class-D amplifier with high immunity to the demodulation filter effects. The high integration level and the on-board signal processing allow excellent audio performance to be achieved.

Thanks to the digital input and to the feedback strategy in the power stage that makes the amplifier immune from the output filter components non-linearity, the number and size of the external components are minimized.

A number of features is included to reduce EMI and the fully digital approach provides a very high immunity to GSM/RF interferences.

The FDA902HP includes: digital I²C and I²S interfaces, internal 24 bits DAC conversion, digital signal processing for interpolation and noise shaping, innovative self-diagnostic functions and automatic detection of wrong load connections or load variations, internal PLL for clock generation.

5 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

5.1 LQFP64 (10x10x1.4 mm exp. pad up) package information

Figure 6. LQFP64 (10x10x1.4 mm exp. pad up) package outline

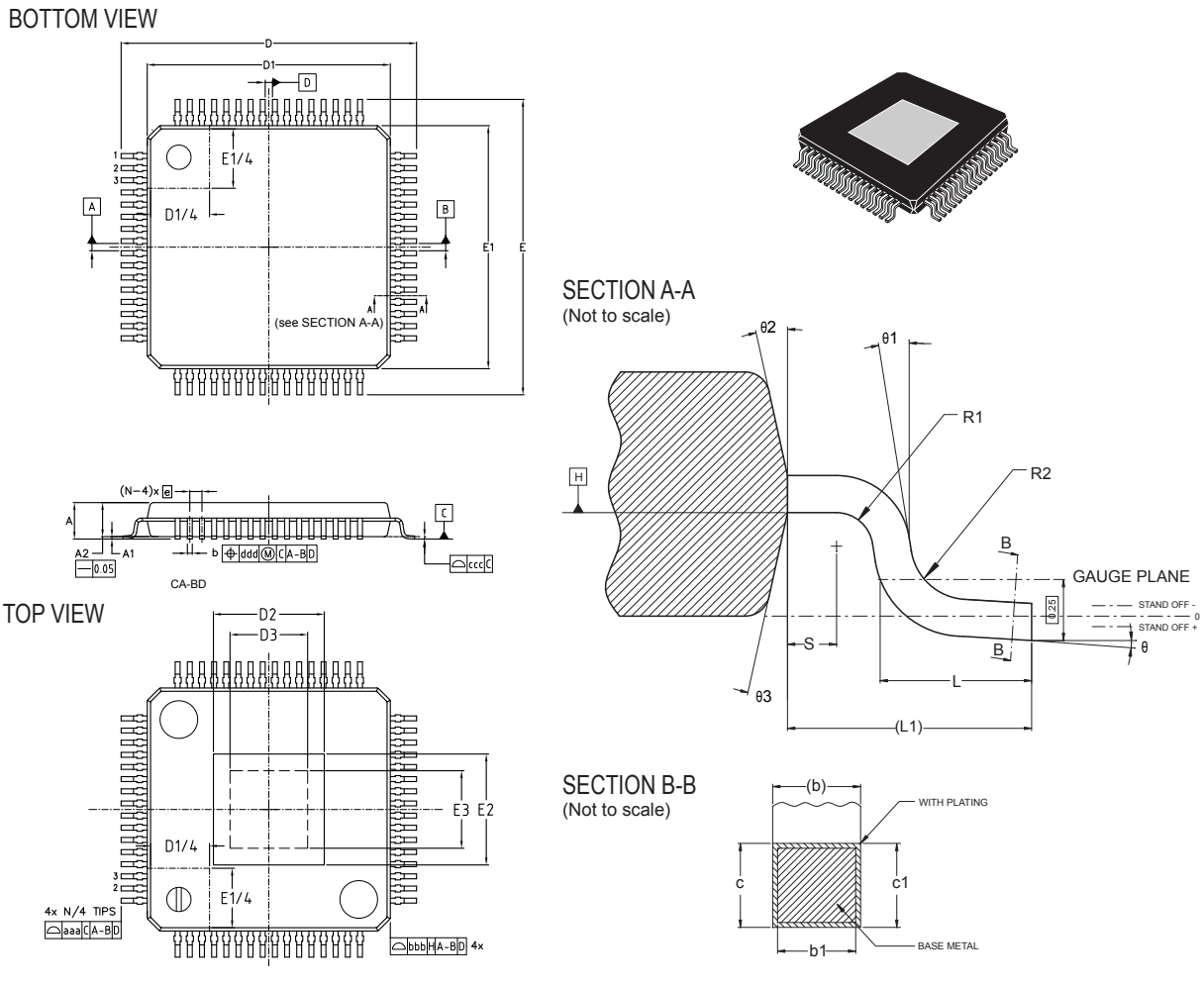


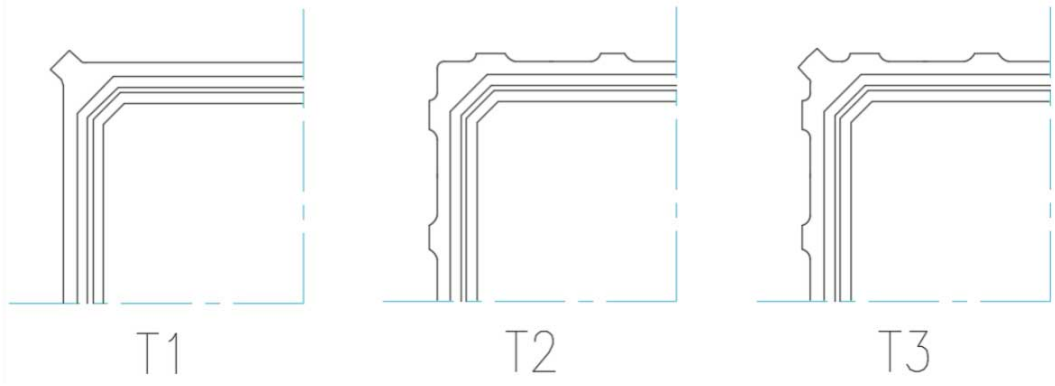
Table 5. LQFP64 (10x10x1.4 mm exp. pad up) package mechanical data

Symbol	Dimensions in mm		
	Min.	Typ.	Max.
Θ	0°	3.5°	6°
Θ1	0°	-	-
Θ2	10°	12°	14°
Θ3	10°	12°	14°
A	-	-	1.49
A1	-0.04	-	0.04
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
b1	0.17	0.20	0.23
c	0.09	-	0.20
c1	0.09	0.127	0.16
D	12.00 BSC		
D1(1)(2)	10.00 BSC		
D2	See VARIATIONS		
D3	See VARIATIONS		
e	0.50 BSC		
E	12.00 BSC		
E1(1)(2)	10.00 BSC		
E2	See VARIATIONS		
E3	See VARIATIONS		
L	0.45	0.60	0.75
L1	1.00 REF		
N	64		
R1	0.08	-	-
R2	0.08	-	0.20
S	0.20	-	-
Tolerance of form and position			
aaa	0.20		
bbb	0.20		
ccc	0.08		
ddd	0.08		
VARIATIONS			
Pad option 6.0x6.0 (T1-T3)(3)			
D2	-	-	6.61
E2	-	-	6.61
D3	4.8	-	-
E3	4.8	-	-

1. *Dimensions D1 and E1 do not include mold flash or protrusions. Allowable mold flash or protrusion is “0.25 mm” per side.*
2. *The Top package body size may be smaller than the bottom package size by much as 0.15 mm.*

3. *Number, dimensions and position of shown groves are for reference only (see the Figure 7).*

Figure 7. Groves diagram



Revision history

Table 6. **Document revision history**

Date	Revision	Changes
13-Jan-2026	1	Initial release.

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