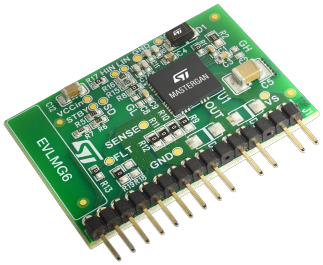
EVLMG6

Data brief

MASTERGAN6 power module for high efficiency Half-Bridge-GaN-based power supply applications



Features

- GaN half-bridge daughter board equipped with MASTERGAN6, suitable for power applications requiring fast wake up time.
- Comprehensive set of input control signals (LIN, HIN, SD, and STBY) with wide amplitude range to be connected to either analog controllers or micro-controllers.
- VCC directly connected to controller IC supply. No needed external voltage regulator to provide a proper supply and protections to GaN drivers.
- Discrete bootstrap diode and capacitor for high frequency solutions.
- Adjustable low side shunt to serve peak current mode control algorithms.
- External parallel body diodes to serve resonant application needs.
- 30 x 40 mm FR4 dual layer PCB with 40 °C/W junction to ambient thermal resistance.
- RoHS compliant.

MasterGaN

Product status link
EVLMG6

Description

The EVLMG6 is a GaN-based half-bridge power module equipped with MASTERGAN6, which quickly creates new topologies without needing a complete PCB design.

The module is shipped with available footprint locations for low side resistors (set to zero) and for two external body diodes (not mounted), connected in parallel to each half-bridge GaN.

The module can be easily configured to operate with many resonant and hard switching topologies.

The VCC supply can be derived directly from the application IC controller. On-board bootstrap diode supplies the high side VBOOT voltage and ensures extremely quick high side section activation. MASTERGAN6 has two internal LDO that quickly generate the optimal 6V supply for the two high side and low side GaN drivers.

The module accepts separate driving signals having an amplitude range between 3 V and 16V independently from VCC level.

The EVLMG6 is a 30 x 42 mm wide FR-4 PCB, resulting in an $R_{th(J-A)}$ of approximately 40 °C/W, without forced airflow.

1 Board pin description

Figure 1 shows the pin connections of the power module: the connector map is reported and summarized in Table 1.

Pins 1 to 8 are dedicated to the half-bridge terminals of each drain-source GaN.

In a typical application, an external supply coming from the motherboard should be connected to the VDD pin.

LIN and HIN (pins 11 and 12) receive the driving signals that come from the controller. Amplitude of PWM signals can be in range of 3 V to 20 V (max) independently from VDD voltage.

SENSE (pin 13) provides the low side current signal: it can be connected, for example, to a peak current mode controller to define the switching-on time of the low side GaN. When this feature is used, sense resistors (R9 to R12) must be sized properly. In fact, the board is sold with 0 Ω resistors.

SD/STBY (pin 9) could be used, alternatively, to get MASTERGAN6 in low consumption (STBY connection, default connection - R18 = removed, R19 = 0 Ω) or to disable outputs asynchronously than LIN and HIN (SD connection - R18 = 0 Ω, R19 = removed).

FLT pin is an open drain output for fault reporting. In default connection, FLT is unused and shorted to GND: to activate this feature, remove R13.

Figure 1. EVLMG6– Supply and signal connection

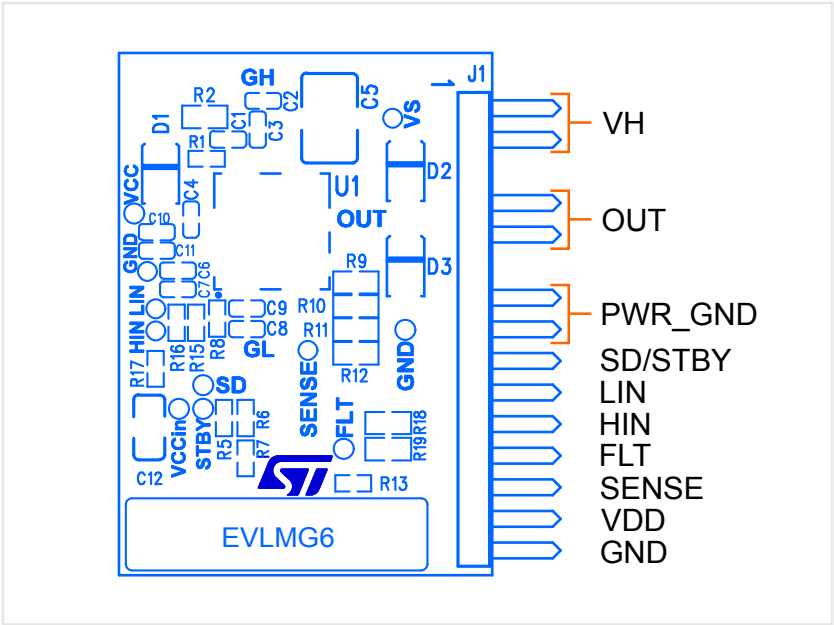


Table 1. Connector Map

Ref.	Pin #	Name	Function	Description
J1	1, 2	VH	INPUT power	These two pins are connected to the VS pins of MASTERGAN6: connect high voltage potential to this pin according to MASTERGAN6 recommended values (520 V).
	4, 5	OUT	OUT power	These two pins are connected to the OUT pins of MASTERGAN6: connect the load to this terminal (e.g. resonant tanks, transformers, etc.).
	7, 8	PWR_GND	POWER GND	These two pins are the reference voltage of power components (POWER GND).
	9	SD/STBY	Standby state activation or Disable	According to selected configuration for R18 and R19, an external signal it can used to

Ref.	Pin #	Name	Function	Description
J1				• Activate low consumption Mode (default) • Disable the device (alternate board configuration) Thanks to on-board pull-up, the pin can be left floating when unused
	10	LIN	INPUT	Direct connection to the LIN of the MASTERGAN6 pins. LIN input range: up to 20 V.
	11	HIN	INPUT	Direct connection to the HIN of the MASTERGAN6 pins. HIN input range: up to 20 V.
	12	FLT	FAULT	Open drain output for fault recording (disabled when board is sold)
	13	SENSE	INPUT	This pin is connected to the SENSE pins of MASTERGAN6: the board is configured with shorted sense resistors (R9, R10, R11 and R12) for LLC topology. As necessary, a peak current mode loop can be sensed here.
	14	VDD	INPUT power	It is the MASTERGAN6 supply voltage input (10 V to 18 V).
	15	GND	POWER GND	Daughter board reference potential.

2 Schematics diagram

Figure 2 shows the schematics of the MASTERGAN6 power module.

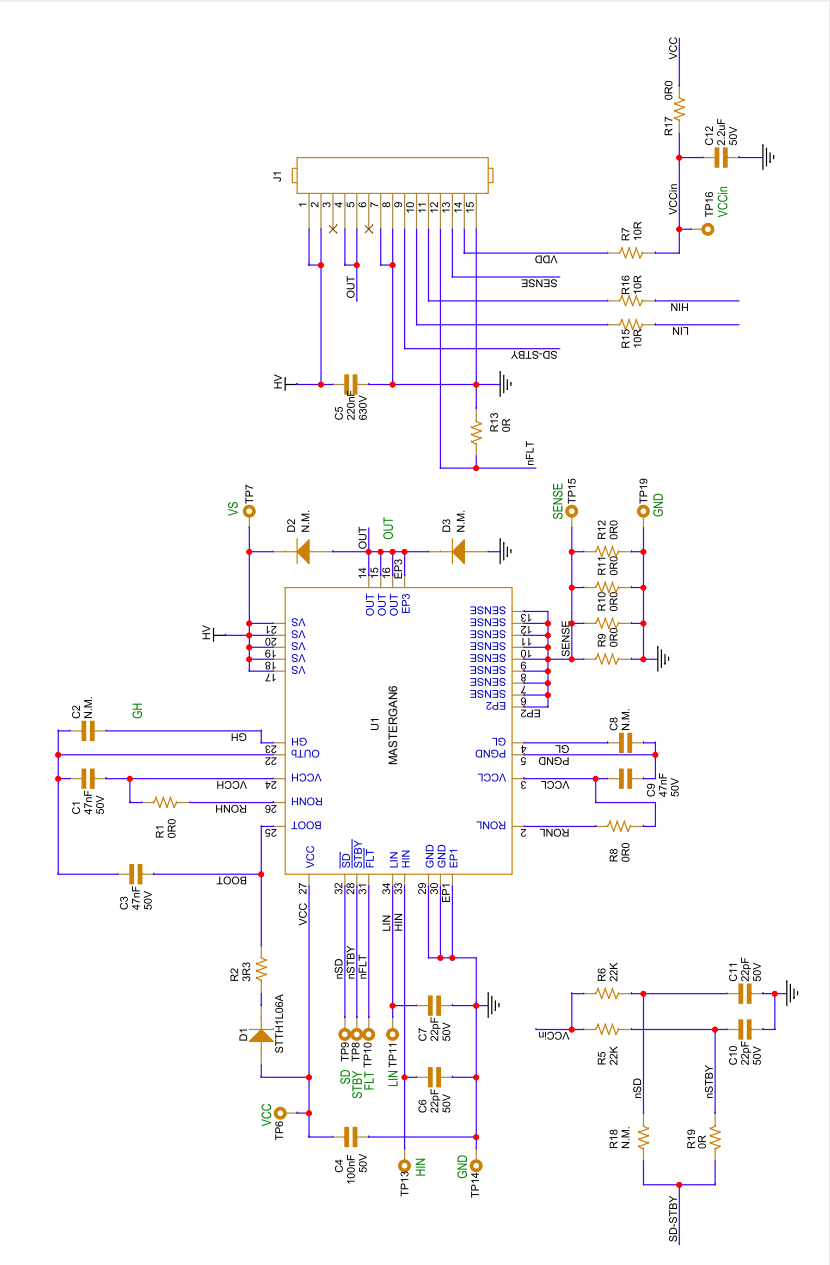
An input supply coming from the motherboard is applied to VDD. Bootstrap diode (D1) provides voltage to BOOT pin while the MASTERGAN6 internal regulators ensures a perfect driving voltage to GaN Transistors (VCCL and VCCH).

R15 and C7, R16 and C6 is used filter undesired glitches and can be exploited to introduce an adjustable delay to input LIN and HIN driving signals.

R1 and R8 can be modified to adjust the steepness of rising or fall edge of OUT pin during turn on.

The STBY pin can be used to activate low consumption mode, while the SD pin can be used as an enable/disable pin for special algorithms or protection implementation. R18 and R19 can be used to activate one or both functions.

Figure 2. EVLMG6– schematic – High density power driver



3 Special setting configurations

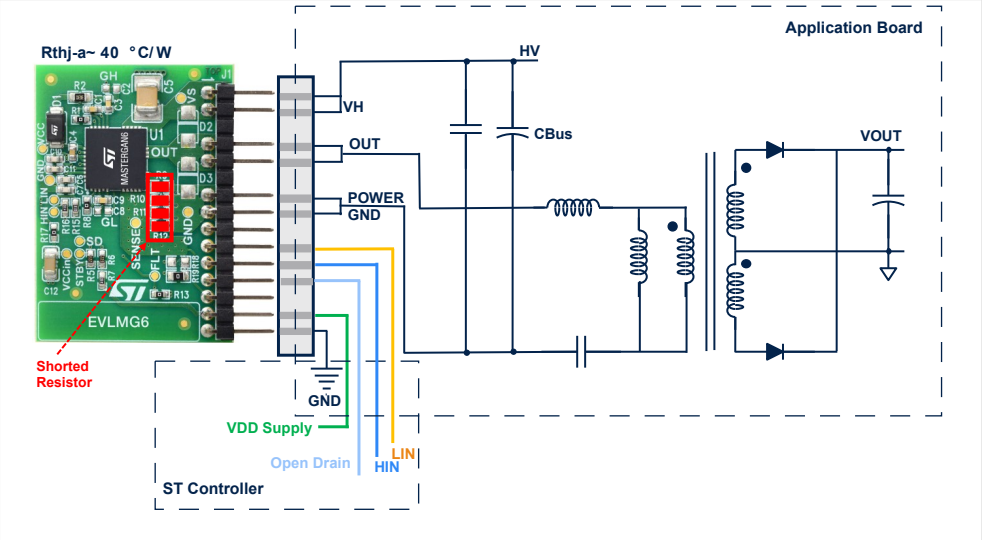
The following paragraph describes, graphically, some of the applications where EVLMG6 can be used. Some possible modifications are described to help designers to fit their own application.

3.1 LLC applications

EVLMG6 is ready to be used in LLC applications.

Figure 3 shows how to connect EVLMG6 to a resonant LLC motherboard with a dedicated STMicroelectronics IC controller .

Figure 3. EVLMG6 – Typical Resonant LLC application



Usually, LLC topologies do not sense the resonant current on low side source connection, therefore R9, R10, R11, and R12 are set to 0 Ω to directly connect low side source GaN to power GND.

Body diodes D6 and D7 (STTH1R06) could be mounted in parallel to each high side and low side GaN to optimize efficiency minimizing the voltage drop during dead times, when reverse conduction occurs. These components could be omitted if controller embeds adaptive dead times feature .

MASTERGAN6 guarantees a very fast wake up time of high side driver after first LIN generation: this ensures a correct very high burst mode efficiency.

An example of the LLC design can be found in the AN5644 - EVLMG1-250 W LLC demo board .

3.2 Flyback applications

A half-bridge is also used in active clamp or resonant flyback applications. Figure 4 and Figure 5 show how to connect the EVLMG6 respectively to an active clamp flyback and a resonant flyback.

For these applications, sense resistors R9, R10, R11, and R12 must be sized properly, depending on the output final target power .

The SENSE pin is connected to the controller to close the peak current mode loop.

The use of one or both external body diodes D6 and D7 (STTH1R06) has to be evaluated case by case.

Figure 4. **EVLMG6 – Typical ACF Flyback application**

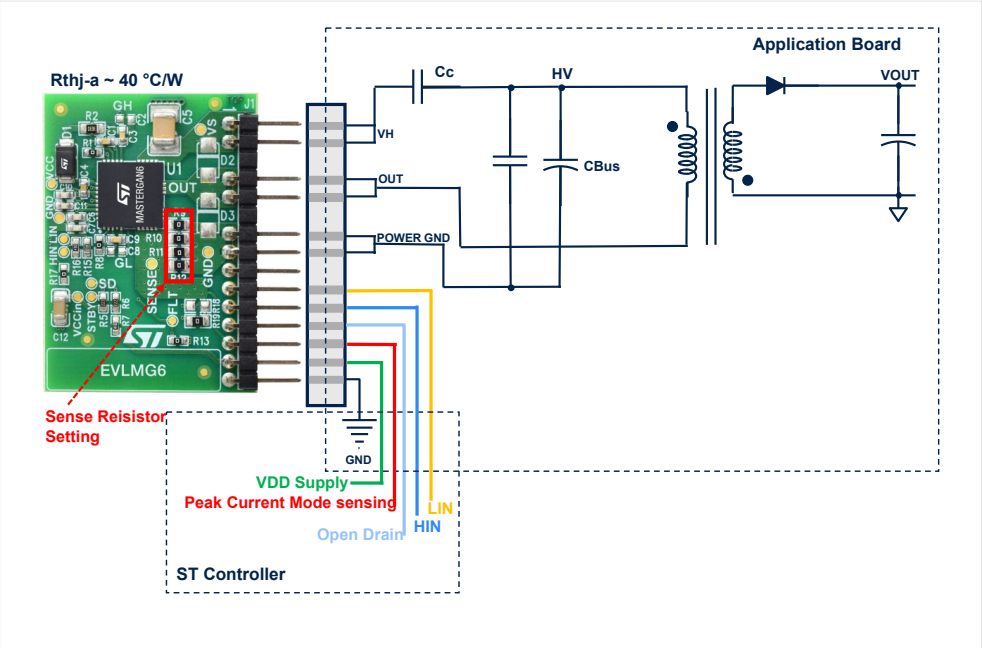
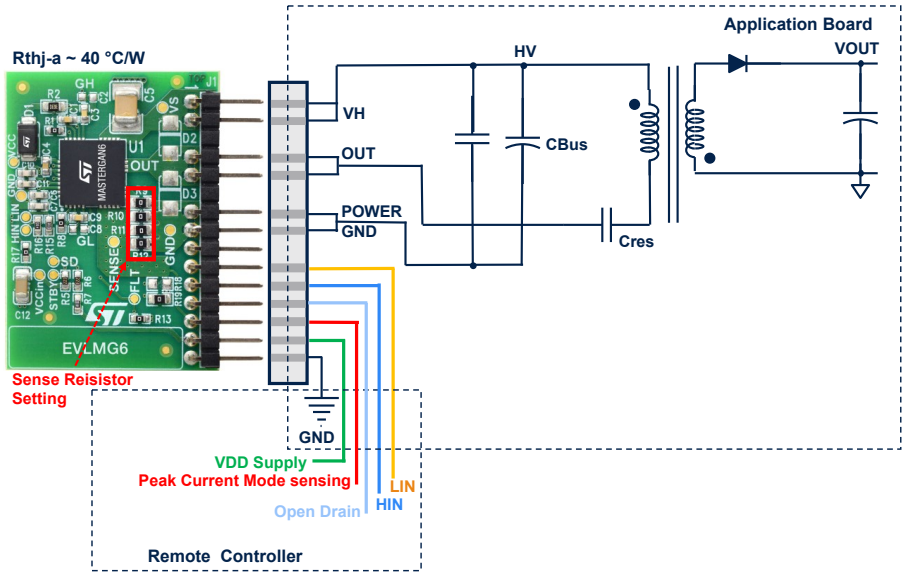


Figure 5. **EVLMG6 – Typical Resonant Flyback application**



3.3 Synchronous inverse buck

A half-bridge can be used in synchronous buck applications configured as either inverted or traditional.

Figure 6 shows how to connect the EVLMG6 to a non-isolated inverse buck in which the switching element and diode are replaced by the MASTERGAN6.

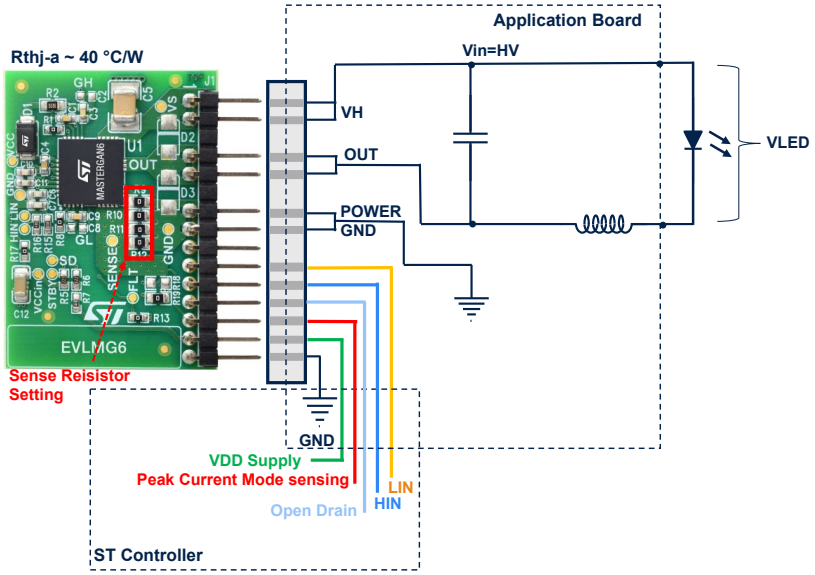
For these applications sense resistors R9, R10, R11, and R12 must be sized properly depending on the output's final target power.

In reference , a dimmable GaN based LED driver has been designed to provide up to 500 W with an applied input voltage of 400 V and an output 1.2 A LED string voltage range between 150 V and 350 V.

In that configuration, the SENSE pin is connected to the controller to close the peak current mode loop, while external body diodes D6 and D7 are not needed.

Embedded linear regulators ensure safe operation during all phases of either DCM or CCM control algorithm.

Figure 6. EVLMG6 – Synchronous Inverse Buck application



4 Architecture and component placement

The EVLMG6 is a 30 x 40 mm wide, 1.6mm thich, dual layer (2oz.) FR-4 PCB, resulting in an $R_{th(J-A)}$ of 40 °C/W, without forced airflow .

Component placement and PCB layout of both top and bottom sides are depicted in the following pictures Figure 7 and Figure 8.

Figure 7. EVLMG6 – top and bottom component placement

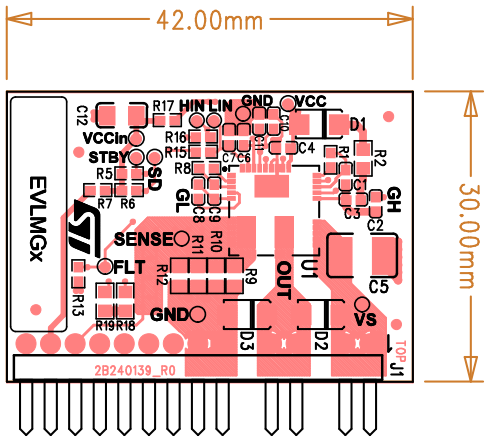
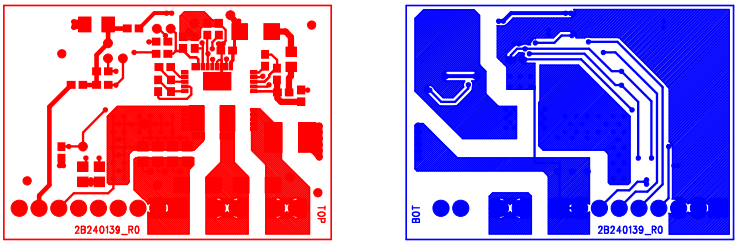


Figure 8. EVLMG6 – top and bottom PCB layout



5 Bill of material

Table 2. **Bill of material**

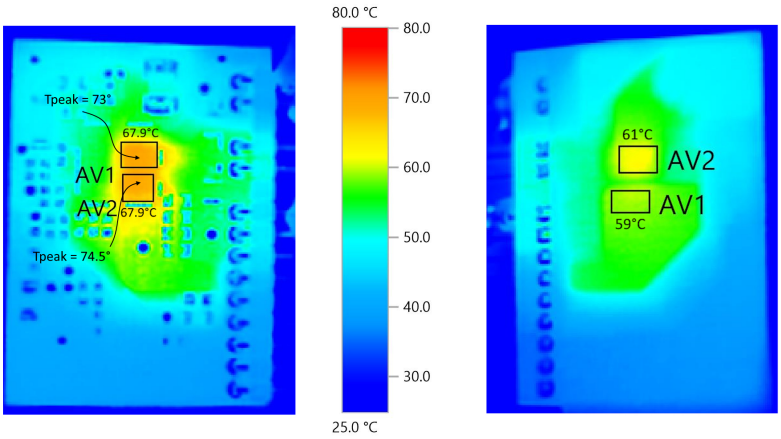
Ref.	Value	Package	Description	Supplier
C1	47nF	0603	SMD CERCAP. General Purpose 50V, +/-10%	
C2	N.M.	0603	SMD CERCAP. General Purpose 50V, +/-10%	
C3	47nF	0603	SMD CERCAP. General Purpose 50V, +/-10%	
C4	100nF	0603	SMD CERCAP. General Purpose 50V, +/-10%	
C5	220nF	1812	SMD CERCAP. General Purpose 630V, +/-10% Soft Termination	
C6	22pF	0603	SMD CERCAP. General Purpose 50V, +/-10%	
C7	22pF	0603	SMD CERCAP. General Purpose 50V, +/-10%	TDK
C8	N.M.	0603	SMD CERCAP. General Purpose 50V, +/-20%	
C9	47nF	0603	SMD CERCAP. General Purpose 50V, +/-10%	
C10	22pF	0603	SMD CERCAP. General Purpose 50V, +/-10%	
C11	22pF	0603	SMD CERCAP. General Purpose 50V, +/-10%	
C12	2.2µF	1206	SMD CERCAP. General Purpose 50V, +/-10%	
D1	STTH1L06A	SMA	SMD Rectifier 600V, 1A	STMicroelectronics
D2	N.M.	SMA		
D3	N.M.	SMA		
J1	HEADER 15		Single Row Right Angle PCB Header 15 ways	Wurth code: 61304011021
R1	0R0	0603	SMD Resistor 1/10W, 1%	
R2	3R3	0805	SMD Resistor 1/8W, 1%	
R5	22K	0603	SMD Resistor, 1/10W, 1%	
R6	22K	0603	SMD Resistor, 1/10W, 1%	
R7	10R	0603	SMD Resistor 1/10W, 1%	
R8	0R0	0603	SMD Resistor 1/10W, 1%	
R9	0R0	0805	SMD Resistor 1/8W, 1%	
R10	0R0	0805	SMD Resistor 1/8W, 1%	
R11	0R0	0805	SMD Resistor 1/8W, 1%	
R12	0R0	0805	SMD Resistor 1/8W, 1%	
R13	0R0	0603	SMD Resistor 1/10W, 1%	
R15	10R	0603	SMD Resistor 1/10W, 1%	
R16	10R	0603	SMD Resistor 1/10W, 1%	
R17	0R0	0603	SMD Resistor 1/10W, 1%	
R18	N.M.	0603		
R19	0R0	0805	SMD Resistor 1/8W, 1%	
U3	MASTERGAN6	QFN 9x9x1mm	600V half-bridge enhancement mode GaN HEMT with high voltage driver	STMicroelectronics

6 Thermal Performance

The thermal performance of EVLMG6 are evaluated in terms of overall thermal resistance and equals 40 °C/W. The evaluation is based on measurements made on temperature increase exhibited by MASTERGAN6 when the overall GaN dice power dissipation equals 1 Watt.

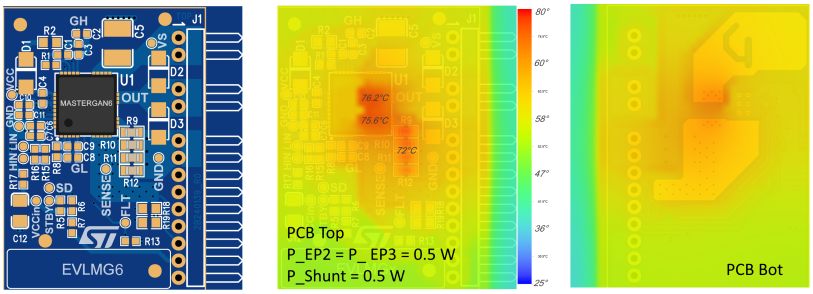
In asymmetrical topologies, the GaNs dissipate uneven power. The thermal resistance of low side and high side transistors are well balanced and can be considered equal to $Rth_{j(LS),amb}$ = $Rth_{j(HS),amb}$ = 80 °C/W.

Figure 9. EVLMG6 Thermal Maps



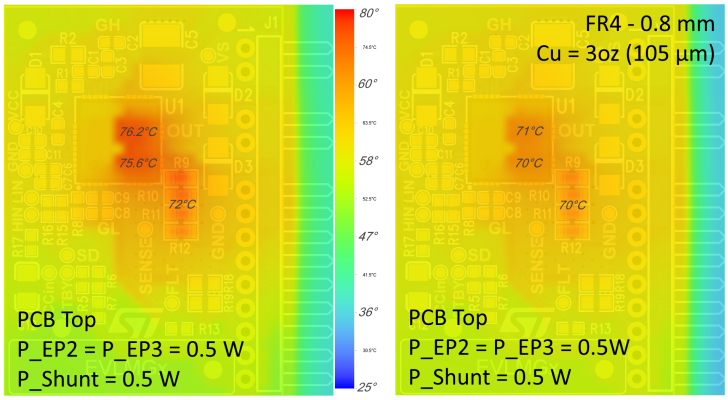
EVLMG6 and MASTERGAN6 Thermal model is included into PCB Thermal Simulator. This tool can be used to perform comprehensive analysis: for example, it helps to estimate the absolute temperature of each component mounted on the board.

Figure 10. EVLMG6 PCB Thermal Simulator results



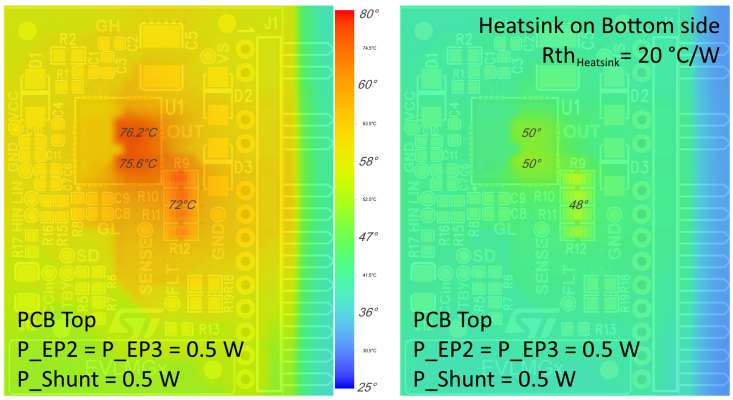
The impact of PCB thickness or copper thickness can be evaluated as well adjusting relevant parameters into the tool.

Figure 11. PCB Thermal Simulator - results with different PCB stackups



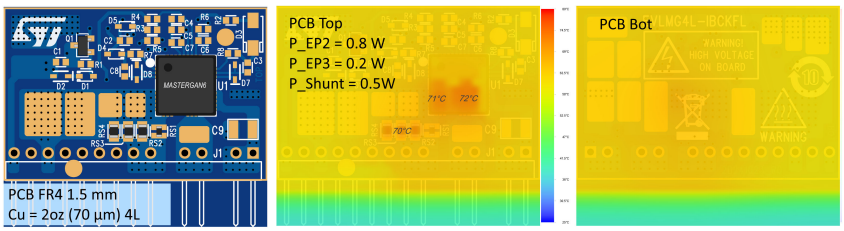
A heatsink on top or bottom side of the board can be added into simulation to anticipate the right size of this component prior to connect to the board.

Figure 12. PCB Thermal Simulator - results using heatsink on EVLMG6



Finally, a simulation of a user defined board can be set up form scratch starting form the board's Gerber file and the MASTERGAN6 thermal model that is selectable from tool's library.

Figure 13. PCB Thermal Simulator - results using MASTERGN6 on custom PCB layout



7 References

[1]
MASTERGAN6: “650 V GaN Half Bridge with high-voltage driver and protections” datasheet on www.st.com
[2]
PCB Thermal simulator (see eds.st.com/eds-console/#/electrical-simulator/pcb)
[3]
AN5917: “PCB design optimization for maximizing thermal dissipation in MasterGaN family” on www.st.com

Revision history

Table 3. **Document revision history**

Date	Version	Changes
13-Oct-2025	1	Initial release.

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