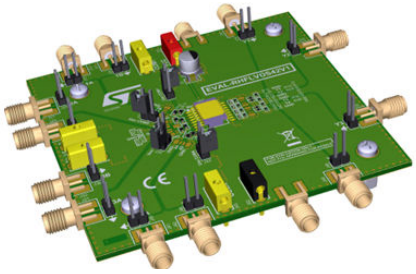
EVAL-RHFLVDS42

Data brief

Evaluation board for the RHFLVDS42



Maturity status link
EVAL-RHFLVDS42

Features

- Mounted RHFLVDS42 Engineering Model: Rad-hard, 600 Msps, LVDS driver
  - See RHFLVDS42 datasheet for further information
- Mounted components (ready-to-use)
- Material: 4-layered FR-4
- PCB thickness: 1.6 mm
- Copper thickness: 35 µm
- I/O Connectors: SMA , SIP 2.54 mm
- Power supply connections: banana 2 mm and SIP 2.54 mm
- Footprints for probes and CMS components
- Double ground layer which demonstrated the best performance
- Decoupling capacitive network close to the ICs to prevent noise on power supplies
- Numerous test points

Description

The EVAL-RHFLVDS42 evaluation board is a ready-to-use, configurable hardware, which allows designers to efficiently test the RHFLVDS42, a radiation-hardened LVDS driver.

This document describes the components included on the EVAL-RHFLVDS42 evaluation board and recommends several ways to use the board.

The EVAL-RHFLVDS42 evaluation board is intended for evaluation purposes only.

1 Device pin connection and description

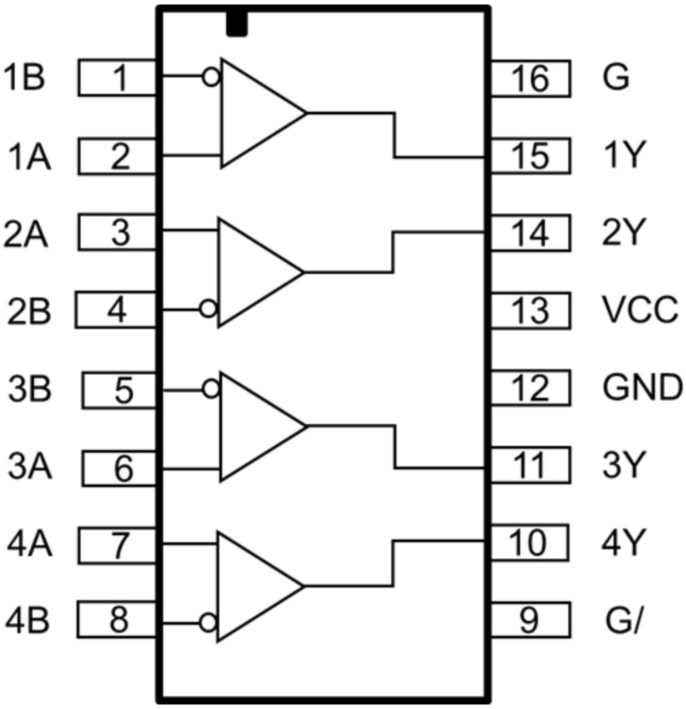


Figure 1. **RHFLVDS42 pin connections**

Table 1. **RHFLVDS42 pin description**

Pin number	Symbol	Name and function
2, 3, 6, 7	1A to 4A	Receiver inputs
1, 4, 5, 8	1B to 4B	Negated receiver inputs
15, 14, 11, 10	1Y to 4Y	Receiver outputs
16	G	Enable/Disable inputs
9	G/	
13	GND	Ground
12	VCC	Supply voltage

2 Evaluation board schematic

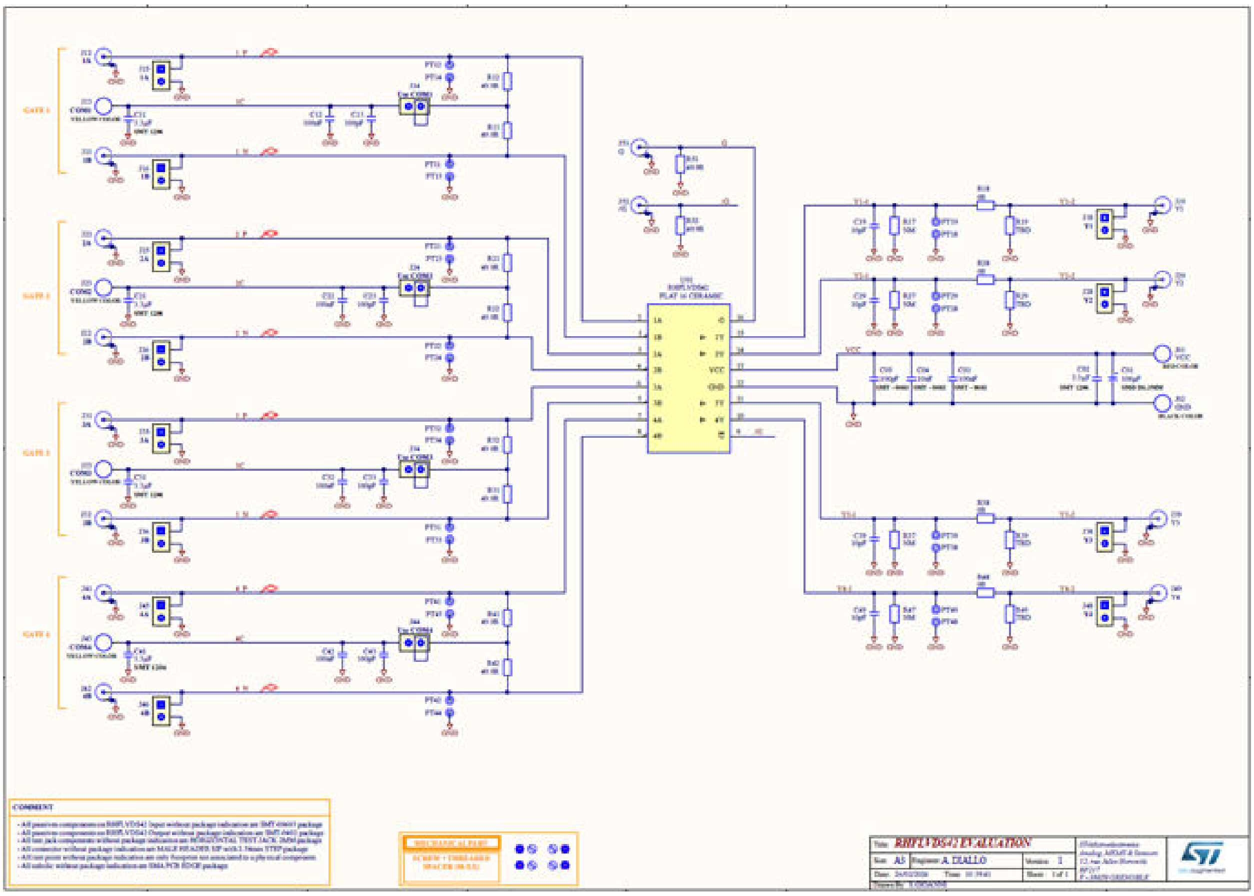


Figure 2. EVAL-RHFLVDS42V1 evaluation board schematic

3 PCB print out

To allow high-bandwidth signal measurements, the PCB is a four-layered FR-4 material with a thickness of 1.6 mm. The external copper thickness is 45 µm. The PCB tracks of the LVCMOS outputs are adapted to a 50 Ω impedance, while the LVDS differential pair inputs are adapted to a 100 Ω impedance. The following figures (Figure 3 to Figure 8) show the different layers of the EVAL-RHFLVDS42V1 PCB board.

Figure 3. **Top layer**

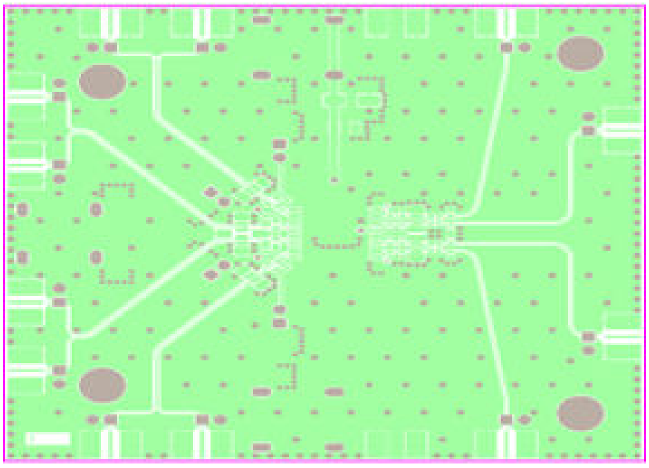


Figure 4. **Top overlay**

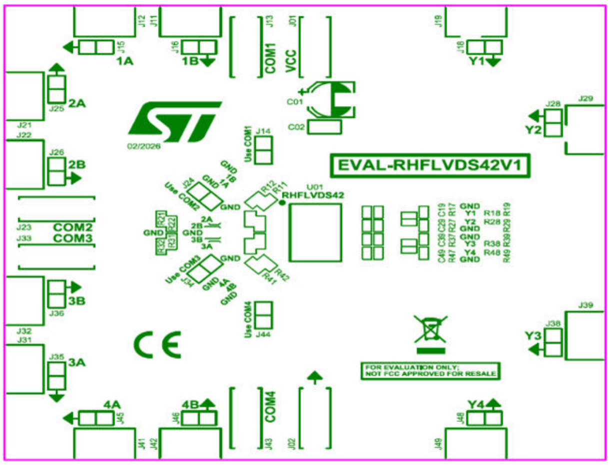


Figure 5. **Bottom layer**

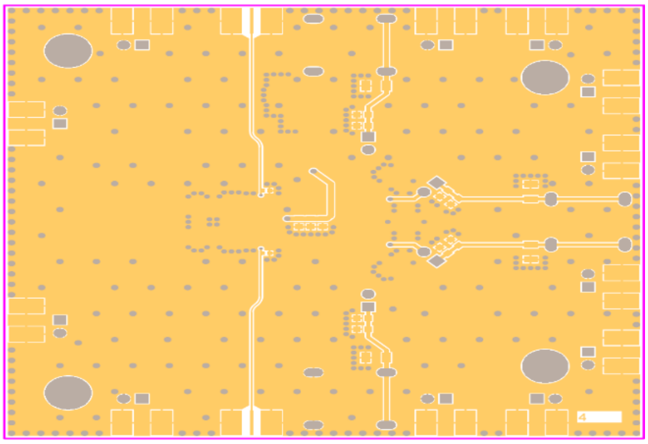


Figure 6. **Bottom overlay**

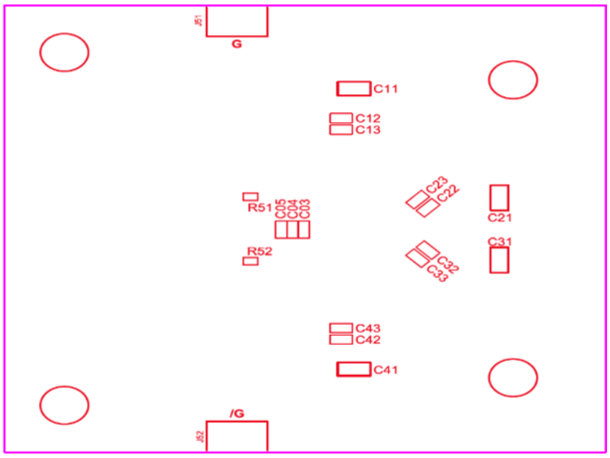


Figure 7. **Internal layer N° 2**

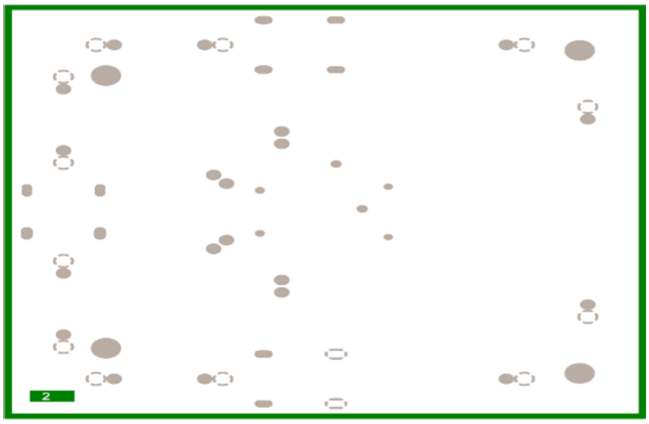
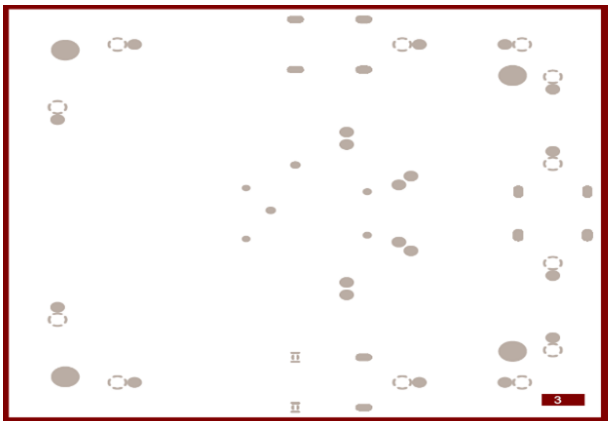


Figure 8. **Internal layer N° 3**



4 Bill of materials

Table 2. **Bill of materials**

Quantity	Reference	Value	Package/Footprint	Manufacturer	Manufacturer's Part Number
1	C01	100 µF	SMD D6.3MM	WURTH ELEKTRONIK	865060445005
5	C02, C11, C21, C31, C41	3.3 µF	SMT 1206	WURTH ELEKTRONIK	885012208067
5	C03, C12, C22, C32, C42	100 nF	SMT - 0603	WURTH ELEKTRONIK	885012206095
1	C04	10 nF	SMT - 0603	WURTH ELEKTRONIK	885012206089
5	C05, C13, C23, C33, C43	100 pF	SMT - 0603	WURTH ELEKTRONIK	885012206077
4	C19, C29, C39, C49	10 pF	SMT - 0402	WURTH ELEKTRONIK	885012005055
1	J01	RED COLOR	HORIZONTAL TEST JACK 2MM	JOHNSON - CINCH CONNECTIVITY	105-0752-001
1	J02	BLACK COLOR	HORIZONTAL TEST JACK 2MM	JOHNSON - CINCH CONNECTIVITY	105-0753-001
14	J11, J12, J19, J21, J22, J29, J31, J32, J39, J41, J42, J49, J51, J52	SUBCLIC	SMA PCB EDGE MOUNT	RF SOLUTIONS	CON-SMA-EDGE-S
4	J13, J23, J33, J43	YELLOW COLOR	HORIZONTAL TEST JACK 2MM	JOHNSON - CINCH CONNECTIVITY	105-0757-001
16	J14, J15, J16, J18, J24, J25, J26, J28, J34, J35, J36, J38, J44, J45, J46, J48	SIP 1x2 MALE	SIP 1X2 STEP 2.54MM	WURTH ELEKTRONIC	61300211121
4	JU14, JU24, JU34, JU44	BLACK COLOR	STEP 2.54 MM	WURTH ELEKTRONIK	609002115121
4	M-01, M-02, M-03, M-04	10MM	HOLE M3	WURTH ELEKTRONIK	970100321
4	M-05, M-06, M-07, M-08	6MM	HOLE M3	ETTINGER	81.58.322
0	R11, R12, R21, R22, R31, R32, R41, R42	49.9R	SMT - 0603	WURTH ELEKTRONIK	560112116133
0	R17, R27, R37, R47	NM	SMT - 0402		
4	R18, R28, R38, R48	0R	SMT - 0402	WURTH ELEKTRONIK	560112110001
0	R19, R29, R39, R49	TBD	SMT - 0402	WURTH ELEKTRONIK	560112110021
0	R51, R52	49.9R	SMT - 0402	WURTH ELEKTRONIK	560112110002
1	U01	RHFLVDS42	FLAT 16 CERAMIC	STMICROELECTRONICS	RHFLVDS42

5 Evaluation board description

5.1 Power supply

The power supply VCC connectors are banana 2 mm and 1x2 SIP male types.

Typical power supply voltages are as follows: V_{CC} = 2.3 V to 2.7 V and V_{CC} = 3 V to 3.6 V.

To prevent noise on the power supply VCC, a 100 µF electrolytic capacitor and a 3 µF ceramic capacitor are placed near the VCC connector, at the board edge.

Three additional bypass capacitors (ceramics) of 100 nF, 10 nF and 100 pF are placed close to the RHFLVDS42 device VCC pin.

5.2 Receiver enable and disable pins

When the connectors J51 and J52 are left open, RHFLVDS42 is enabled by default.

When using an external generator with a 50 Ω source impedance, R51 and R52 resistors are set to a 50 Ω value for impedance adaptation.

5.3 LVDS receiver inputs

The 4 LVDS differential input pairs (1A/1B, 2A/2B, 3A/3B, 4A/4B) have different connectors:

- J15/J16 , J25/J26, J35/J36 and J45/J46 (1x2 SIP male) are dedicated for the LVDS inputs driven directly, or for test points. For example, these connectors can be uses for signal probing with active probes.
- The high-bandwidth SMA connectors, J11/J12 , J21/J22, J31/J32, and J41/J42 are dedicated for the LVDS inputs driven directly by an external generator or from another LVDS driver such as the LVDS41 (see Figure 9).
- The banana connectors J13 , J32, J33 and J43 can be used for an external common-mode voltage application. Then, the jumpers J14/J54/J34/J44 must be closed.
- The 100 Ω termination resistor, a sum of two 50 Ω resistors (R11 , R12 , R21, R22, R31, R32, R41, R42) are placed by default at the LVDS inputs. They can be removed if not needed.
- Test point footprint for high-bandwidth probe tips soldering are also available (PT11/PT12 , PT21/PT22 ,PT31/PT32 , PT41/PT42). Differential probe tips can also be soldered in differential mode to directly probe the receiver differential input voltage signal VID = VA-VB.

5.4 LVCMOS receiver outputs

There are different test points at the LVCMOS outputs.

- For medium-frequency signal probing (up to 200 Mbps), the LVDS signals can be observed at test points J18, J28, J38, and J48 with active probes.
- For a high-speed signal probing up to 600 Mbps, it is advised to use a high bandwidth probes tips soldered at PT19 to PT49 test points. Then, the 0Ω serial resistor, R12, R18, R28, R38 and R48 must be removed to reduce reflections on the measured signal.
- The SMA connectors J19, J29, J39 and J49 can be used to observe a high-bandwidth signal at the scope 50 Ω input.
- Load capacitors of 10 pF (C11, C12, C21, C22, C31, C32, C41, and C42) are placed at the LVDS outputs. Of course, the user can adapt this value to their application.
- Other load resistor footprints are also available.

Figure 9. Typical LVDS receiver/receiver system schematic

Revision history

Table 3. **Document revision history**

Date	Revision	Changes
23-Jun-2026	1	Initial release.

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