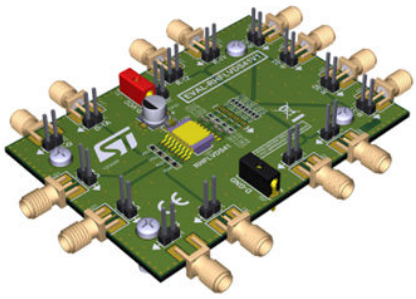
EVAL-RHFLVDS41

Data brief

Evaluation board for the RHFLVDS41



Maturity status link
EVAL-RHFLVDS41

Features

- Mounted RHFLVDS41 Engineering Model: Rad-hard, 600 Msps, LVDS driver
  - See RHFLVDS41 datasheet for further information
- Mounted components (ready-to-use)
- Material: 4-layered FR-4
- PCB thickness: 1.6 mm
- Copper thickness: 35 µm
- I/O Connectors: SMA, SIP 2.54 mm
- Power supply connections: banana 2 mm and SIP 2.54 mm
- Footprints for probes and CMS components
- Double ground layer which demonstrated the best performance
- Decoupling capacitive network close to the ICs to prevent noise on power supplies
- Numerous test points

Description

The EVAL-RHFLVDS41 evaluation board is a ready-to-use, configurable hardware, which allows designers to efficiently test the RHFLVDS41, a radiation-hardened LVDS driver.

This document describes the components included on the EVAL-RHFLVDS41 evaluation board and recommends several ways to use the board.

The EVAL-RHFLVDS41 evaluation board is intended for evaluation purposes only.

1 Device pin connection and description

Figure 1. **RHFLVDS41 pin connections**

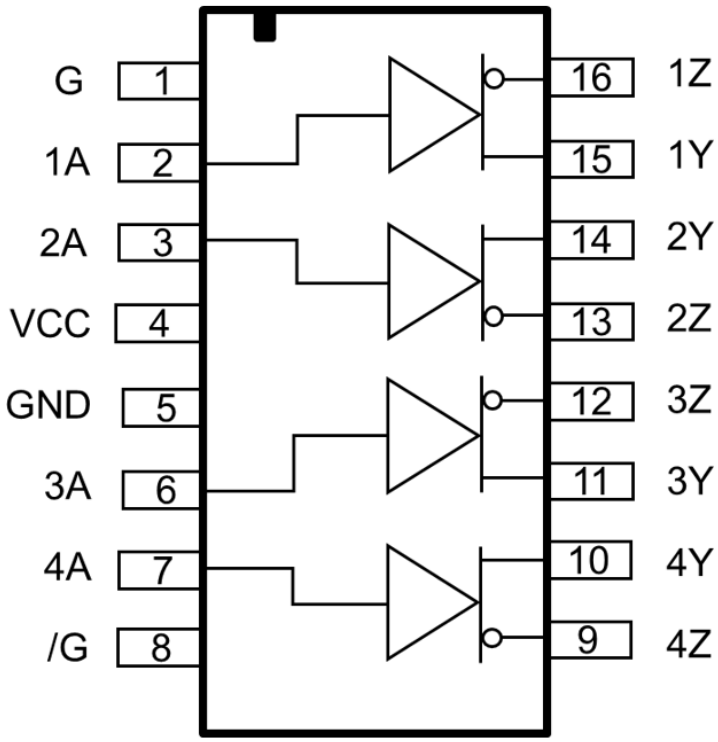
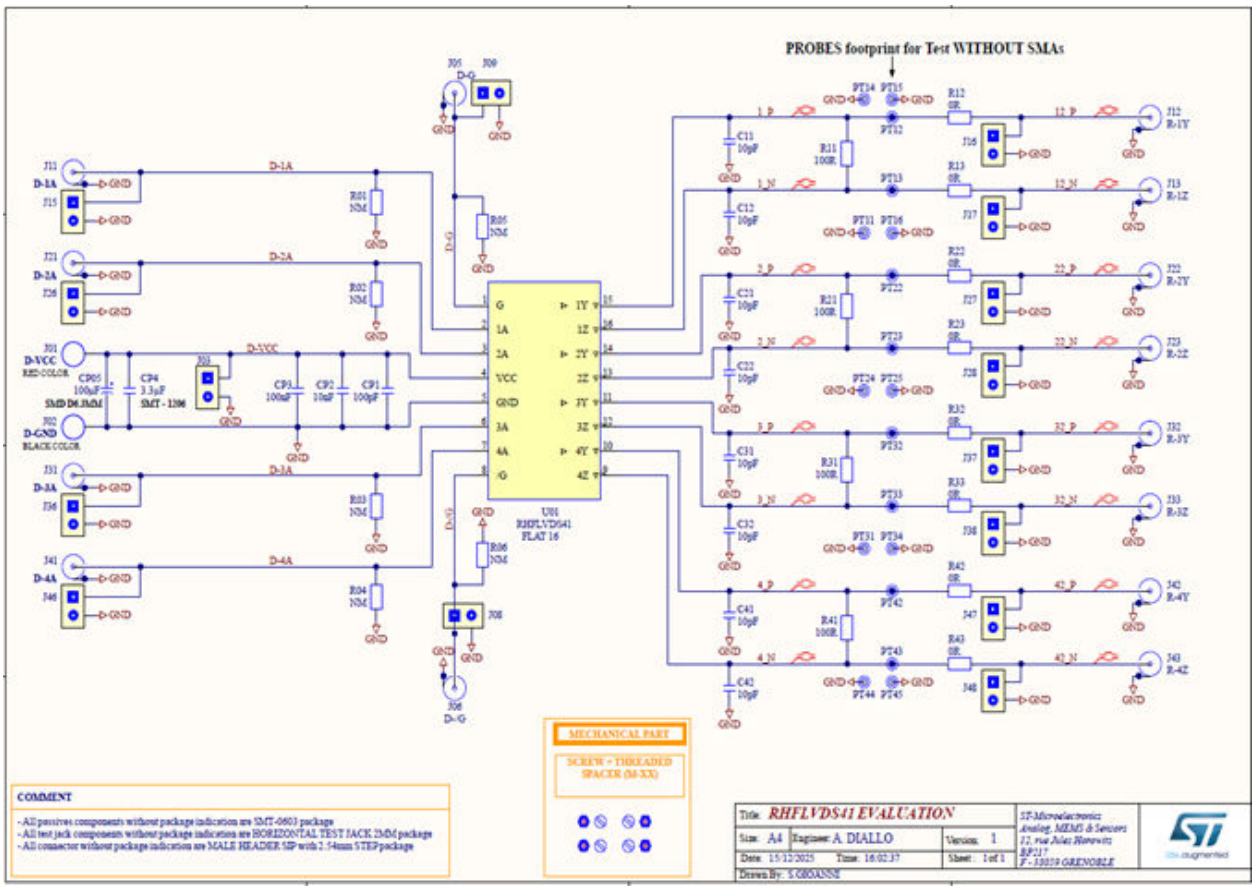


Table 1. **RHFLVDS41 pin description**

Pin number	Symbol	Name and function
2, 3, 6, 7	1A to 4A	LVCMOS inputs
15, 14, 11, 10	1Y to 4Y	LVDS outputs
16, 13, 12, 9	1Z to 4Z	
1	G	Enable
8	/G	Disable
5	GND	Ground (internally connected to the metallic lid)
4	VCC	Supply voltage

2 Evaluation board schematic

Figure 2. **EVAL-RHFLVDS41V1 evaluation board schematic**



3 PCB print out

To allow high-bandwidth signal measurements, the PCB is a four-layered FR-4 material with a thickness of 1.6 mm. The external copper thickness is 45 µm. The PCB tracks of the LVCMOS inputs are adapted to a 50 Ω impedance, while the LVDS outputs differential pairs are adapted to a 100 Ω impedance. The following figures (Figure 3 to Figure 8) show the different layers of the EVAL-RHFLVDS41V1 PCB board.

Figure 3. Top layer

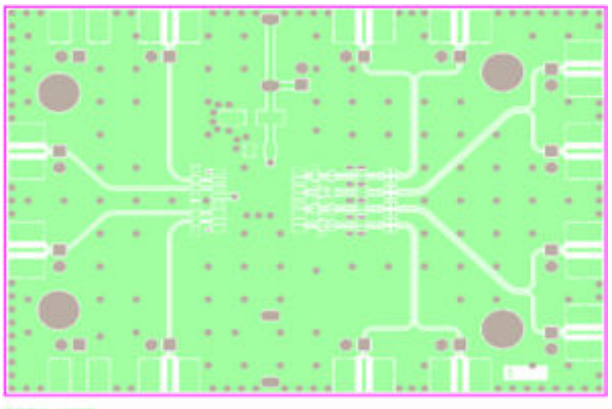


Figure 4. Top overlay

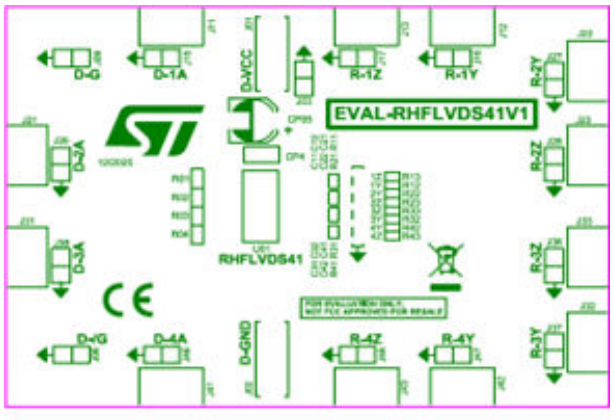


Figure 5. Bottom layer

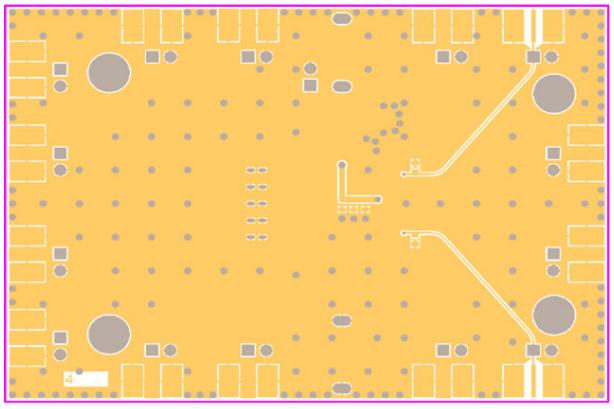


Figure 6. Bottom overlay

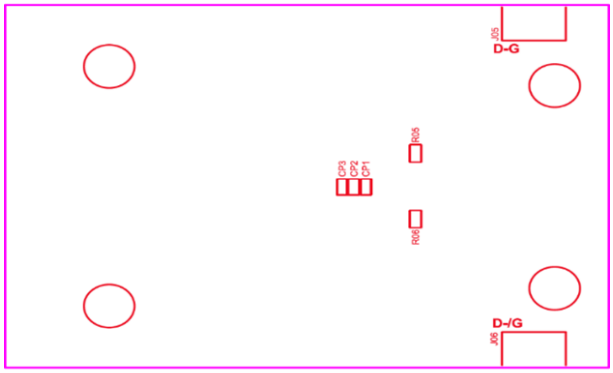


Figure 7. Internal layer N° 2

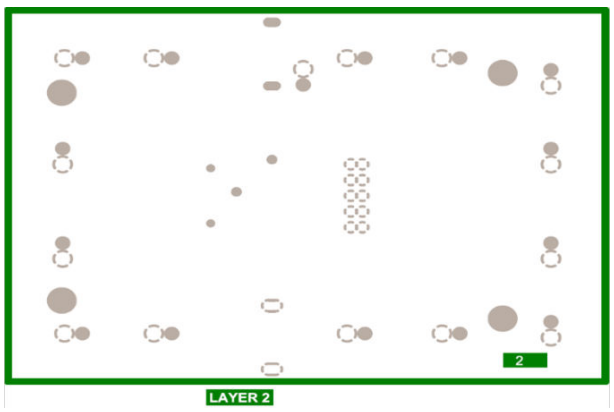
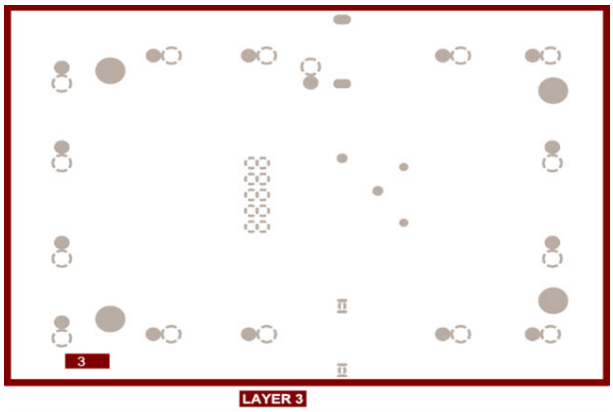


Figure 8. Internal layer N° 3



4 Bill of materials

Table 2. Bill of materials

Q.ty	Reference	Value	Package/Footprint	Manufacturer	Manufacturer's part number
8	C11, C12, C21, C22, C31, C32, C41, C42	10 pF	SMT - 0402	WURTH ELEKTRONIK	885012005055
1	CP1	100 pF	SMT - 0603	WURTH ELEKTRONIK	885012206077
1	CP2	10 nF	SMT - 0603	WURTH ELEKTRONIK	885012206089
1	CP3	100 nF	SMT - 0603	WURTH ELEKTRONIK	885012206095
1	CP4	3.3 µF	SMT - 1206	WURTH ELEKTRONIK	885012208067
1	CP05	100 µF	SMD D6.3MM	KEMET	EXV107M025A9HAA
1	J01	RED COLOR	HORIZONTAL TEST JACK 2MM	JOHNSON - CINCH CONNECTIVITY	105-0752-001
1	J02	BLACK COLOR	HORIZONTAL TEST JACK 2MM	JOHNSON - CINCH CONNECTIVITY	105-0753-001
15	J03, J08, J09, J15, J16, J17, J26, J27, J28, J36, J37, J38, J46, J47, J48	SIP 1x2 MALE	SIP 1x2 STEP 2.54 MM	WURTH ELEKTRONIC	61300211121
14	J05, J06, J11, J12, J13, J21, J22, J23, J31, J32, J33, J41, J42, J43	Subclic	SMA PCB EDGE MOUNT	JOHNSON - CINCH CONNECTIVITY	142-0711-821
4	M-01, M-02, M-03, M-04	10 MM	HOLE M3	ETTINGER	005.03.101
4	M-05, M-06, M-07, M-08	6 MM	HOLE M3	ETTINGER	81.58.322
6	R01, R02, R03, R04, R05, R06	NM = Not Mounted	SMT - 0603	WURTH ELEKTRONIK	560112116133
4	R11, R21, R31, R41	100 R	SMT - 0402	WURTH ELEKTRONIK	560112110022
8	R12, R13, R22, R23, R32, R33, R42, R43	0 R	SMT - 0402	WURTH ELEKTRONIK	560112110001
1	U01	RHFLVDS41	FLAT 16	STMICROELECTRONICS	RHFLVDS41

5 Evaluation board description

5.1 Power supply

The power supply VCC connectors are banana 2 mm and 1 x 2 SIP male types.

Typical power supply voltages are as follows: V_{CC} = 2.3 V to 2.7 V, and V_{CC} = 3 V to 3.6 V.

To prevent noise on the power supply V_{CC}, a 100 µF electrolytic capacitor and a 3 µF ceramic capacitor are placed near the V_{CC} connector, at the board edge.

Three additional bypass capacitors (ceramics) of 100 nF, 10 nF and 100 pF are placed close to the RHFLVDS41 device VCC pin.

5.2 Driver Enable and Disable pins

When the connectors J05/J09 and J06/J08 are left open, RHFLVDS41 is enabled by default.

It is possible to enable or disable the device by applying a voltage level to J05/J09 and J06/J08.

When using an external generator with a 50 Ω source impedance, R05 and R06 resistors can be set to a 50 Ω value for impedance adaptation.

5.3 LVCMOS driver inputs

The 4 LVCMOS input channels (1A, 2A, 3A, and 4A) have different connectors:

- J15, J26, J36 and J46 (1x2 SIP male) are dedicated for the LVCMOS inputs driven directly by another integrated circuit such as a microcontroller or FPGA, or for test points. For example, these connectors can be used for signal probing with active probes.
- The high-bandwidth SMA connectors, J11 , J21, J31, and J41 are dedicated for the LVCMOS inputs driven directly by an external generator. If the generator source impedance is 50 Ω, then a 50 Ω resistance can be mounted on R01, R02, R03, or R04 for impedance adaptation. These SMA connectors are also suitable for input signal connection from other boards with an SMA coaxial cable.

5.4 LVDS driver Outputs

5.4.1 EVAL-RHFLVDS41V1 board usage in driver single evaluation

By default, the EVAL-RHFLVDS41V1 is designed for driver mode evaluation.

Thus, the 4 LVDS output channels have 100 Ω termination resistors (R11, R21, R31, R41) between each pair of differential outputs.

Load capacitors of 10 pF (C11, C12, C21, C22, C31, C32, C41, and C42) are placed at the LVDS outputs. Of course, the user can adapt this value to their application.

The test points are as follows :

- For low-signal probing (up to 80 Mbps), the LVDS signals can be observed at test points J16, J17 , J27, J28, J37, J38, J47, and J48 with any type of probe. The SMA connectors J12, J13, J22, J23, J32, J33, J42, and J43 can also be used with an SMA cable with a BNC adaptor at the oscilloscope high-impedance input.
- For medium-frequency signal probing (up to 200 Mbps), the LVDS signals can be observed at test points J16, J17, J27, J28, J37, J38, J47, and J48 with active probes.
- For high-speed signal probing up to 600 Mbps, it is advised to use high-bandwidth probes at the PT11 to PT45 test points. Then, the 0 Ω serial resistor (R12, R13, R22, R23, R32, R33, R42, R43) must be removed to reduce reflections on the measured signal. Differential probe tips can also be soldered in differential mode to directly probe the driver differential output voltage signal $V_{OD} = V_y - V_z$.

5.4.2 EVAL-RHFLVDS41V1 board usage in driver/receiver system evaluation

For driver/receiver system configuration testing, those 100 Ω resistors must be removed from the EVAL-RHFLVDS41V1 board and placed at the receiver board side, such as EVAL-RHFLVDS42V1. The 100 Ω termination resistor must be placed as close as possible to the LVDS receiver inputs (see Figure 9).

The receiver board could be connected to the EVAL-RHFLVDS41V1 through SMA coaxial cables thanks to the connectors J12, J13, J22, J23, J32, J33, J42 and J43.

Figure 9. Typical LVDS driver/receiver system schematic

Revision history

Table 3. **Document revision history**

Date	Revision	Changes
30-Jun-2026	1	Initial release.

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