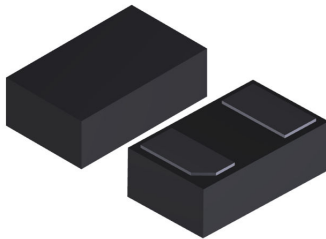
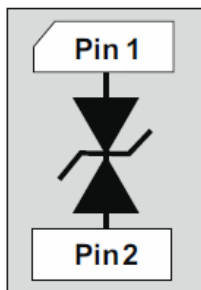



Automotive single line ESD protection for high speed lines in SOD882T (0402)



SOD882T(0402)
(QFN-2L 1.0 x 0.6 x 0.35)



Features

- AEC-Q101 qualified and PPAP capable 
- Ultra large bandwidth: 15 GHz
- Ultra low capacitance: 0.3 pF
- Very low leakage current at V_{RM} ($I_R < 100$ nA)
- Operating T_j max.: 150 °C
- RoHS compliant component

Complies with the following standards

- J-STD-020 MSL level 1 and UL94, V0
- ISO 10605 - C = 150 pF, R = 330 Ω
 - ± 20 kV (contact discharge)
 - ± 30 kV (air discharge)
- ISO 10605 - C = 330 pF, R = 330 Ω
 - ± 15 kV (contact discharge)
 - ± 30 kV (air discharge)
- ISO 7637-3:
 - pulse 3a: $V_s = -150$ V
 - pulse 3b: $V_s = +150$ V
 - pulse 2a: $V_s = \pm 85$ V

Product status link

[ESDXLC6-1BT2Y](#)

Application

Automotive high-speed application where electrostatic discharges and other transients must be suppressed such as:

- SerDes buses like FPD-Link, GMSL, AsA, MIPI A-PHY, APIX
- Short-reach LVDS like MIPI CSI
- Automotive cameras and Display
- Sensors
- RF antenna
- USB 2.0 and USB 3.x
- HDMI 2.2
- Ethernet

Description

The **ESDXLC6-1BT2Y** is a bidirectional ESD device designed to protect sensitive automotive high-speed electronics from damage or latch-up due to repetitive electrostatic discharges (ESD) without aging effect and performance drift.

The **ESDXLC6-1BT2Y** helps ensure excellent signal integrity on challenging automotive high-speed interfaces such as SerDes communication links or multi-Giga Ethernet.

In addition, this product is available in a small, popular SOD882T package, with 1.0 mm x 0.6 mm size, ideal for space-constrained applications.

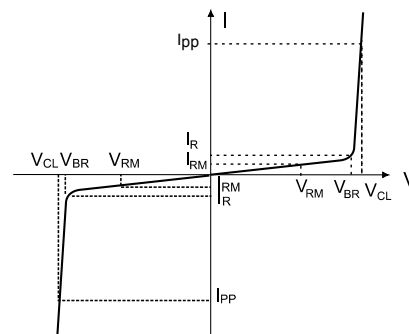
1 Characteristics

Table 1. Absolute maximum ratings ($T_{amb} = 25\text{ }^{\circ}\text{C}$)

Symbol	Parameter	Value	Unit	
V_{PP}	Peak pulse voltage	ISO10605 / IEC 61000-4-2 (C = 150 pF, R = 330 Ω):	kV	
		Contact discharge		20
		Air discharge		30
		ISO10605 (C = 330 pF, R = 330 Ω):		
	Contact discharge	15		
	Air discharge	30		
P_{PP}	Peak pulse power dissipation (8/20 μs)	TBD	W	
I_{PP}	Peak Pulse current (8/20 μs)	3	A	
T_{stg}	Storage temperature range	-65 to +150	$^{\circ}\text{C}$	
T_j	Operating junction temperature range	-55 to +150	$^{\circ}\text{C}$	
T_L	Maximum lead temperature for soldering during 10 s	260	$^{\circ}\text{C}$	

Figure 1. Electrical characteristics (definitions)

Symbol	Parameter
V_{BR}	Breakdown voltage
V_{RM}	Stand-off voltage
V_{CL}	Clamping voltage
I_{RM}	Leakage current at V_{RM}
I_{PP}	Peak pulse current
R_d	Dynamic impedance
C_{LINE}	Input capacitance per line


Table 2. Electrical characteristics (values) ($T_{amb} = 25\text{ }^{\circ}\text{C}$)

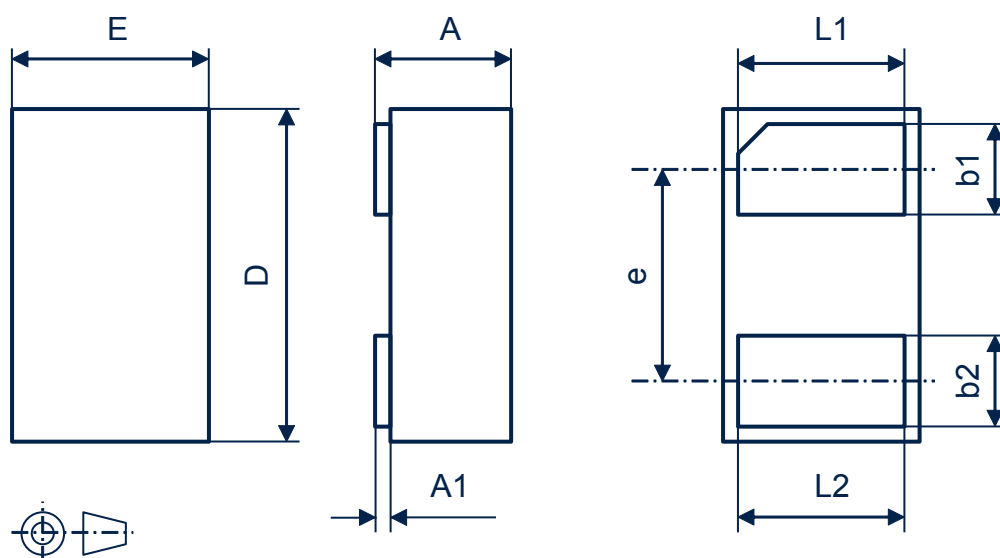
Symbol	Test conditions	Min.	Typ.	Max.	Unit
V_{BR}	$I_R = 1\text{ mA}$	6	7		V
I_{RM}	$V_{RM} = 3\text{ V}$			100	nA
V_{CL}	ISO 10605 - C = 150 pF, R = 330 Ω +8 kV contact discharge, measured at 30 ns		25		V
$C_{I/O-GND}$	$V_{I/O} = 0\text{ V}$, 200 MHz < f < 3 GHz, $V_{OSC} = 30\text{ mV}$		0.3		pF
f_C	$S_{21} = -3\text{ dB}$		15		GHz

2 Package information

To meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

2.1 Package information

Figure 2. Package outline



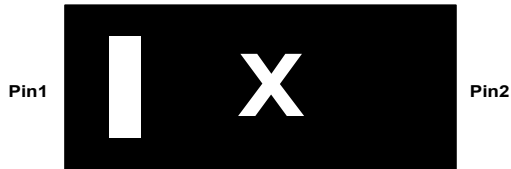
7979241_Rev7_package-outline

Table 3. Package mechanical data

Ref.	Dimensions		
	Millimeters		
	Min.	Typ.	Max.
A	0.30		0.40
A1	0.00		0.05
L1	0.45	0.50	0.55
L2	0.45	0.50	0.55
D	0.95	1.00	1.05
E	0.55	0.60	0.65
e	0.60	0.65	0.70
b1	0.20	0.25	0.30
b2	0.20	0.25	0.30

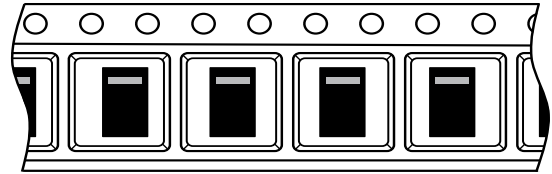
2.2 Packing and marking information

Figure 3. Marking layout



X: Refer to ordering information table for marking.

Figure 4. Package orientation in reel



Taped according to EIA-481

Note: Pocket dimensions are not on scale
Pocket shape may vary depending on package
On bidirectional devices, marking and logo may be not always in the same direction

Figure 5. Tape leader and trailer dimensions

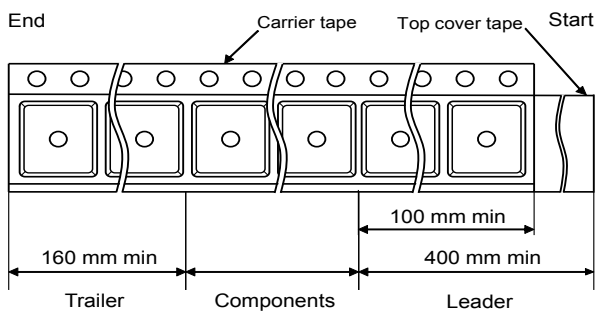


Figure 6. Tape and reel orientation

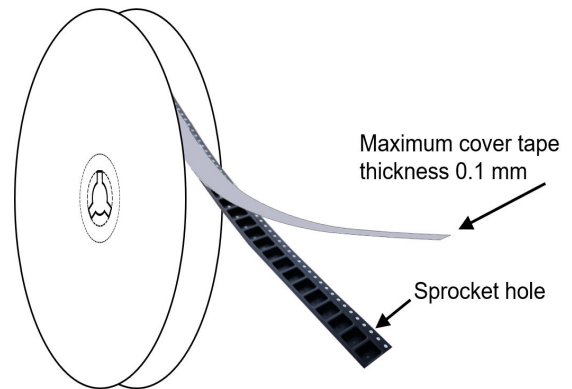


Figure 7. Reel dimensions (mm)

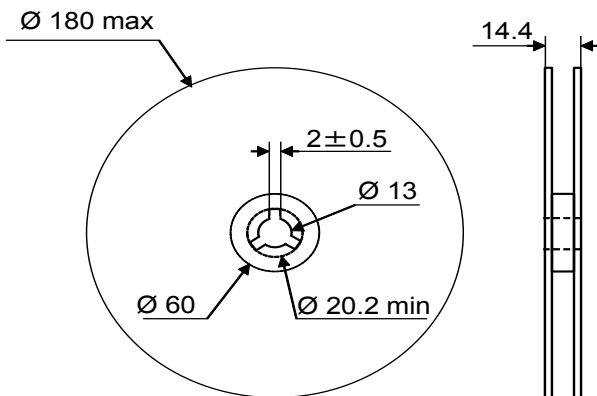


Figure 8. Inner box dimensions (mm)

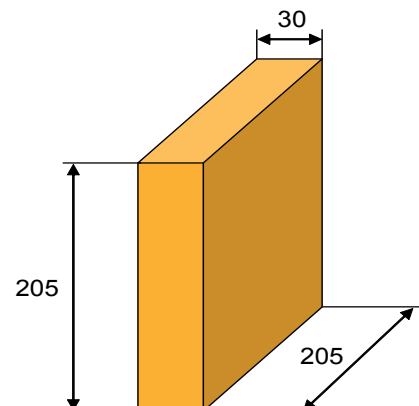
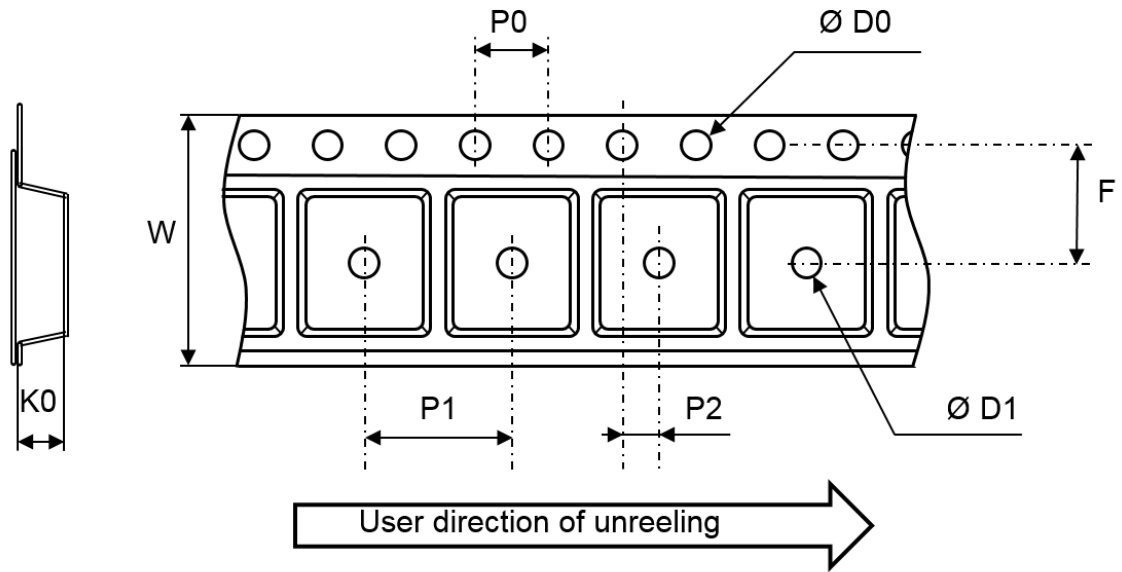


Figure 9. Tape outline



Note: Pocket dimensions are not on scale
Pocket shape may vary depending on package

Table 4. Tape and reel mechanical data

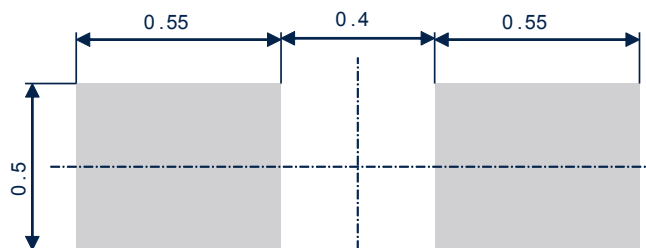
Ref.	Dimensions		
	Millimeters		
	Min.	Typ.	Max.
D0	1.45	1.5	1.6
D1	0.35		
F	3.45	3.5	3.55
K0	0.42	0.47	0.52
P0	3.9	4	4.1
P1	1.95	2	2.05
P2	1.95	2	2.05
W	7.9	8	8.3

3 Recommendations on PCB assembly

3.1 Footprint

SMD footprint design is recommended.

Figure 10. SOD882T recommended footprint

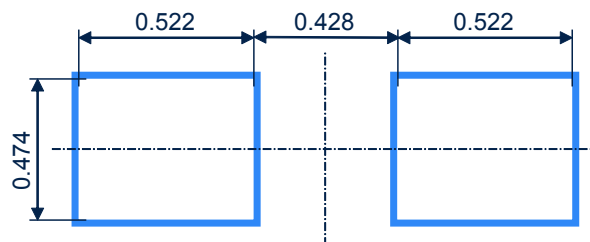


7979241_Rev-7_footprint

3.2 Stencil opening design

Stencil opening thickness: 75 μm / 3 mils

Figure 11. Stencil opening recommendations



3.3 Solder paste

1. Halide-free flux, qualification ROL0 according to ANSI/J-STD-004.
2. "No clean" solder paste recommended.
3. Tack force high enough to resist component displacement during PCB movement.
4. Particles size 20-38 μm per IPCJ STD-005.

3.4 Placement

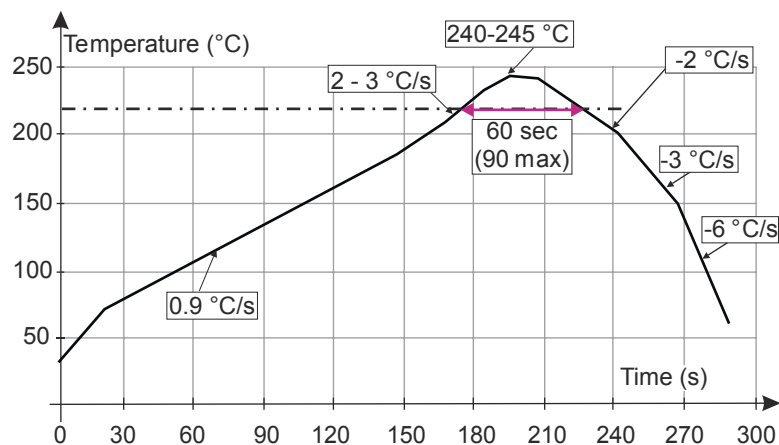
1. It is recommended to use leads recognition instead of package outline for accurate placement on footprint with adequate resolution tool.
2. Tolerance of $\pm 50 \mu\text{m}$ is recommended.
3. 1.0 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
4. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

3.5 PCB design preference

1. Any via around or inside the footprint area must be closed to avoid solderpaste migration in the via.
2. Position and dimensions of the tracks should be well balanced. A symmetrical layout is recommended to prevent assembly troubles.

3.6 Reflow profile

Figure 12. ST ECOPACK recommended soldering reflow profile for PCB mounting



Note: Minimize air convection currents in the reflow oven to avoid component movement. O_2 rate inside the oven must be below 500 ppm. Maximum soldering profile corresponds to the latest IPC/JEDEC J-STD-020.

Revision history

Table 5. Document revision history

Date	Revision	Changes
01-Jul-2026	1	Initial release.

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