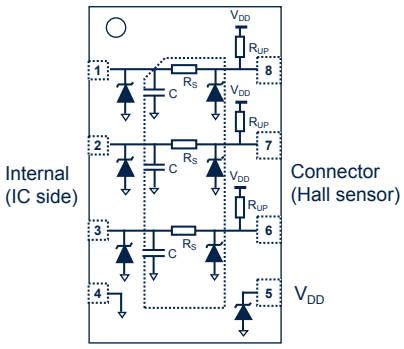
EMIF03-22K10M8Y

Data brief

Automotive 3-line EMI filter with ESD protection for BLDC motor controlled with hall sensors

QFN-8L 2.0 x 1.5 mm



GND connected to exposed pad and pin 4

Product status
EMIF03-22K10M8Y

Features

- AEC-Q101 qualified and PPAP capable
- 3-line EMI filter low pass filter and pull-up resistors
- High efficiency in EMI filtering: -20 dB from 700 kHz
- Embedded ESD protection including V_{DD} input
- Wettable-flank QFN package with exposed pad
- Low leakage current
- ECOPACK2 RoHS compliant component
- **Complies with the following standards**:
  - J-STD-020 MSL level 1 and UL94, V0
  - IPC7531 footprint and JEDEC registered package
- **Complies with ISO 10605 / IEC 61000-4-2 - C = 150 pF, R = 330 Ω**:
  - ±TBD kV (air discharge)
  - ±15 kV (contact discharge)
- **Complies with ISO 10605 - C = 330 pF, R = 330 Ω**:
  - ±TBD kV (air discharge)
  - ±12 kV (contact discharge)
- **Complies with ISO 7637-3**:
  - Pulse 3a : -150 V
  - Pulse 3b : +150 V
  - Pulse 2a: +/-85 V

Application

Brushless DC motor applications using hall sensors where EMI filtering and protection against ESD are required:

- Automotive BLDC motor
  - Electric power steering (EPS)
  - Seat control, HVAC and climate control
- Industrial BLDC motor control
  - Power tools, Servo drives, Drones
  - Robotics, E-bike

Description

Developed for brushless DC (BLDC) motor applications to filter spikes on the hall sensors lines while protecting the MCU or the motor control IC against ESD events, the EMIF03-22K10M8Y is a 3-line EMI filter embedding pull-up resistors and ESD protections.

Housed in wettable flank QFN-8L 2.0 x 1.5 mm, ideal for space constrained applications, it is designed to withstand ISO 10605 and ISO 7637-3 surges.

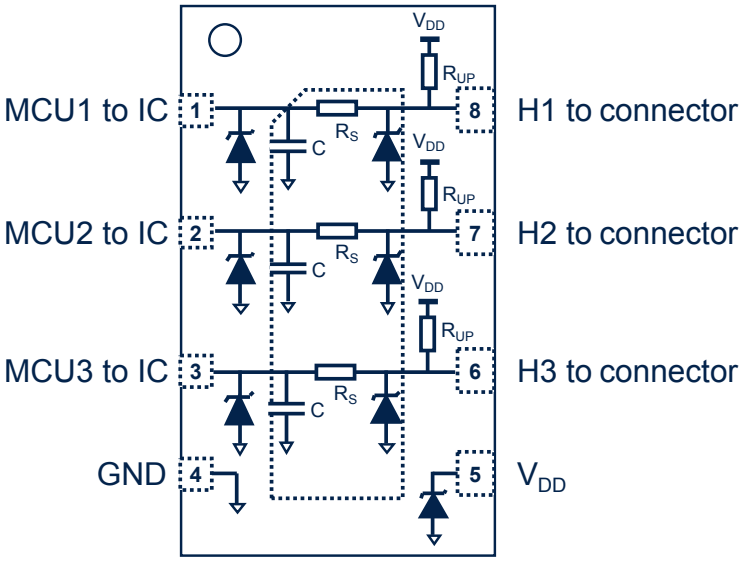
This component is perfect for designers looking to improve their products' EMI suppression capabilities with a space-efficient and reliable solution.

1 Pin configuration and functions

Table 1. EMIF03-22K10M8Y pin description

Pin #	Name	Description
1	MCU1	Hall sensor 1 filter output to IC, ESD protected
2	MCU2	Hall sensor 2 filter output to IC, ESD protected
3	MMCU3	Hall sensor 3 filter output to IC, ESD protected
4	GND	Ground
5	V_{DD}	V_{DD} rail ESD protection and pull-up resistors inputs
6	H1	Hall sensor 1 input, ESD protected
7	H2	Hall sensor 2 input, ESD protected
8	H3	Hall sensor 3 input, ESD protected
TAB	GND	Ground

Figure 1. EMIF03-22K10M8Y pinout (top view)



Connect both exposed pad and pin4 to ground to lower ground path parasitics

2 Characteristics

Table 2. Absolute maximum ratings (T_{amb} = 25 °C)

Symbol	Parameter			Value	Unit
V_{PP}	Peak pulse voltage	ISO 10605 / IEC 61000-4-2 level, 4 C = 150 pF, R = 330 Ω: Contact discharge Air discharge	H_X pins; V_{DD}	±15 ±TBD	kV
			MCU_X pins	±25 ±TBD	
		ISO 10605 - C = 330 pF, R = 330 Ω: BUS pins Contact discharge Air discharge	H_X pins; V_{DD}	±12 ±TBD	
		HBM (human body model) - MIL STD 883C (C = 100 pF, R = 1.5 kΩ) IC pins	All pins	±8	
T_j	Operating junction temperature range			-55 to +150	°C
T_{stg}	Storage temperature range			-55 to +150	°C
T_L	Maximum lead temperature for soldering during 10 s			260	°C

Figure 2. Electrical characteristics (definitions)

V_{RM} Maximum stand-off voltage
I_{RM} Maximum leakage current @V_{RM}
V_R Stand-off voltage
I_R Leakage current @V_R
V_{BR} Breakdown voltage @I_{BR}
I_{BR} Breakdown current
V_{CL} Clamping voltage @I_{PP}
I_{PP} Peak pulse current
R_D Dynamic resistance
V_F Forward voltage drop @I_F
I_F Forward current

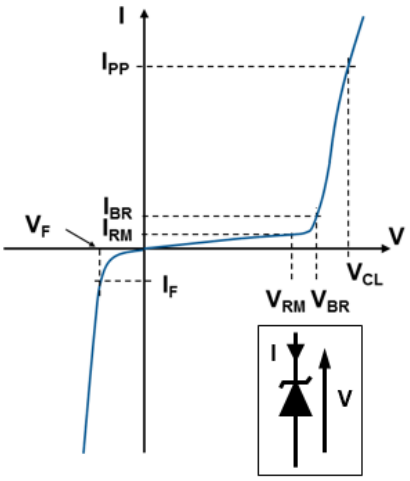


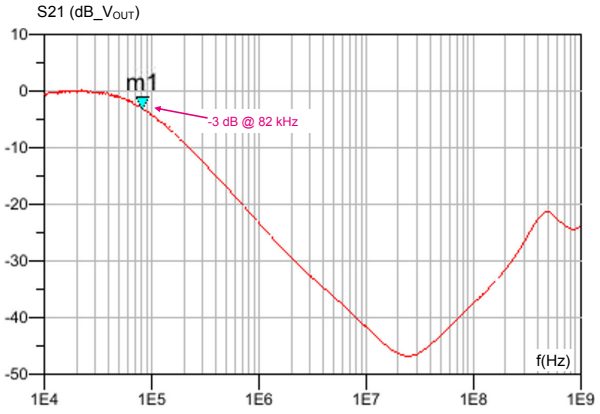
Table 3. Electrical characteristics (T_{amb} = 25 °C, unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{RM}	Reverse Stand-off voltage	Any I/O pin to GND			5	V
V_{BR}	Breakdown voltage	I_R = 1 mA, any I/O pin to GND	18	19		V
V_F	Forward voltage	I_F = 10 mA, any I/O pin to GND		1		
I_R	Reverse leakage current at V_R	V_R = 3.3 V, any I/O pin to GND			TBD	nA
I_{RM}	Reverse leakage current at V_{RM}	V_{RM} = 5 V, any I/O pin to GND			100	nA
R_S	Serial resistor	I_{RS} = 0.5 mA	19.8	22	24.2	kΩ
R_{UP}	Pull-up resistor	I_{RUP} = 1.0 mA	0.8	1	1.2	kΩ
C_{LINE}	Line capacitance	V_{LINE} = 0 V, f = 1 MHz, V_{osc} = 180 mV, measured on MCU_X pins	80	100	120	pF
f_C (1)(2)	Cut-off frequency	Cut-off frequency at -3dB with R_{IN} (H_X pin) = 10 Ω and R_{OUT} (MCU_X pins) = 1 MΩ, pin4 and exposed pad connected to ground		82		kHz
V_{CL} (1)	Clamping voltage	ISO 10605 / IEC 61000-4-2, C = 150 pF, R = 330 Ω + 8 kV contact discharge on H_X pins, measured at 30 ns on MCU_X pins		TBD		V

1. *Specified by design – Not tested in production.*
2. *Normalized to attenuation at 1 MHz*

2.1 Characteristics curves

Figure 3. S21 response with R_{IN} (Hx pins) = 10 Ω and R_{OUT} (MCU pins) = 1MΩ



3 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

3.1 Package information

Figure 4. QFN-8L package outline

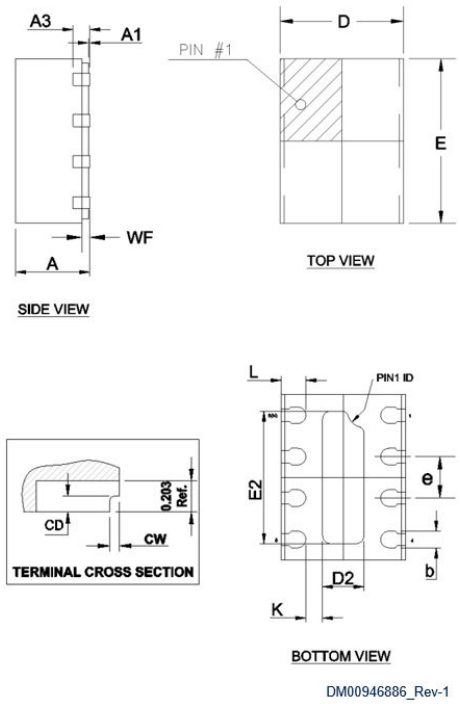


Table 4. QFN-8L package mechanical data

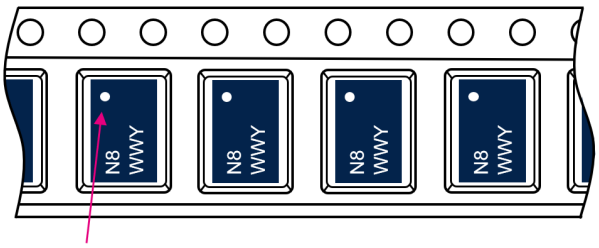
Ref.	Dimensions (mm)		
	Min.	Typ.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.203	
b	0.15	0.20	0.25
D	1.45	1.50	1.55
E	1.95	2.00	2.05
e		0.50	
D2	0.40	0.50	0.60
E2	1.50	1.60	1.70
K	0.20		
L	0.20	0.30	0.40
CD	0.10		
CW	0.02	0.05	0.08
WF	0.10		

Figure 5. Marking

N8: Marking
WW : Week Y : Year

Dot indicates pin 1

Figure 6. Package orientation in reel



Pin 1 located according to EIA-481

Note: Pocket dimensions are not on scale only pin 1 mark must be used to orient the component for its placement on a PCB.

Figure 7. 7" reel dimension values (mm)

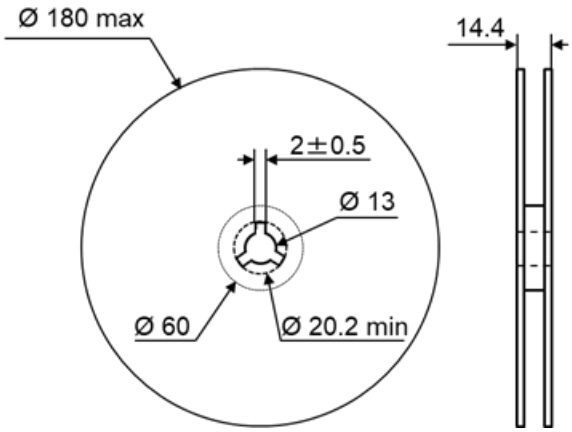


Figure 8. Tape and reel orientation

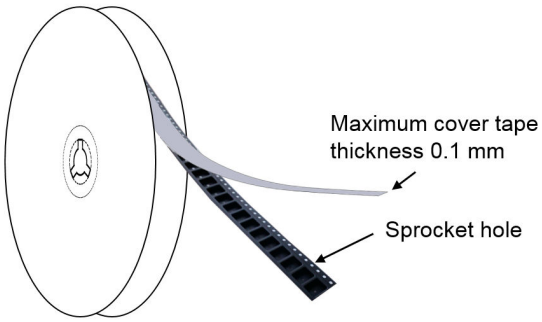


Figure 9. Inner box dimensions (mm)

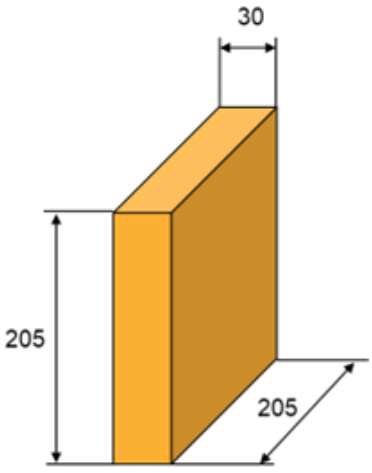
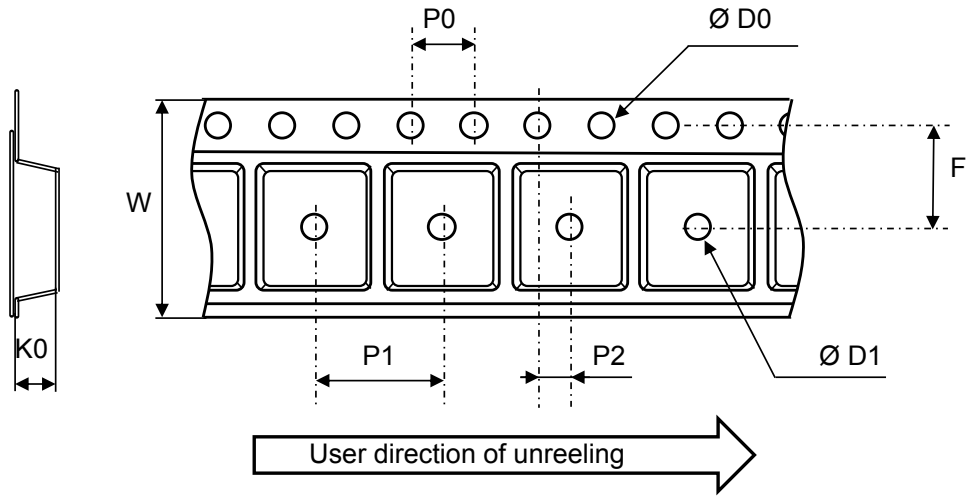


Figure 10. **Tape and reel outline**

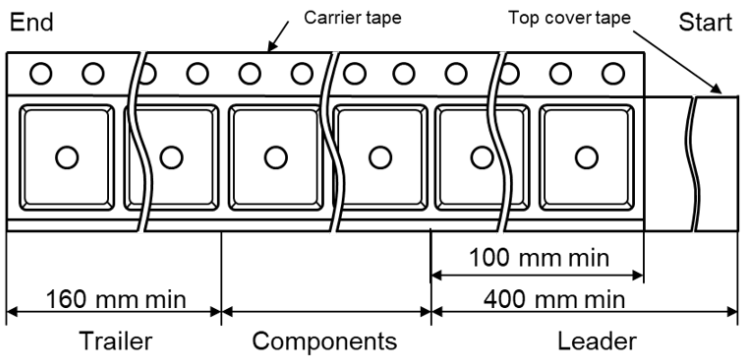


Note: Pocket dimensions are not on scale
Pocket shape may vary depending on package

Table 5. **Tape and reel mechanical data**

Ref	Dimensions		
	Millimeters		
	Min	Typ	Max
D0	1.50	1.55	1.60
D1	1.00	1.05	1.10
F	3.45	3.50	3.55
K0	0.85	0.90	0.95
P0	3.90	4.00	4.10
P1	3.90	4.00	4.10
P2	1.95	2.00	2.05
W	7.90	8.00	8.30

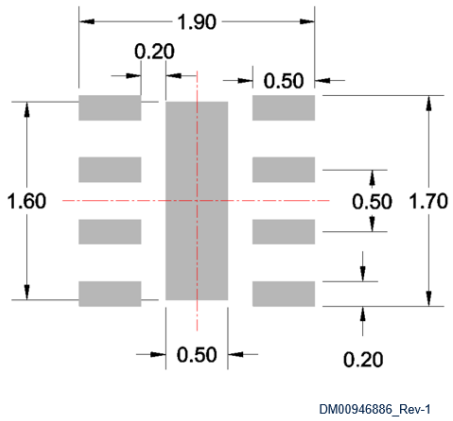
Figure 11. **Tape leader and trailer dimensions**



4 Recommendation PCB assembly

4.1 Footprint

Figure 12. **Recommended footprint in mm**



4.2 Stencil opening design

- Stencil opening thickness: 75 µm / 3 mils
- Stencil opening ratio: 90%

Figure 13. **Stencil opening recommendations in mm**

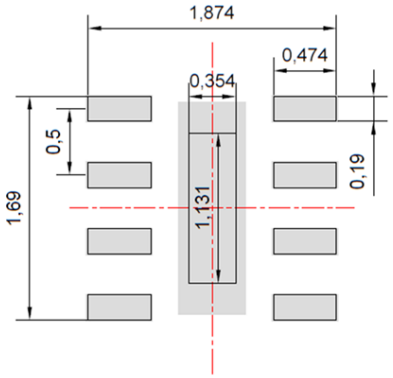


Figure 14. **Wettable flank profile**

Note: You can find the wettable flank values in Table 4.

4.3 Solder paste

1. Halide-free flux, qualification ROL0 according to ANSI/J-STD-004.
2. “No clean” solder paste recommended.
3. Tack force high enough to resist component displacement during PCB movement.
4. Particles size 20-38 µm per IPCJ STD-005.

4.4 Placement

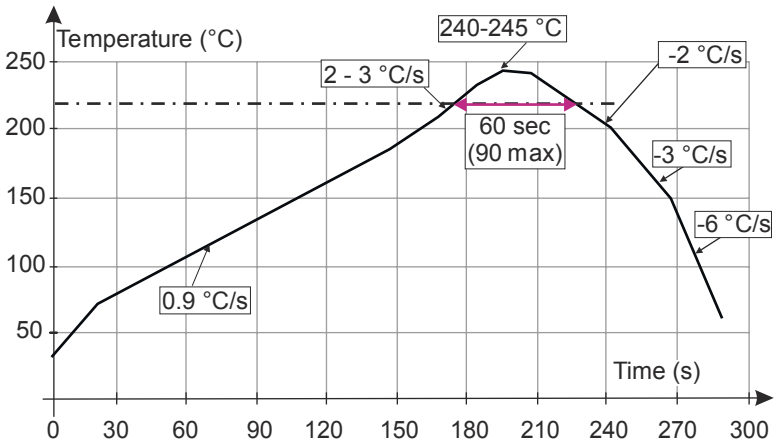
1. It is recommended to use leads recognition instead of package outline for accurate placement on footprint with adequate resolution tool.
2. Tolerance of ±50 µm is recommended.
3. 1.0 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
4. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

4.5 PCB design preference

1. Any via around or inside the footprint area must be closed to avoid solderpaste migration in the via.
2. Position and dimensions of the tracks should be well balanced. A symmetrical layout is recommended to prevent assembly troubles.

4.6 Reflow profile

Figure 15. ST ECOPACK recommended soldering reflow profile for PCB mounting



Note: Minimize air convection currents in the reflow oven to avoid component movement. O_2 rate inside the oven must be below 500 ppm. Maximum soldering profile corresponds to the latest IPC/JEDEC J-STD-020.

5 Ordering information

Figure 16. **Ordering information scheme**

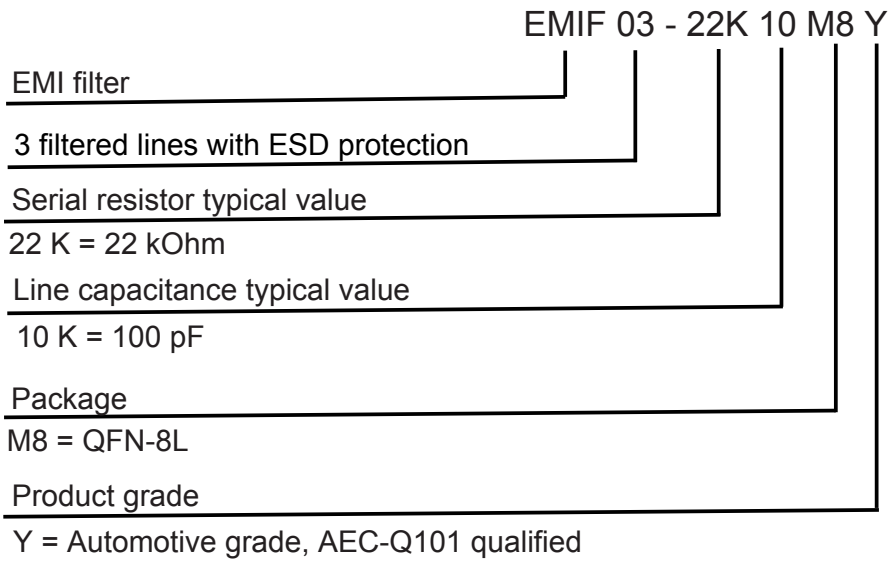


Table 6. **Ordering information**

Order code	Marking	Package	Weight	Base qty.	Delivery mode
EMIF03-22K10M8Y	N8[1]	QFN-8L	6.67 mg	3000	Tape and reel

1. *The marking can be rotated by 90° to differentiate assembly location*

Revision history

Table 7. **Document revision history**

Date	Revision	Changes
10-Aug-2026	1	Initial release.

IMPORTANT NOTICE – READ CAREFULLY

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice.

In the event of any conflict between the provisions of this document and the provisions of any contractual arrangement in force between the purchasers and ST, the provisions of such contractual arrangement shall prevail.

The purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgment.

The purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of the purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

If the purchasers identify an ST product that meets their functional and performance requirements but that is not designated for the purchasers' market segment, the purchasers shall contact ST for more information.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, refer to www.st.com/trademarks. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.