Linear mode operations for motor control with planar "Linear Proof" STripFET™ and "Simple Added Features FET" SAFeFET™

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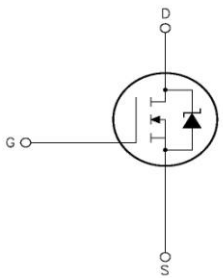
Abstract: Due to the straight link with the thermal coefficient Z_{thj-a} and application conditions (V_{ds} and I_{ds}), the planar STripFET technology devices are able to withstand very high power dissipation, during turn off phase, in a linear mode FAN control application. Bench measurements are performed to compare the performances of standard planar STripFET versus the "linear proof technology", which SAFeFET™ belongs to.

1. Introduction

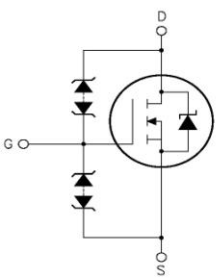
In order to reduce costs and design features in an easier manner, most of the largest automotive customers are recently including the Power MOSFET driven in "linear mode" in most of their electronic systems. The main advantage in using a MOSFET as a "voltage controlled resistor" is that the EMI issues linked to the PWM are resolved and costs are reduced. Due to the very hard working conditions, high V_{DS} and I_D, the MOSFET is forced to manage a very high power, so it should match some technology requirements, plus thermal management inquires, which allow it to withstand such thermo-mechanical and electrical stress. In order to be successful in this kind of environment, STMicroelectronics has developed a dedicated planar STripFET™ structure, which sustains the high power dissipation linked to the linear operations. Three different devices have been tested in a FAN control system board, where the Power MOSFET is used as a linear regulator to drive the FAN:

1. **STP141NF55** "linear proof" STripFET™ device
2. **STP80NS04ZB** (SAFeFET™: Simple Added Features FET), STripFET™ device with gate to source ESD protection and drain-gate active clamp, see pictures below.
3. **Standard** StripFET™ device

The devices belong to the Automotive Graded products.



Standard STripFET™



SAFeFET™

2. Bench measurements between Standard and Linear Proof STripFET technology

The first bench measurement is performed by creating a test board with a P-channel FET that allows the user to discharge a previously stored energy in two 47000µF paralleled capacitors, directly connected by a 100Ω resistor to the 48V power supply (fig.1). The D.U.T. is turned off with the gate connected by a 500Ω resistor to the ground. By connecting two 39V/0.5W Zener diodes back to back between the gate and the drain, when the drain-source voltage rises, achieving the Zener breakdown, a discharging capacitor energy proportional current, which flows through the diodes and the gate-ground resistor, provide a relative gate-source voltage drop, which is able to turn on the device. This working condition pushes the Power MOSFET to manage the energy in a different manner. In fact, it now works in linear zone (V_{DS}>$V_{DS(sat)}$): it is turned on and the current flows through its channel instead of following the avalanche path provided by the body-drain diode id the V_{DS} ,which was overcome by the breakdown of the device .

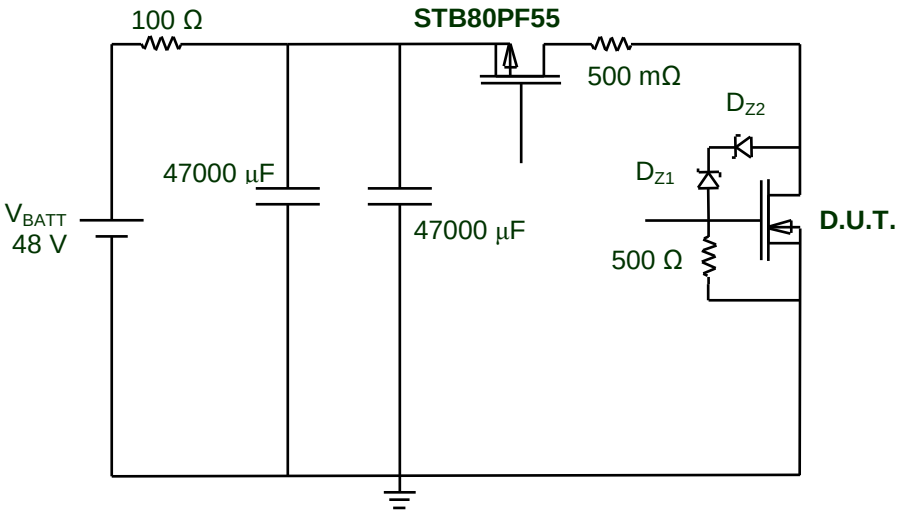


Fig.1

In fig.2, the single 50µs pulse applied to both devices is reported, as shown below, that when a negative V_{GS} is applied to the p-channel device, the energy is transferred to the DUT.

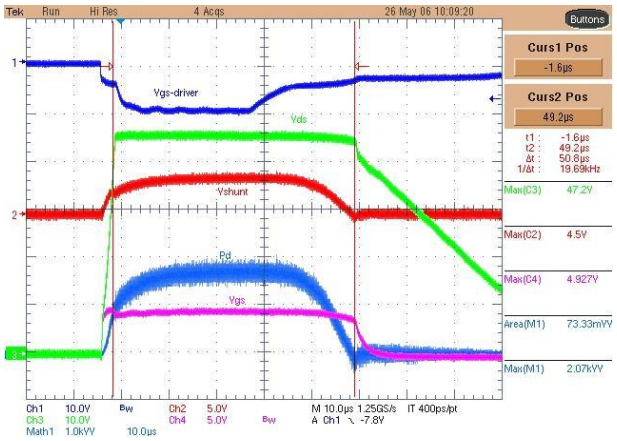


Fig.2

The Power MOSFET V_{GS} decreases proportionally to the current that flows through it. Fig.3, reports the pulse sequence, which both devices that belong to different technologies are submitted to. After a specific number of pulses, the device fails, it becomes short circuited and doesn't manage the flowing current anymore. This will be clamped to the maximum current limit provided by the Power Supply Unit.

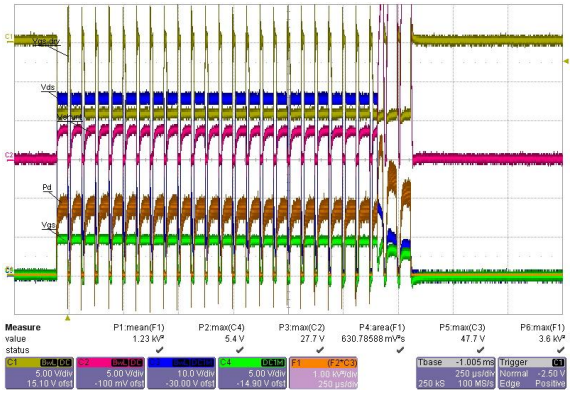


Fig.3

Finally, in fig.4, a cumulative distribution on the failure pulse number for both devices is illustrated:

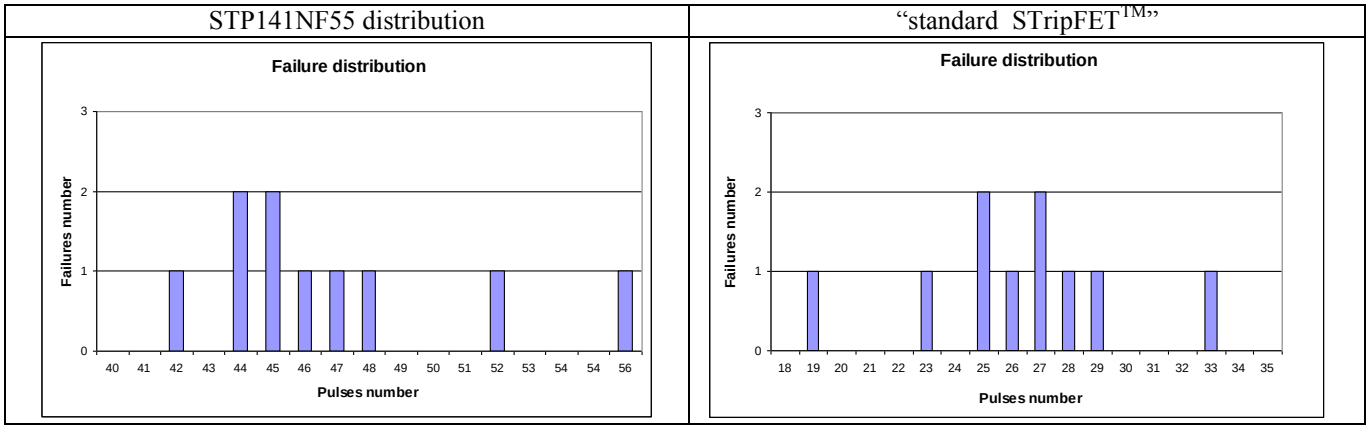


Fig.4

We can easily see that the average number of pulses before a failure is higher for STP141NF55 (at the same test conditions). Therefore, the higher ruggedness of this dedicated technology is clearly identified.

To test the ruggedness of STP80NS04ZB, we submitted it to 1 hour of a continuous endurance test. The test layout set up is shown in fig.5. Here, the Power MOSFET is in the high-side position, with the motor coil directly connected to the source; the drain is connected to the 15V Power Supply Unit and the gate is driven by a power amplifier in push-pull configuration. Two samples have been tested. Figure 5 illustrates the Power MOSFET gate driving circuit and the test board.

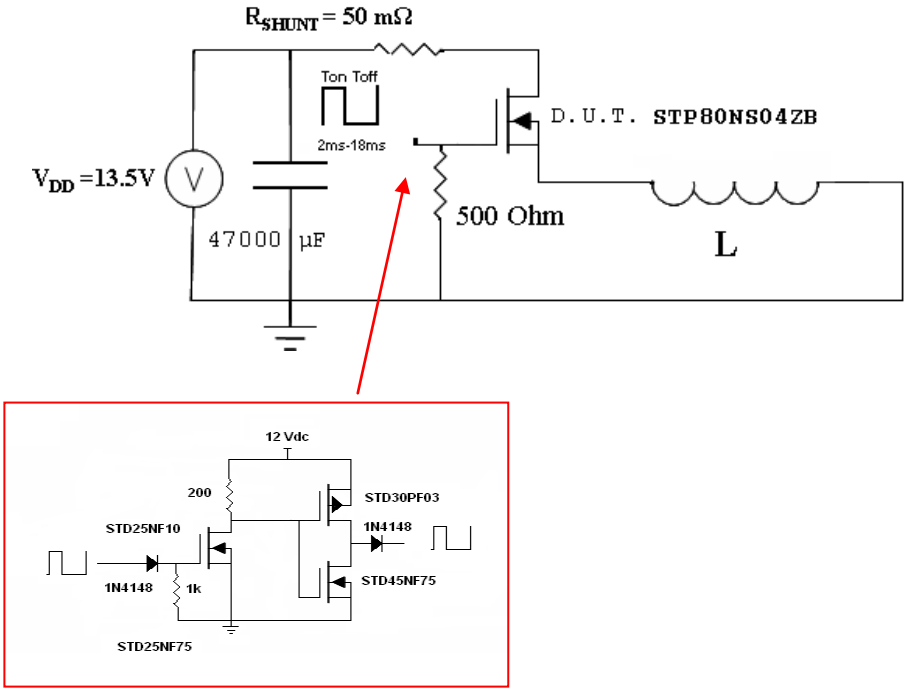


Fig.5

Below the single pulse detail, pulse sequence (fig.6) and comparative table of the main electrical parameters measured before and after the continuous 1h endurance test on the two samples is shown.

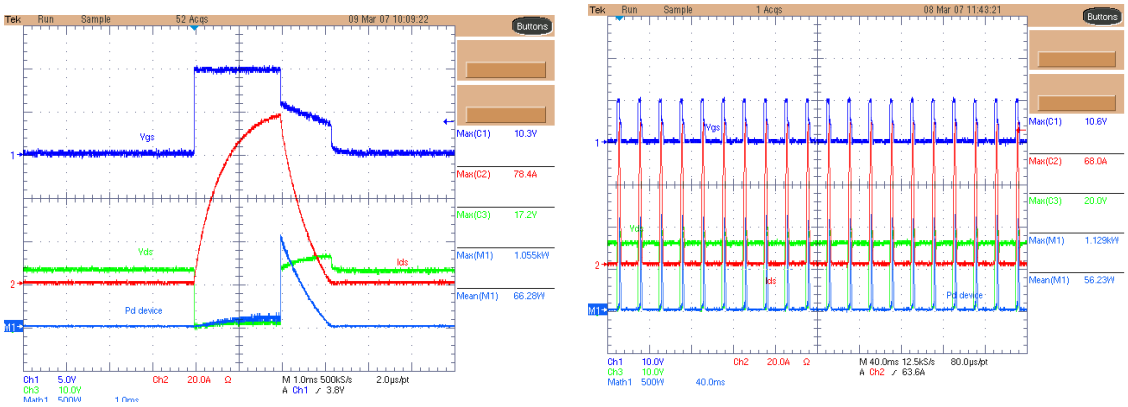


Fig.6

In fig.7, we can see that no electrical parameter is modified by the thermo-mechanical and electrical stress applied on the device under test.

	BV_{DSS} [V]	Vth @ Ids=250µA [V]	Idss @ Vds=32V [µA]
sample #1 STP80NS04ZB Before stress	36.8	2.7	4
sample #1 STP80NS04ZB after stress	36.8	2.7	4
sample #2 STP80NS04ZB Before stress	37	2.70	3.2
sample #2 STP80NS04ZB after stress	37	2.70	3.6

Fig.7 - Comparative table

3. Real system evaluation

Finally, the real system evaluation trial on the STP80NS04ZB in a "linear driven" fan control system is reported. Figure 8 illustrates the functional diagram of the system analyzed .By increasing the duty cycle of the BJT, the V_{GS} applied to the MOSFET may be reduced , as well as the motor speed.

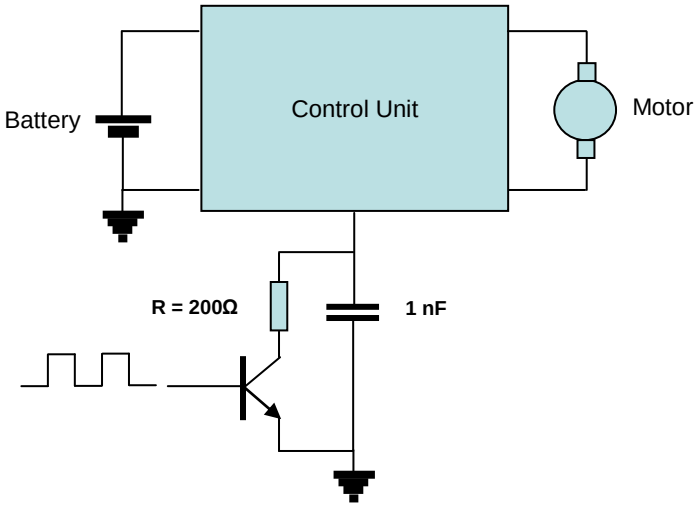


Fig.8

In the following waveforms the steady state working conditions (fig.9) and the start up power dissipation (fig.10), when the duty cycle is set up at 50 % are shown.

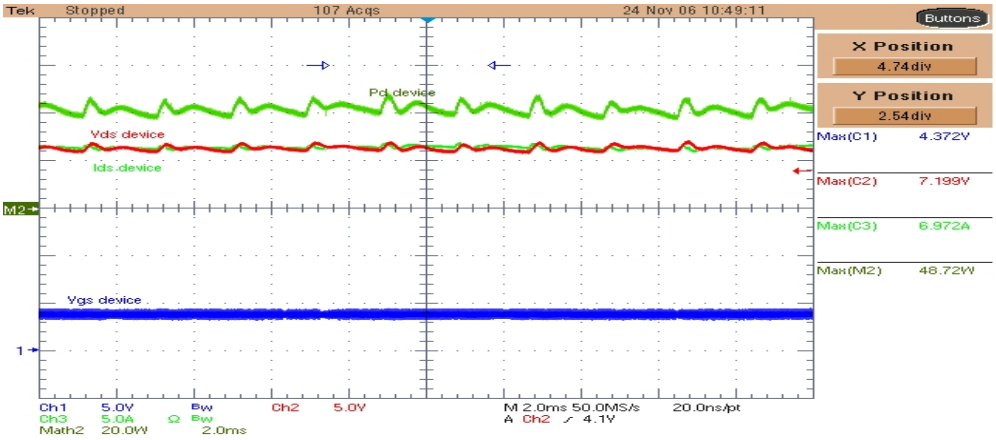


Fig.9

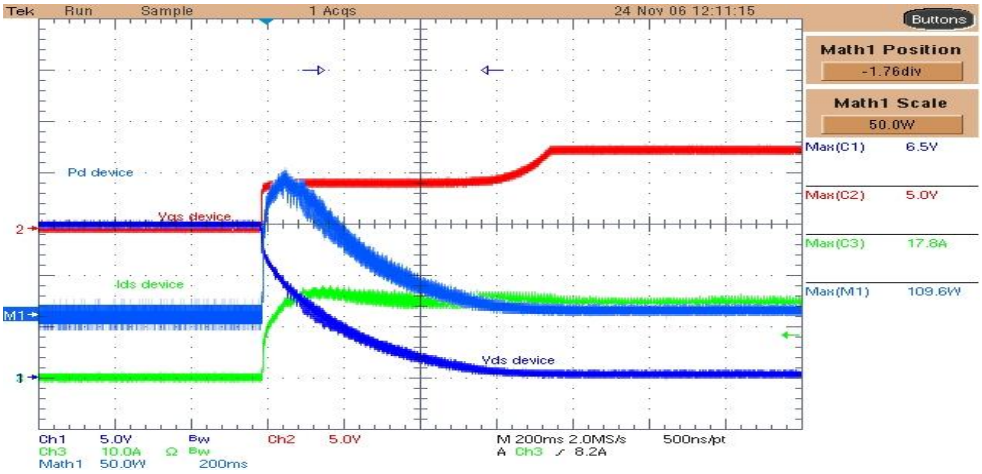


Fig.10

The duration of the test is 1 hour, without any failure and electrical parameter deviation. The start-up maximum power dissipation is 110 W, while in steady state conditions, the Power MOSFET is forced to manage an average power equal to 49 W.

4. Theoretical explanations

A deeper investigation [1, 2] about the gap in terms of thermal performances between the two different devices begins from a brief explanation of the Power MOSFETs electrical behavior in the so called “linear zone”. Under this working condition, the drain current is provided by the following formula:

$$I_D = \frac{1}{2} \cdot \mu \cdot \frac{W}{L} \cdot C_{OX} \cdot (V_{GS} - V_T)^2 = K \cdot (V_{GS} - V_T)^2 \qquad (1)$$

Where C_{OX} is the gate oxide capacitance, μ is the electron mobility, W and L respectively the channel width and length and $K = \frac{1}{2} \cdot \mu \cdot \left(\frac{W}{L} \right) \cdot C_{OX}$. So, the drain current is independent on the drain-source voltage. Under these conditions, the drain current thermal coefficient is:

$$\frac{\partial I_D}{\partial T} = \frac{\partial K}{\partial T} \cdot (V_{GS} - V_T)^2 - 2 \cdot K \cdot (V_{GS} - V_T)^2 \cdot \frac{\partial V_T}{\partial T} \qquad (2)$$

From (1) and (2), the following formula is obtained:

$$\frac{\partial I_D}{\partial T} = \frac{\partial K}{\partial T} \frac{I_D}{K} - 2 \cdot \sqrt{K} \cdot \sqrt{I_D} \cdot \frac{\partial V_T}{\partial T} \qquad (3)$$

As $\frac{\partial K}{\partial T}$ and $\frac{\partial V_T}{\partial T}$ (for V_{DS} = const.) are negative, if the second term is smaller than the first one, no failure occurs.

The drain current temperature coefficient is strictly related to the thermal management of a Power MOSFET. In fact, the power dissipation may be expressed as below:

$$V_{DS} I_D = \frac{\Delta T}{R_{thja}} \qquad (4)$$

If a power pulse is applied to the MOSFET, its temperature rise is related to the drain current temperature coefficient. The power dissipation variation is $V_{DS} \frac{\partial I_D}{\partial T}$; the device is able to manage the power dissipation until it reaches the failure point, which is expressed by the following formula:

$$V_{DS} \frac{\partial I_D}{\partial T} = \frac{\partial (\Delta T)}{\partial T \cdot R_{thj,a}} = \frac{1}{R_{thj,a}} \qquad (5)$$

Finally:

$$\left. \frac{\partial I_D}{\partial T} \right|_{I_D = \cos t} = \frac{1}{V_{DS} \cdot R_{thj,a}} \qquad (6)$$

is the maximum value of the drain current temperature coefficient before a failure. The previous formulas show that, for high V_{DS}, the device can fail even for low drain current. As a consequence, this phenomenon causes a slight variation of the boundary conditions in the SOA curve (for high V_{DS} and I_D).

The higher ruggedness of STripFET™ "linear proof" technology versus the standard technology ones can be explained using the previous formulas and the thermal coefficient curves. In fact, in fig.11, the thermal coefficient curves (normalized to the channel perimeter, W) of STP141NF55 and standard technology are compared. It is easy to see that the drain current temperature coefficient is higher for the std technology, than for the dedicated one, underlining a lower thermal ruggedness. Furthermore, the current range where $\frac{\partial I_D}{\partial T}$ is positive is smaller for the STP141NF55: in other words, the thermal stabilization takes place at lower drain current ($\frac{\partial I_D}{\partial T}$ sign inversion).

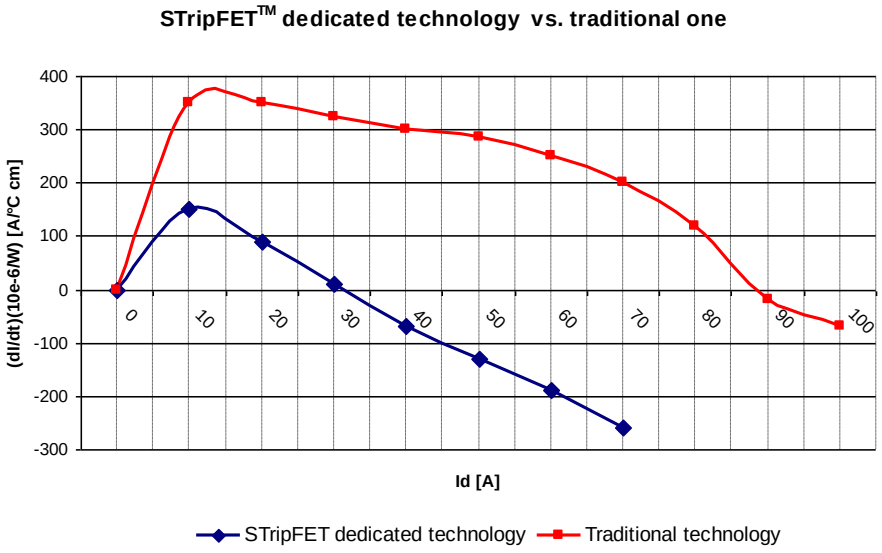


Fig.11

From looking at the previous formulas, one can see that the thermal coefficient is heavily affected by the negative derating of the threshold voltage when the device temperature increases. The relevant R_{DSon} increase is not enough to produce a self-limiting effect on the device current capability. Due to the electrical parameter mismatch of the single Power MOSFET elementary cell of the whole die surface and the process spread, a high current focalization occurs in a narrow portion of the active area. Figure 12 illustrates a typical example of a thermal runaway device that failed.

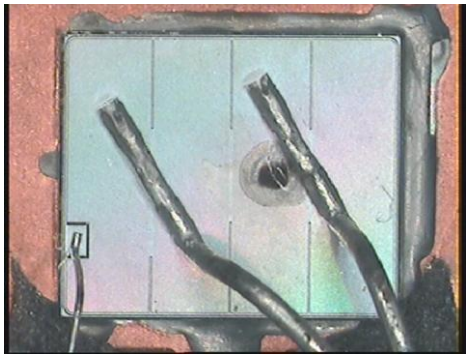


Fig.12

5. Conclusions

After having performed dedicated bench measurements and real system evaluations, the ***STripFET***^{TM} "linear proof technology" has been clearly identified to be suitable for linear mode applications. Thanks to its structural and process features, it matches more appropriately with the application needs (thermal runaway robustness), compared to the standard planar STripFET devices, as well as the standard Trench devices.

References

[1] : A. Consoli, F. Gennaro, A. Testa, G. Consentino, F. Frisina, R. Letor, A. Magri': "Thermal instability of Low Voltage Power MOSFETs", IEEE Transactions on Power Electronics, Vol.15,N.3, pp. 575-581

[2] : G. Consentino, G. Bazzano, "Investigations on electro-instability of low-voltage high current MOSFETs: theoretical models and experimental comparison results for different structures"

This paper was originally published at the APE 2007 conference