Design rules for paralleling of Silicon Carbide Power MOSFETs

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Abstract

Increasing the capability of a power switch by using several individual MOSFETs connected in parallel is a common practice with silicon semiconductor devices. This paper deals with the results of an investigation of the issues linked to paralleling the Silicon Carbide (SiC) MOSFETs. Based on the experimental validation of paralleled discrete devices the investigation focuses on the main electrical parameters affecting the performance of the paralleled switch. Moreover the influence of circuit mismatch on paralleling SiC MOSFETs is investigated as well as the impact of the "Kelvin source" connection that is tailored to mitigate the effects of not fully symmetric layout. A dedicated test vehicle has been developed to include all these aspects in the evaluation and carry out the tests on a switch element rated up to 300A.

1. Introduction

Wide Band Gap (WBG) materials such as SiC and Gallium Nitride (GaN) offer superior electrical and thermal properties. For the same voltage and current rating a SiC power semiconductor device offers smaller die area, higher operating temperature, higher operating frequency with lower switching losses compared to a Si power device. From the past years paralleling silicon MOSFETs in the 600V range is quite common; for higher voltage ratings IGBTs are massively used in parallel in several applications, even if with some big limitations inherent to the switching frequency. Hence SiC MOSFET is the first device facing the challenge of paralleling several individual transistors in very high voltage, very high frequency and high power applications. BUS voltage levels up to 950V in a frequency range extended above 200 kHz make critical MOSFETs paralleling and some special care must be taken in order to keep switching losses as low as possible. For the paralleled operation of power semiconductor devices, current unbalance is the main concern since it may cause unequal conduction loss and switching loss. Conduction losses unbalance represents a minor problem and it is not treated in the current work. However the steady-state current unbalance lead to unequal transient current distribution and can further result in higher losses unbalance and current overshoot in the

device. The current unbalance in paralleled power semiconductor devices arise mainly from two different areas related the first one to the device mismatch and the second one to the asymmetrical circuit layout. Among the device parameters of MOSFETs, the on state resistance ($R_{DS(on)}$) and the gate threshold voltage ($V_{GS(th)}$) have significant effect on the current sharing performance when paralleling MOSFETs both silicon and SiC ones. The aim of this paper, therefore, consists in defining the key parameters to ensure the goodness of the parallel connection as well as the most relevant aspects influencing paralleling SiC MOSFETs (device and circuit mismatch). The conclusions will be based on real tests performed inside STMicroelectronics laboratories on the second generation of ST SiC MOSFETs featuring extremely low $R_{DS(on)}$x Q_g Figure-of-Merit.

2. Consequences of unideal paralleling in the application

There are several possible causes for current unbalance that may result in a particular device exceeding its peak current or continuous thermal ratings. Unbalance my be generated by device parameter mismatch, gate driver mismatch, power circuit mismatch or by, more close to reality, a variable mix of these ones.

2.1. Device parameters mismatch

Due to manifacturing intrinsic tolerances when paralleling two or more SiC MOSFET the total current is generally not equally balanced among the devices. In the following some consideration on the main souce of unbalance: the on state resistance ($R_{DS(on)}$) and the gate threshold voltage ($V_{GS(th)}$).

2.1.1 $R_{DS(on)}$ mismatch

From simple considerations on parallel resistances calculation if we consider a couple of device having a 20% $R_{DS(on)}$ variance respect to the typical data-sheet value, the device having lower $R_{DS(on)}$ should carries, during conduction state, a current that is 1.5 times greater than the one having higher $R_{DS(on)}$. So the two device switches different current levels leading to different losses.

As a measure of this Fig.1 reports an example of how turn-off losses are not equally shared between two, 1200V 50A, paralleled devices selected with very similar electrical characteristics ($V_{(BR)DSS}$ $V_{GS(th)}$ ...) but having $R_{DS(on)}$ which differs ±20% from the typical value.

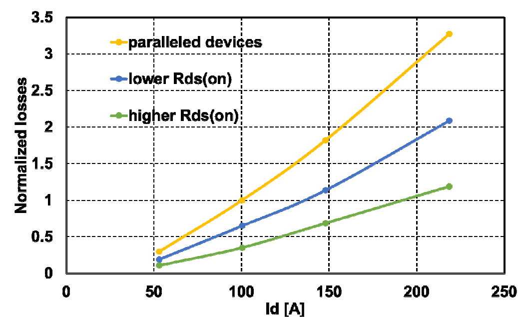

Figure 1 Normalized turn-off losses for paralleled devices, lower Rds(on) device and higher Rds(on) device

Such effect is partially compensated by SiC MOSFET temperature characteristic. For temperature range of interest in common application, SiC MOSFET devices have Positive Temperature Coefficient (PTC) characteristic. Similarly to a Si MOSFET the higher the junction temperature the less will be the shared current for paralleled parts leading in the end to a thermal equilibrium. Fig. 2 reports the normalized $R_{DS(on)}$ vs temperature for the STMicroelectronics current generation of high voltage SiC MOSFET.

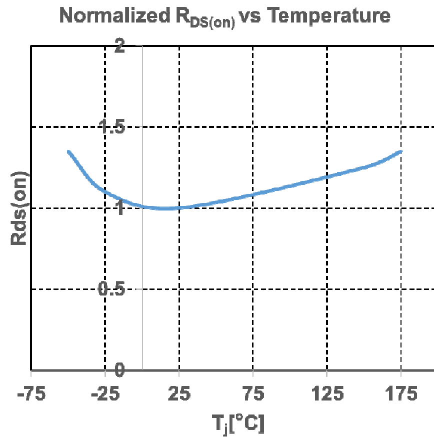

Figure 2 normalized $R_{DS(on)}$ vs Temperature

2.1.2 $V_{GS(th)}$ mismatch

In addition to the conduction losses, whose unbalance can be mitigated by the $R_{DS(on)}$ PTC characteristic, switching losses unbalance have to be considered. The $V_{GS(th)}$ variance causes the device with the lower one to switch-on earlier and switch-off later than the other with higher $V_{GS(th)}$. The overall energy could be not equally distributed among the paralleled devices even if some precautions, like using device with the same $R_{DS(on)}$ and a common heatsink for temperature negative feedback, have been adopted.

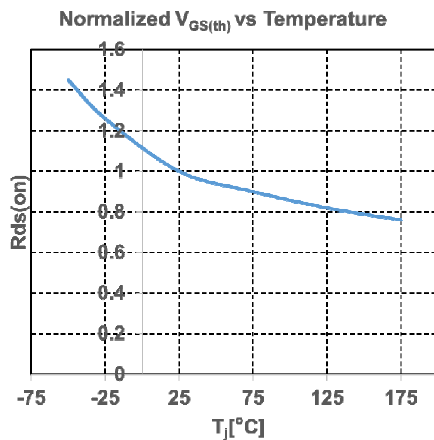

Figure 3 normalized $V_{GS(th)}$ vs Temperature

Due to the Negative Temperature Coefficient (NTC) characteristic of $V_{GS(th)}$ (Fig. 3) the initial threshold difference can increase enhancing the switching losses difference and thus the risk of thermal runaway is not negligible especially when switching losses predominate over conduction ones.

Fig. 4 reports an example of how turn-off losses are not equally shared between two, 1200V 50A, paralleled devices selected with the same electrical characteristics ($V_{(BR)DSS}$, $R_{DS(on)}$...) but having $V_{GS(th)}$ which differs 700mV from each other.

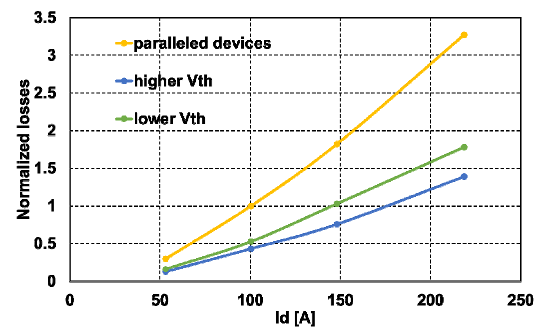

Figure 4 Normalized turn-off losses for paralleled devices, lower $V_{GS(th)}$ device and higher $V_{GS(th)}$ device.

2.2. Gate driver mismatch

The dimensioning of the gate circuit is the result of a compromise between the necessity of fast switching to minimize power losses and the need of avoiding possible oscillations. Once fixed the voltage swing, the positive value for the desired $R_{DS(on)}$ and the negative one for noise immunity, the gate Rg values and topology have to be selected in an appropriate manner.

Fig. 5 reports 3 possible choices for gate topology: (a) all the gates are linked togheter and there is only one gate resistor, (b) each device has a separate gate resistance so each one is indipendently driven, (c) is a mix of the previous two trying to get the best of both.

The (a) solution is less sensitive to dynamic unbalance because of the gate all tied togheter, but is susceptible of high frequency oscillations, due to equivalent RLC gate series resonant circuit, even if the internal gate mesh resistor could be sufficient for damping oscillations. The (b) solution, where the gates are strongly decoupled, can cause both current and transition energy unbalance. A trade-off solution is achievable using the (c) topology that allows minimizing parasitic oscillations without significantly increase the dynamic unbalance.

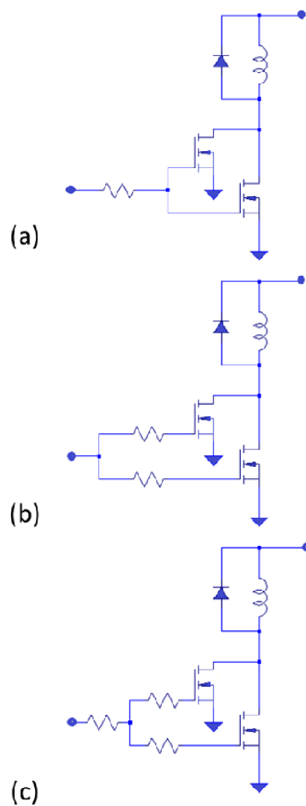

Figure 5 gate resistance topology having fully gate decouping (a), no gate decoupling (b) and partially gate decoupling (c)

2.3. Power circuit mismatch

Considering the power circuit external to paralleded devices a possible source of unbalance is due to layout. The presence of differential parasitic inductance in the drain and/or source path, as reported in

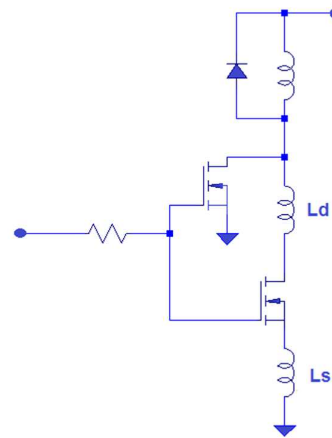

Figure 6 external circuit unbalance due to drain, Ld, and source, Ls, parasitic inductances

Fig. 6 as an example for two devices, is to be minimized The primary cause of unbalance is related to the Ls being the Ld inductance less influent. Ld generally can lead to a negligible current unbalance amount even if the differential drain–source voltage is not so negligile with conseguent losses unbalance. The Ls inductance acts as a negative feedback whenever the drain current of the device changes: the faster the dI/dt the higher the negative feedback opposing the gate voltage. The package internal wiring and the inductance associated with the interconnections should be minimized for faster switching and simmetrically designed for limiting unbalance when paralleling devices. But due to some layout constraints the design of symmetrical source inductance is not always feasible so the effect of Ls mismatch has to be reduced with a combined approach. It is necessary, as far as possible, to have a symmetric layout and in addition to adopt an auxiliary source connection bond-wire: the Kelvin contact (Fig.7). In this way the gate signal is totally applied to the device without any loss due to Ls feedback. The feedback amount, i.e. the voltage on the stray Ls inductance, is due not only to the Ls value itself but also to the di/dt of the source current which can be quite different from one device to the other one. The adoption

of kelvin contact will speed-up the device minimizing losses but it do not assure the current balance.

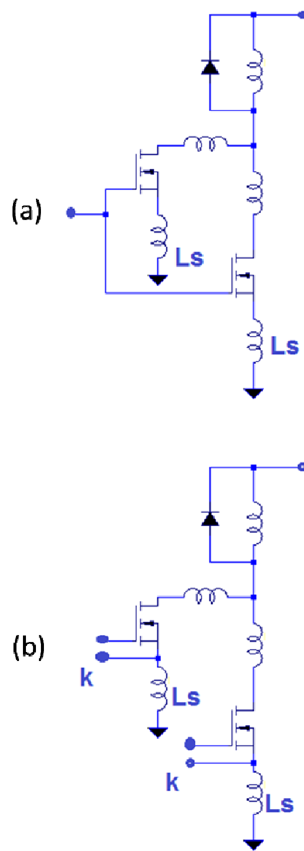

Figure 7 gate circuit topology with (b) and without (a) kelvin contact

What each power application designer ideally expects from paralleling any kind of Power MOSFET consists in easily multiplying the energy of a single transistor by the number of paralleled ones. For instance, connecting in parallel two MOSFETs, each one dissipating around 3000µJ Eoff at 200A as a stand-alone switch, we expect the total energy of the parallel connection to be just twice the single MOSFET energy (i.e. 6000µJ at 400A). Unfortunately, due to the non-ideality of the parallel connection the overall energy is higher than the energy of the single, so leading to lower efficiency. Moreover, due to the current unbalance, the overall energy could be not equally distributed among the paralleled devices, in this way the risk of thermal runaway is not negligible especially when switching losses predominate over the conduction ones. The practical consequence of such behavior consists in some constraints to the maximum power manageable at very high frequency. For instance in DC-DC converter paralleling can be useless since switching losses represent up to 90% of total losses and switching losses in any case increase when paralleling, thus paralleling just allows the heat sharing at the condition that unbalance is minimized.

In the following Fig. 8 the result of a case study is reported.

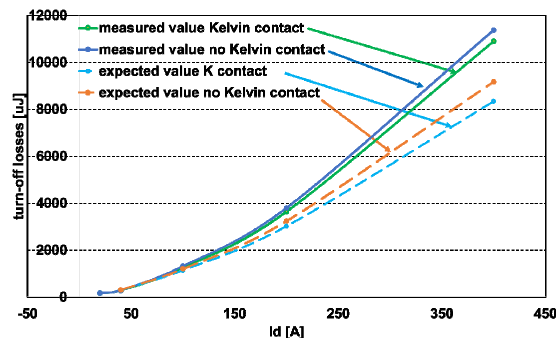

Figure 8 expected energy losses, from single device losses measurement, vs real energy losses using the same paralleled devices

Two 200A, 650V device have been tested and each single turn-off energy vs drain current measured with and without kelvin contact. Then the devices have been paralleled and the measurement repeated. The dotted lines in Fig. 8 reports the algebraic sum of the measured single device energy loss, with and without kelvin contact. The continuous lines represent the measured energy loss for the paralleled devices.

From the graph analysis arises the beneficial effect of kelvin contact in terms of total energy dissipation but the energy loss of the paralleled device is, as the drain current increases, greater than 20% compared to the sum of the single devices.

3. Resuming Considerations

From the above discussion some guidelines, according to the specific situation, i.e. the acceptable level of unbalance depending on the application, the working frequency and duty-cycle, should be adopted.

- $R_{DS(on)}$ is the main parameter to consider for steady-state current balance; it also influences the dynamic losses because of different current levels during switching
- $V_{GS(th)}$ and transconductance are effective for dynamic current balance
- Matching the Ls source inductance is effective to balance dynamic current losses while using kelvin contact helps in their reduction
- The drain stray inductances Ld are not effective in current unbalance while greatly influences the energy losses
- The value of the decoupling gate resistors mesh have to be carefully selected to minimize parasitic oscillations without significantly increase the dynamic unbalance.

4. Conclusions

The test results performed in an inductive load test circuit show that the total turn-off energy of paralleled SiC MOSFETs typically increase more than expected when several dice are paralleled. Moreover such increase is linked to several not completely independent parameters. The maximum allowed gap between real and ideal behavior must be translated in some specific limits to the device and layout mismatch being in the end the main responsible for unideal paralleling operation. Finally a trade-off between switching frequency and cost must be found since especially reducing the device parameters distribution and managing the device mismatch could be expensive and, depending on the application, not necessary.

5. References

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