List of software parameters to check in case of switch:

From M24C32S-FCU to M24128X-FCU

Information

- This document provides a list of software parameters to check in case of switch from M24C32S-FCU to M24128X-FCU.

List of software parameters to check

Parameter	M24C32S-FCU	M24128X-FCU	Action needed	Remarks
Datasheet	M24C32S-FCU	M24128X-FCU	FYI	Available on ST.COM web site : - M24C32S-FCU - M24128X-FCU
Max address	0FFFh	3FFFh	Yes	If the application uses the sequential read instruction, on the M24128X the next address after 0FFFh will be 1000h and roll over will continue up to 3FFFh. After 3FFFh, the next address pointed will be 0000h. Read & write command must take in account the A13 MSB address.
Chip enable address	Fixed : 001	Default : 000	Yes	At factory delivery not compatible but M24128X offers the configurable chip enable address C2,C1,C0 (factory delivery value = 000). The chip enable address (C2,C1,C0) can be modified in the chip enable register. The register can be written & read with specifics command “write chip enable register“ & “read chip enable register“.
Software Write Protect register	Available (Protection by quarter)	Available (Protection of full plan)	Yes	M24C32S offers the software write protection by quarter with the *write protect register*. M24128X offers the software write protection on the entire memory(not by quarter) with *the chip enable register*. Same address for both register (1xxx.xxxx.xxxx.xxxx) On M24128X, the software write protection is managed by SWP bit only. When SWP=0, the memory is not protected against update. When SWP=1 the memory is fully protected against update. Updating the SWP to a new value is a reversible action.
Chip enable register management	Not Available	Available	Yes	With the M24128X, the user writes & reads the *chip enable register* with the specific commands “write chip enable register” & ”read chip enable register”. Can be updated: - The C2,C1,C0 bits for the chip enable address - The SWP bit for the protection of the memory array

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