
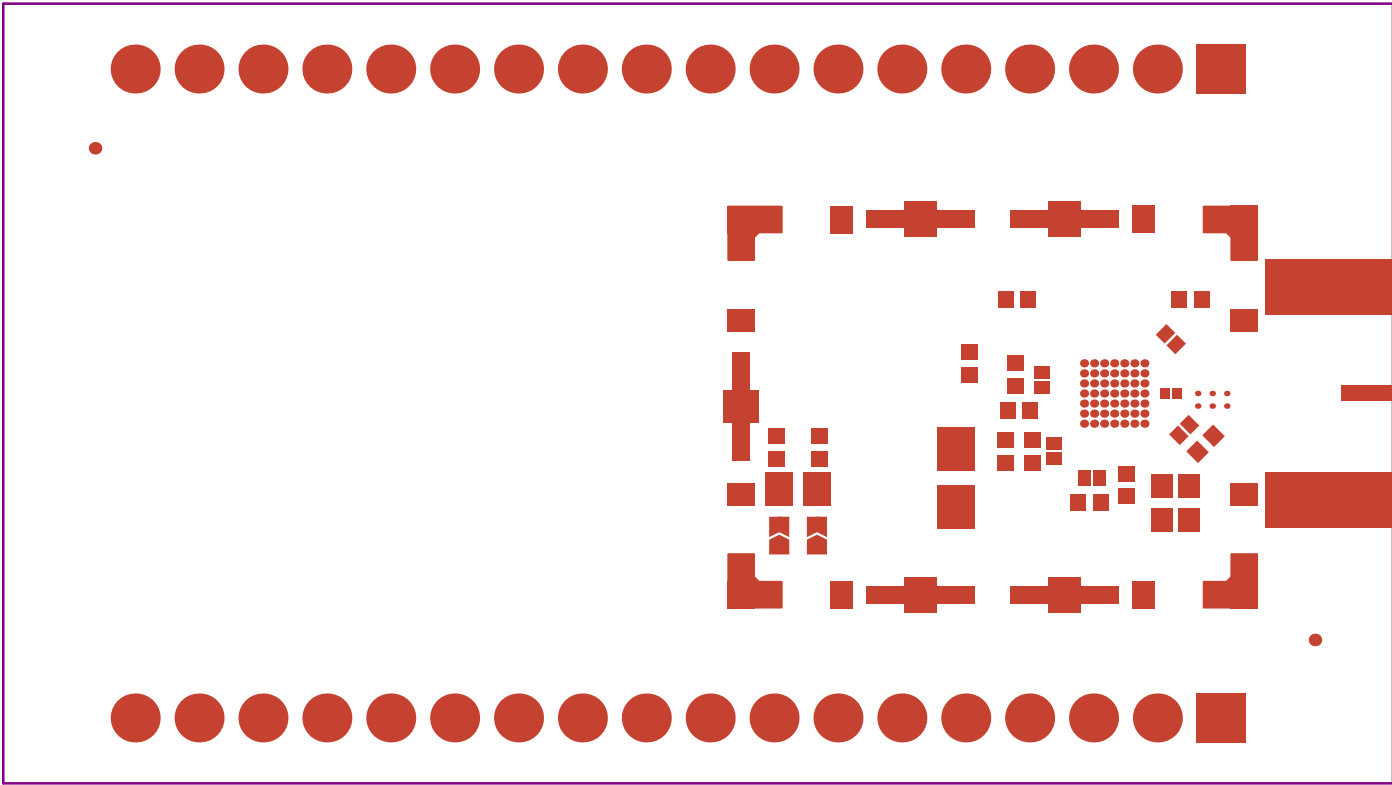

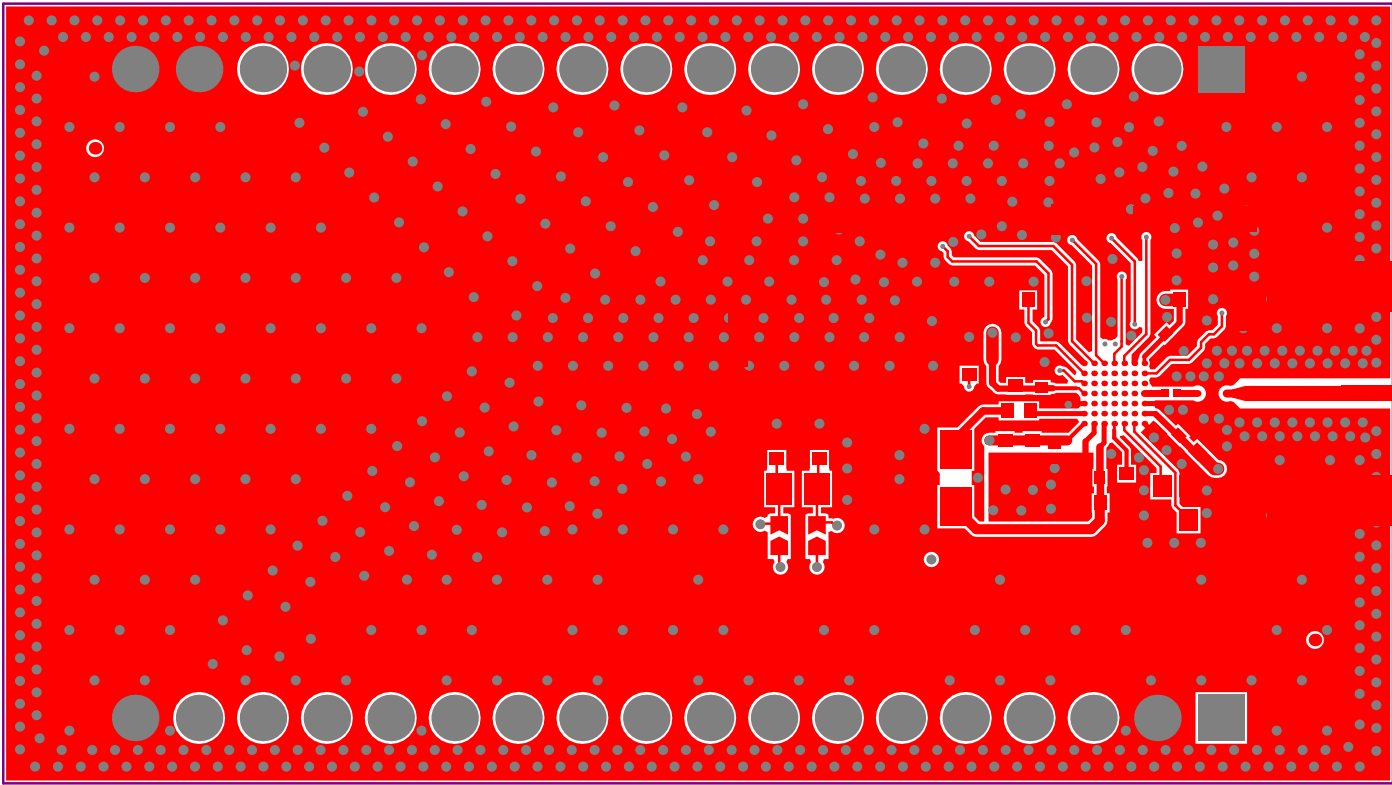



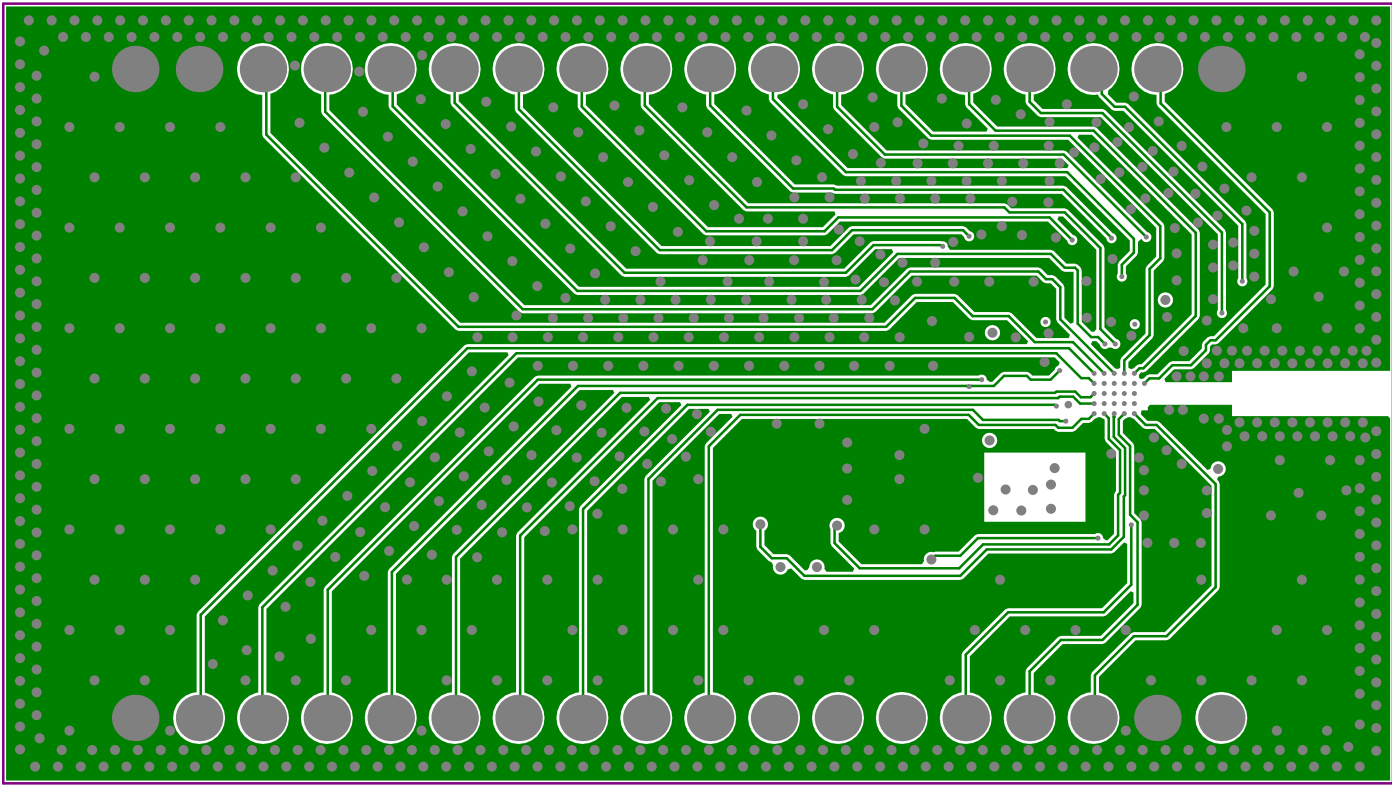
Project: STM32WB07_WLCSP49_4L_IPD		
Layer: Top Overlay	Gerber: .GTO	
Variant: [No Variations]	Ref: MB2270	
Date: 26 August 2025	Rev: A	




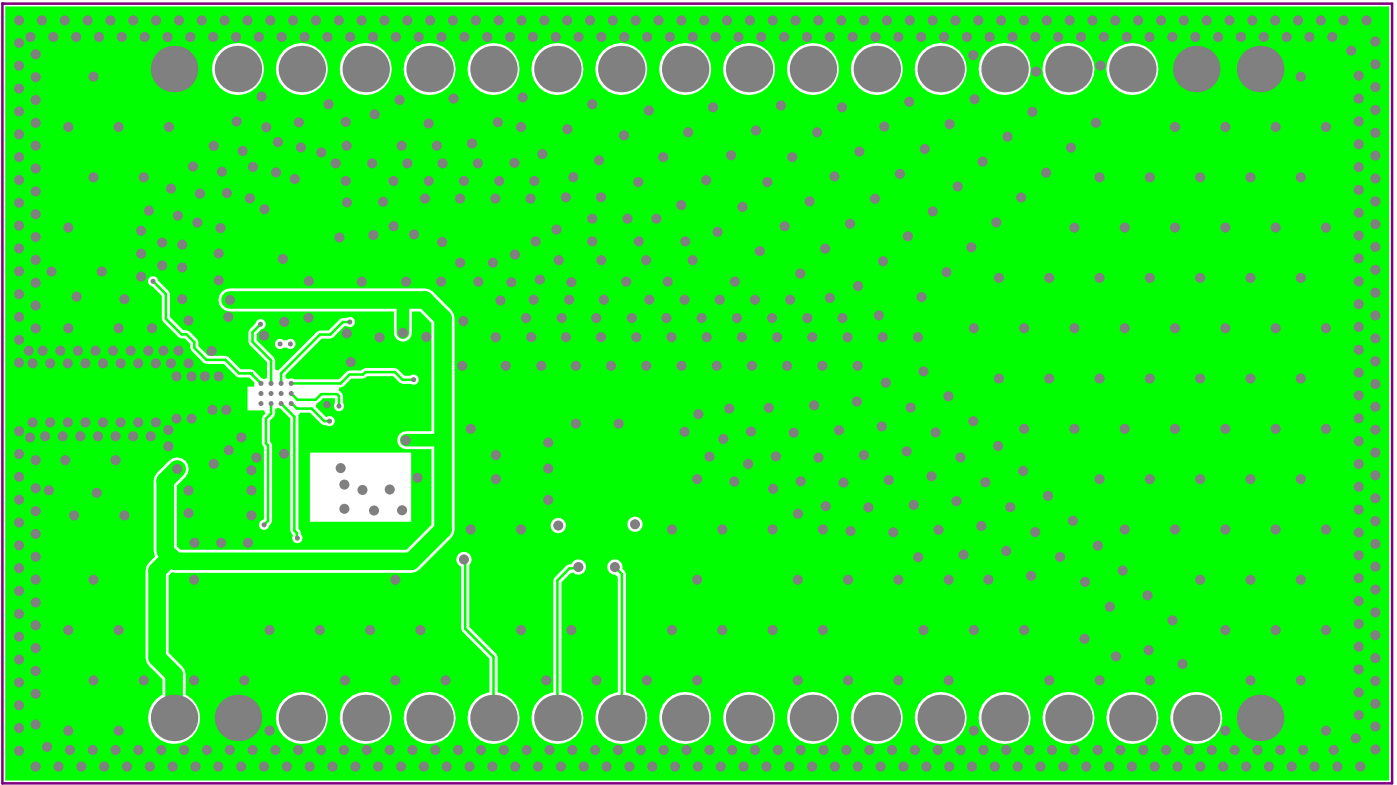
Project: STM32WB07_WLCSP49_4L_IPD		
Layer: Top Solder	Gerber: .GTS	
Variant: [No Variations]	Ref: MB2270	
Date: 26 August 2025	Rev: A	




Project: STM32WB07_WLCSP49_4L_IPD		
Layer: Top Layer	Gerber: .GTL	
Variant: [No Variations]	Ref: MB2270	
Date: 26 August 2025	Rev: A	



Project: STM32WB07_WLCSP49_4L_IPD		
Layer: Layer 1	Gerber: .G1	
Variant: [No Variations]	Ref: MB2270	
Date: 26 August 2025	Rev: A	



Project: STM32WB07_WLCSP49_4L_IPD		
Layer: Layer 2	Gerber:.G2	
Variant: [No Variations]	Ref: MB2270	
Date: 26 August 2025	Rev: A	

Gerber File List

Gerber files are used to define the physical layout of a printed circuit board (PCB). They specify the dimensions, shapes, and positions of various components on the board, including copper layers, solder mask, and components like vias, pads, and components.

The Gerber files are typically organized into a directory structure, with each file representing a specific layer or component of the PCB. The files are usually named with a prefix indicating the layer or component type, followed by a unique identifier.

For example, the Gerber files for a PCB might include:

- Top Layer (e.g., TopLayer.GBL)
- Bottom Layer (e.g., BottomLayer.GBL)
- Internal Layers (e.g., InternalLayer1.GBL, InternalLayer2.GBL)
- Drill Files (e.g., DrillFiles.GBL)
- Component Files (e.g., Components.GBL)

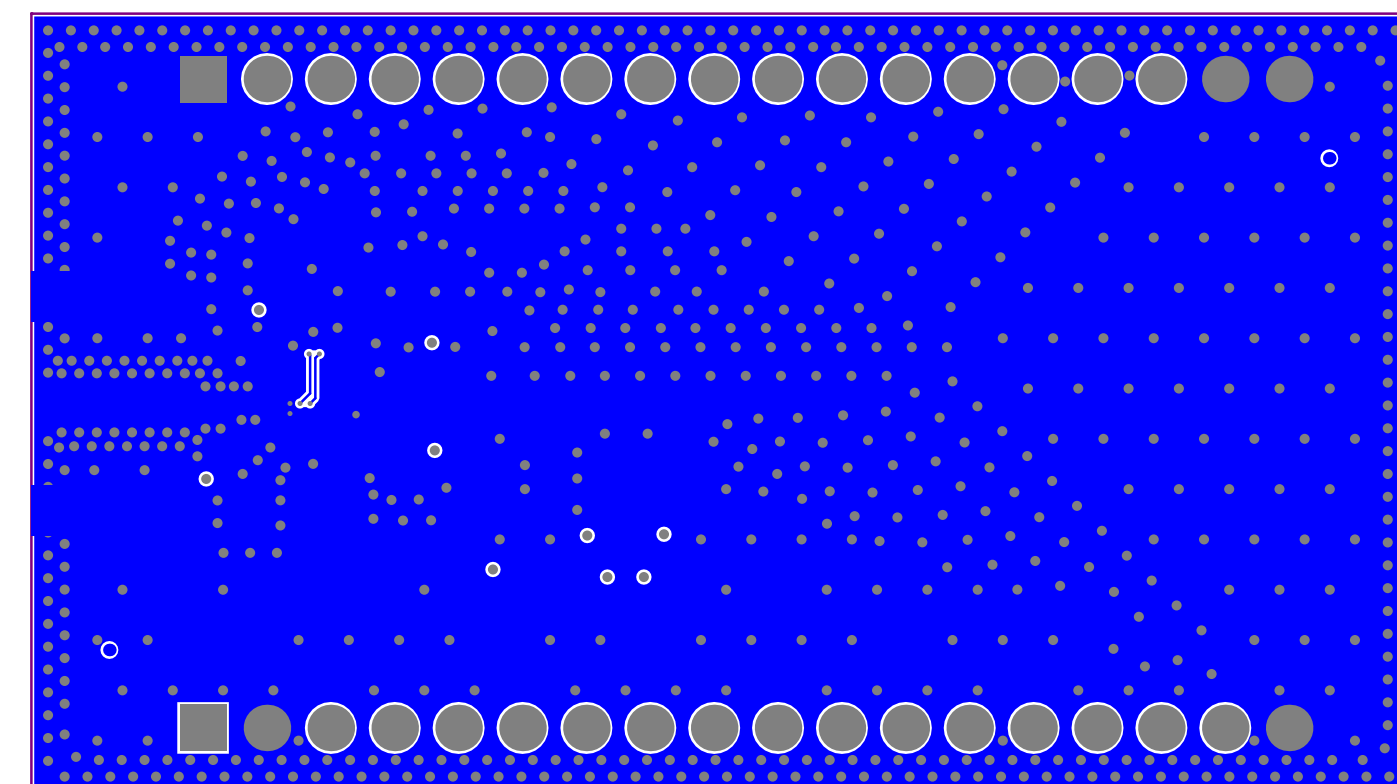
The Gerber files are used by the PCB manufacturer to create the physical board. They provide the necessary information for the manufacturer to fabricate the board accurately, ensuring that all components are placed correctly and the board meets the required specifications.


The Gerber files are also used for quality control and verification. They allow the manufacturer to check the board's dimensions and shapes against the design specifications, ensuring that the board is manufactured correctly.

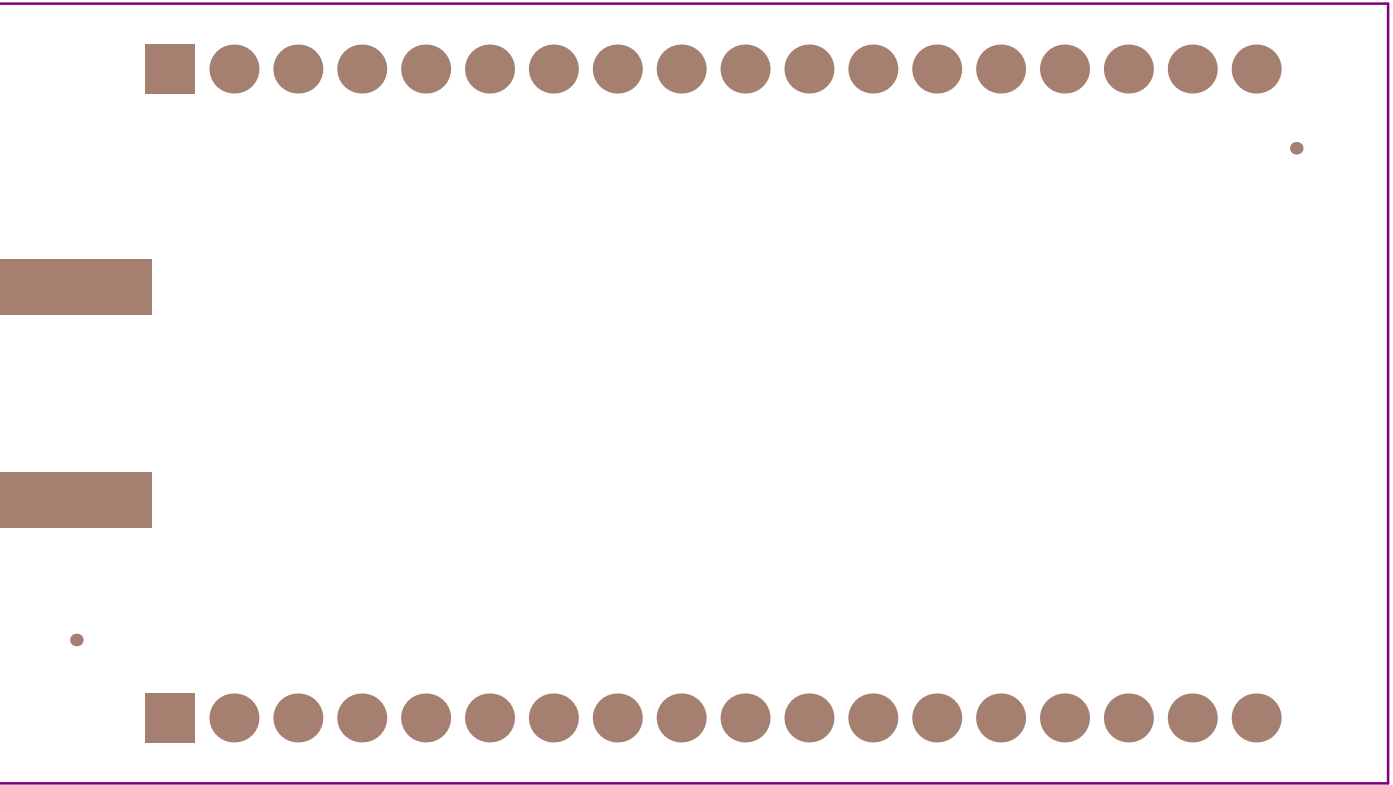
The Gerber files are a critical part of the PCB design process, providing the necessary information for the manufacturer to create the physical board. They are used to define the physical layout of the board, ensuring that all components are placed correctly and the board meets the required specifications.

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Project: STM32WB07_WLCSP49_4L_IPD		
Layer: Bottom Layer	Gerber:.GBL	
Variant: [No Variations]	Ref: MB2270	
Date: 26 August 2025	Rev: A	



Project: STM32WB07_WLCSP49_4L_IPD

Layer: Bottom Solder

Gerber:.GBS

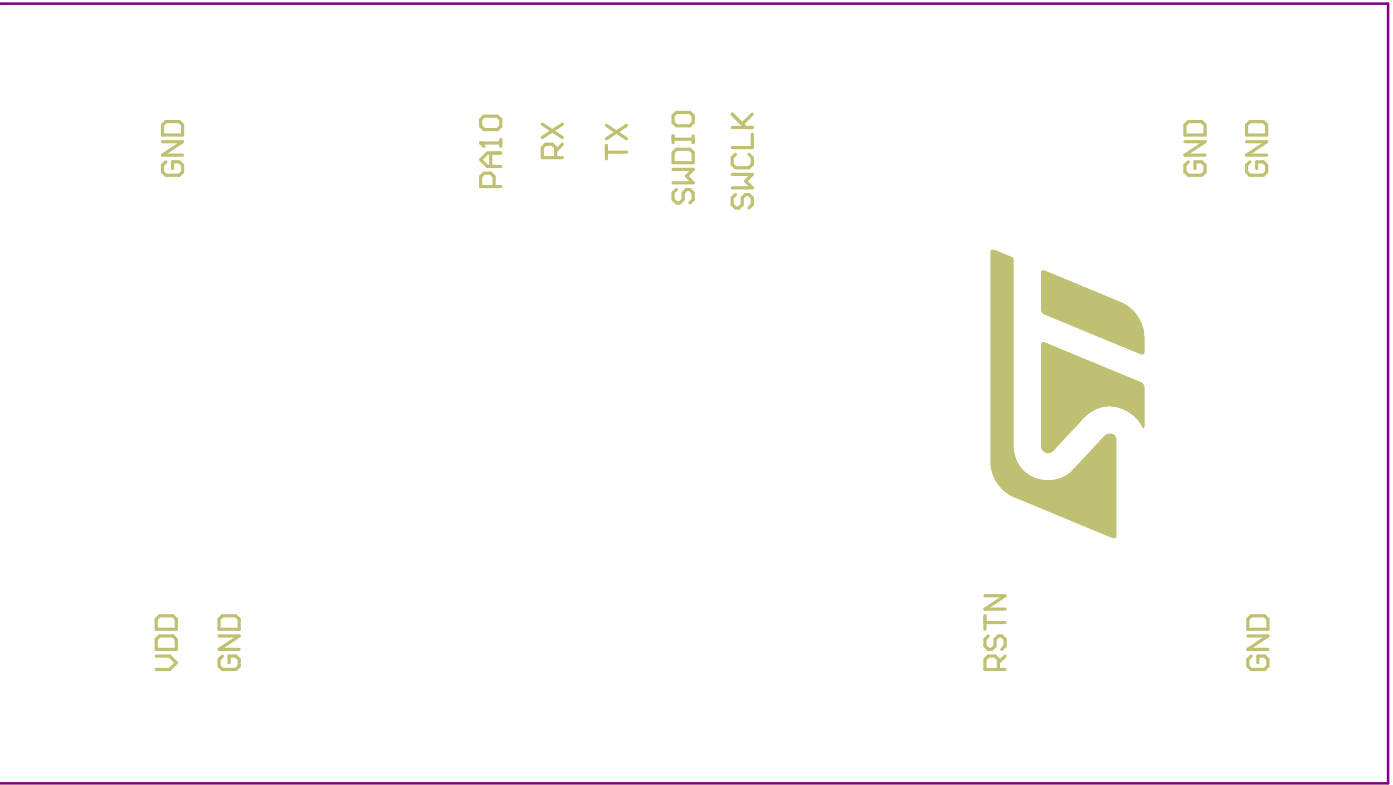
Variant: [No Variations]


Ref: MB2270

Date: 26 August 2025

Rev: A





Project: STM32WB07_WLCSP49_4L_IPD		
Layer: Bottom Overlay	Gerber:.GBO	
Variant: [No Variations]	Ref: MB2270	
Date: 26 August 2025	Rev: A	

Symbol	Count	Hole Size	Plated	Hole Type	Drill Layer Pair	Via/Pad	Pad Shape	Template
✳	1	0.150mm (5.91mil)	PTH	Round	Top Layer - Bottom Layer	Via	Rounded	v30h15m0mx0
□	36	1.000mm (39.37mil)	PTH	Round	Top Layer - Bottom Layer	Pad	Rounded	(Mixed)
○	45	0.100mm (3.94mil)	PTH	Round	(Mixed)	Via	Rounded	(Mixed)
▽	846	0.200mm (7.87mil)	PTH	Round	Top Layer - Bottom Layer	Via	Rounded	(Mixed)
	928 Total							

PCB SPECIFICATIONS :

A. MATERIAL :

B. MATERIAL FAMILY :

C. SOLDERMASK COLOR :

D. SILKSCREEN COLOR :

E. SURFACE FINISH :

F. IMPEDANCE CONTROL :

G. THROUGH VIA :

H. STACK-UP :

FR-4

N/A

☒ GREEN

☐ BLUE

☐ RED

☐ BLACK

☒ WHITE

☐ YELLOW

☐ BLACK

☒ ENIG

☐ IMMERSION SILVER

☐ IMMERSION TIN

☐ HASL

☐ HASL (PB-FREE)

☐ GOLDEN FINGER

☐ NO

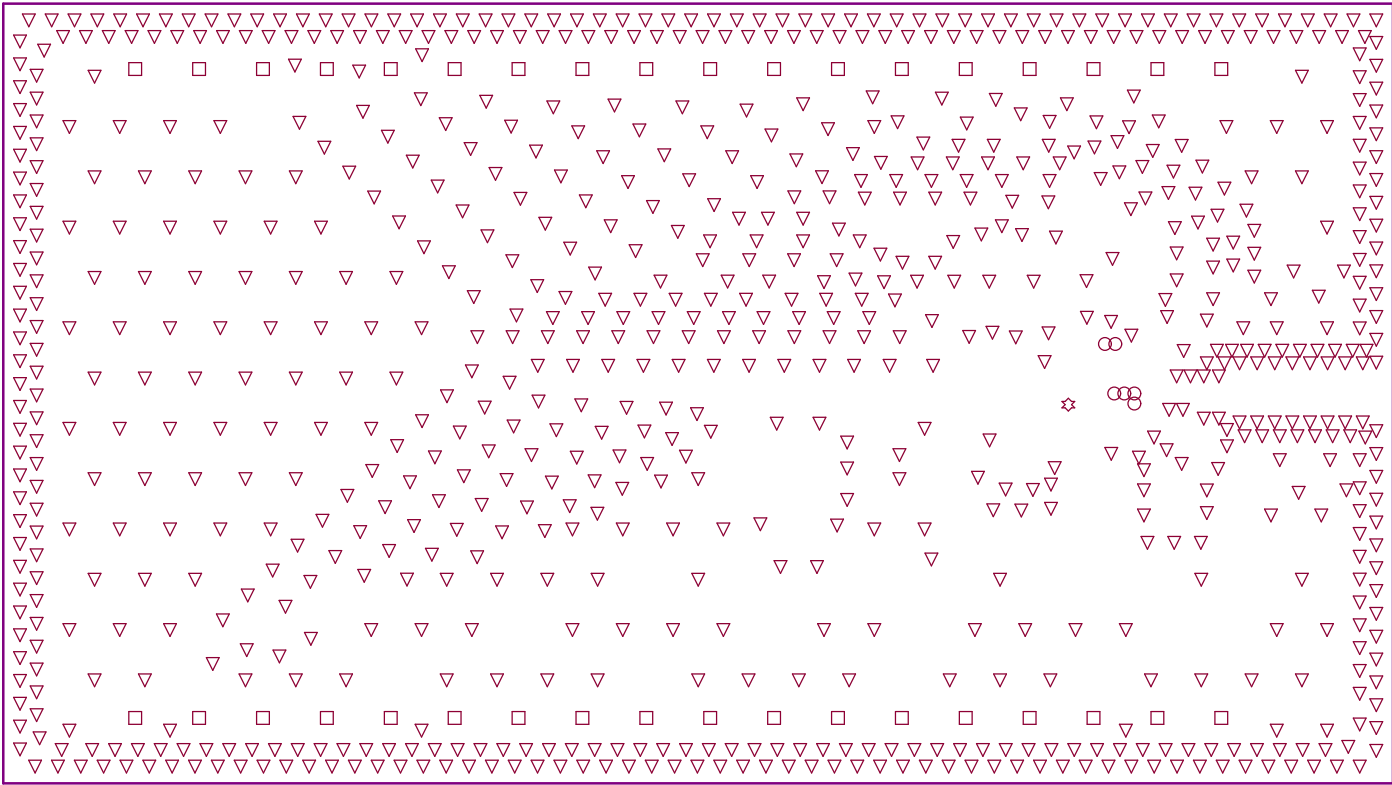
☒ YES (SEE IMPEDANCE TABLE FOR DETAIL INFORMATION)

PLUG THE VIAS WHICH ARE COVERED WITH SOLDERMASK ONE OR TWO SIDE.


PLUG MATERIAL :

☒ SOLDERMASK☐ NON-CONDUCTIVE EPOXY.

SEE LAYER STACK-UP SEQUENCE FOR OVERALL THICKNESS.



Layer	Name	Material	Thickness	Constant
	Top Overlay			
	Top Solder	Solder Resist	0.020mm	3.5
1	Top Layer		0.035mm	
	Dielectric 2	TU-768 (1x2113)	0.102mm	4.2
2	Layer 1		0.035mm	
	Dielectric 1	TU-768 (2x2116)	0.254mm	4.3
3	Layer 2		0.035mm	
	Dielectric 3	TU-768 (1x2113)	0.102mm	4.2
4	Bottom Layer		0.035mm	
	Bottom Solder	Solder Resist	0.020mm	3.5
	Bottom Overlay			

Project: STM32WB07_WLCSP49_4L_IPD		
Layer: Drill Drawing	Gerber: .DRL	
Variant: [No Variations]	Ref: MB2270	
Date: 26 August 2025	Rev: A	

IMPEDANCE TABLE					
LAYER	TRACE	SPACING	IMPEDANCE (Single ended)	IMPEDANCE (Differentiel)	TOL.
TOP	0.6	0.3	50 ohm	NA	+/- 5%
TOP	0.275	0.135	57 ohm	NA	+/- 5%