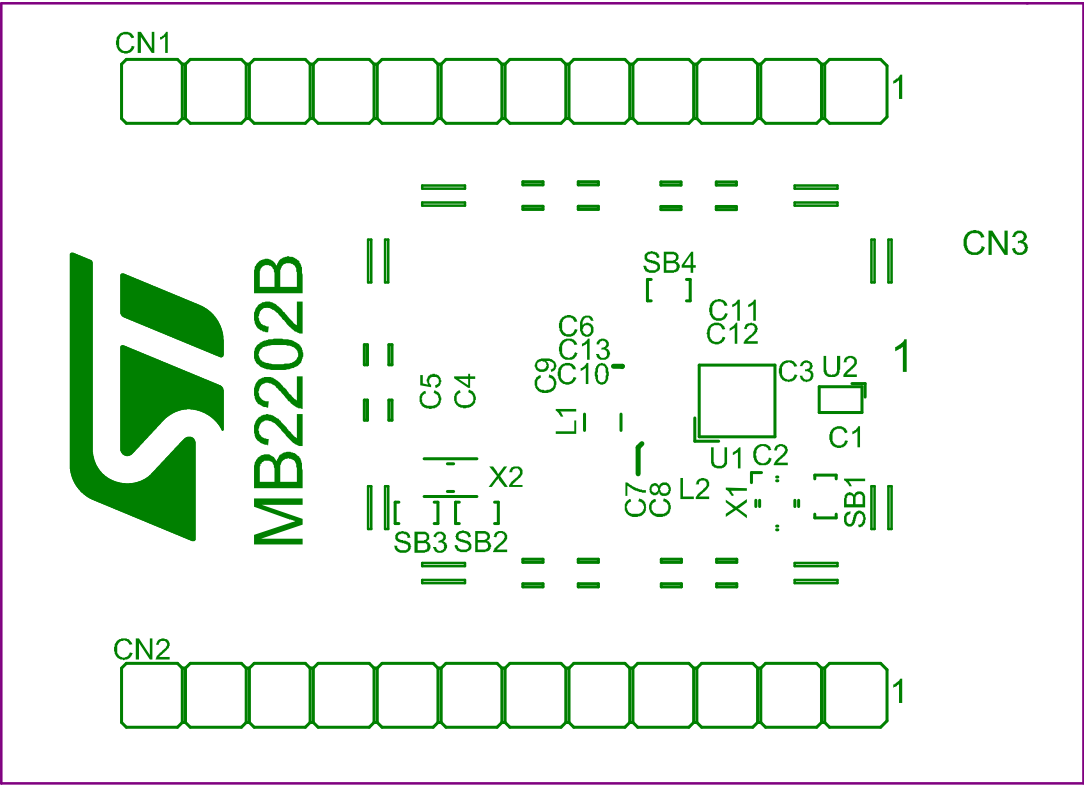
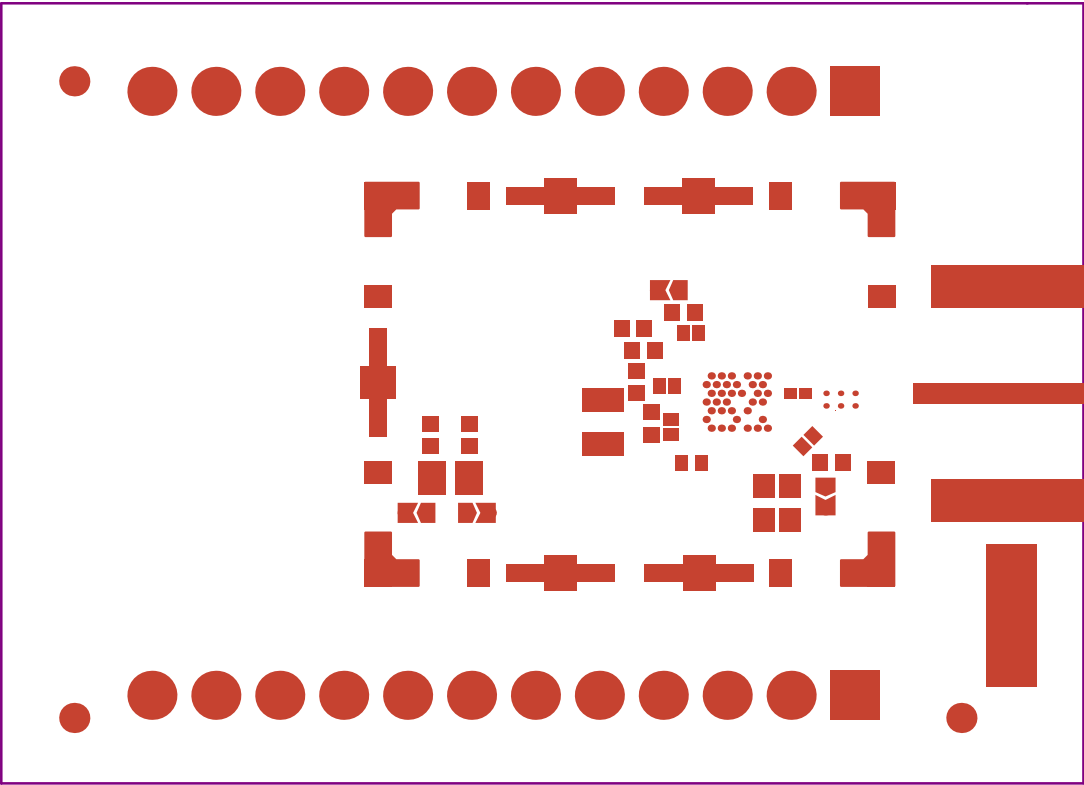
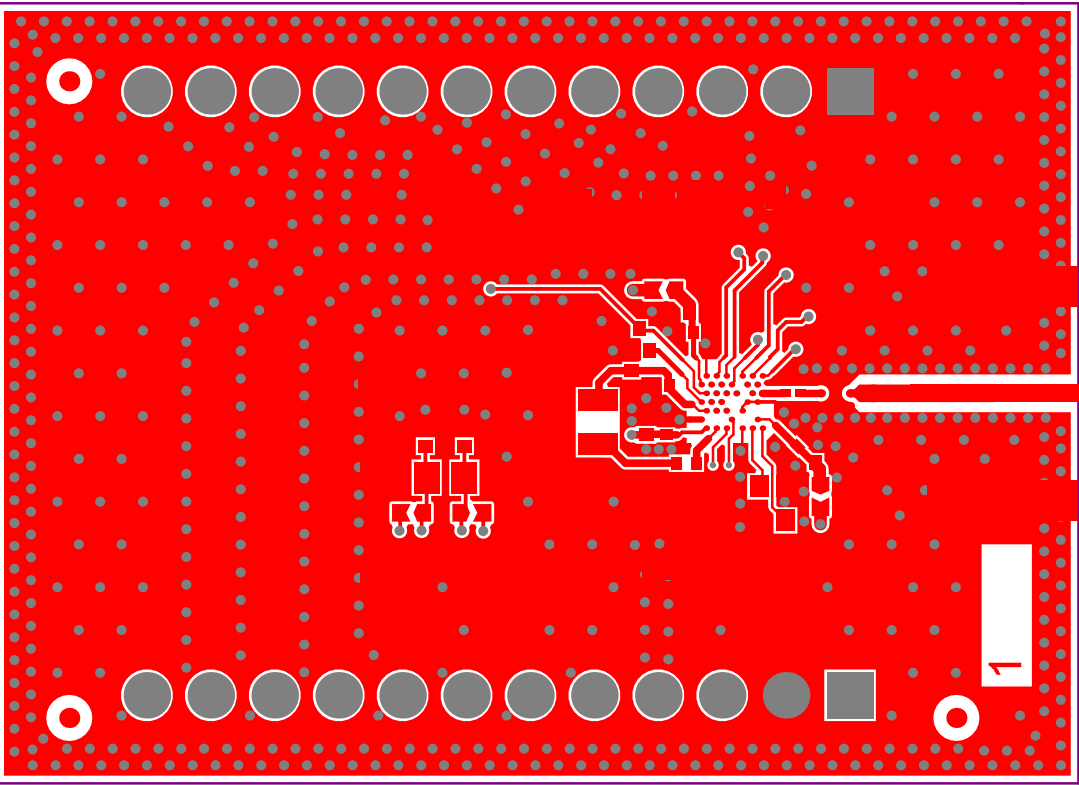




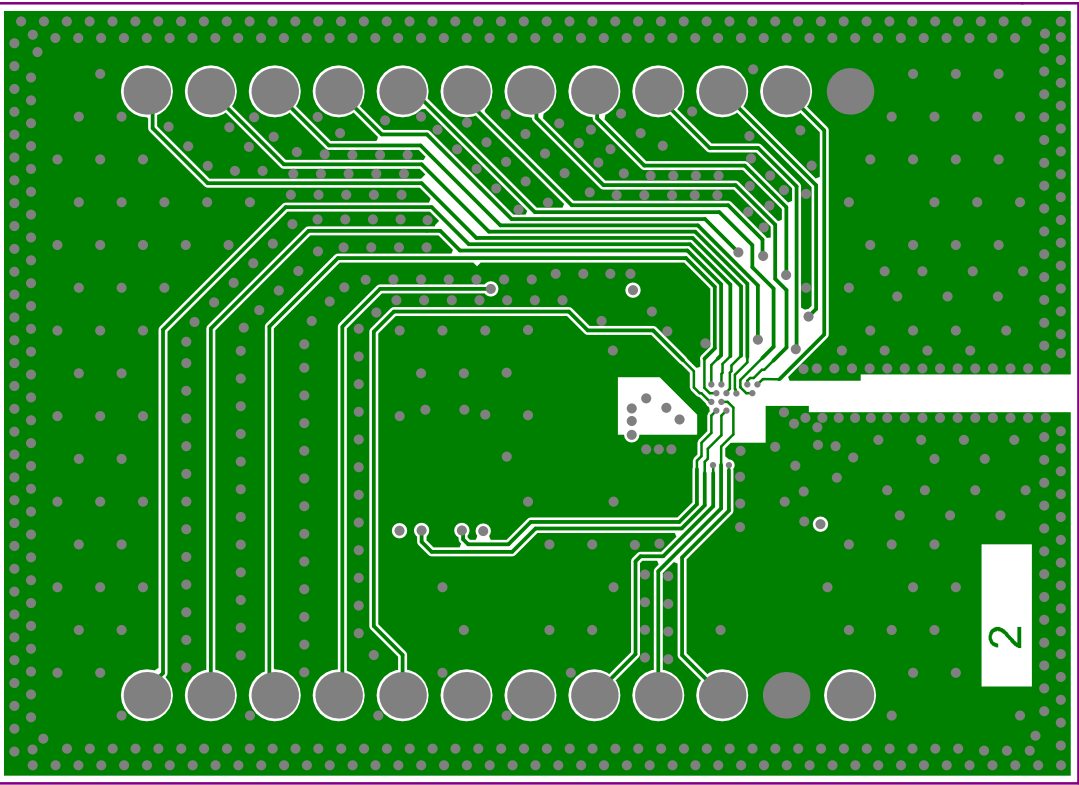
Project: Reference design for STM32WB09TEF - IPD		
Layer: Top Overlay	Gerber: .GTO	
Variant: [No Variations]	MB2202	
Date: 18-12-2025	Rev: B	



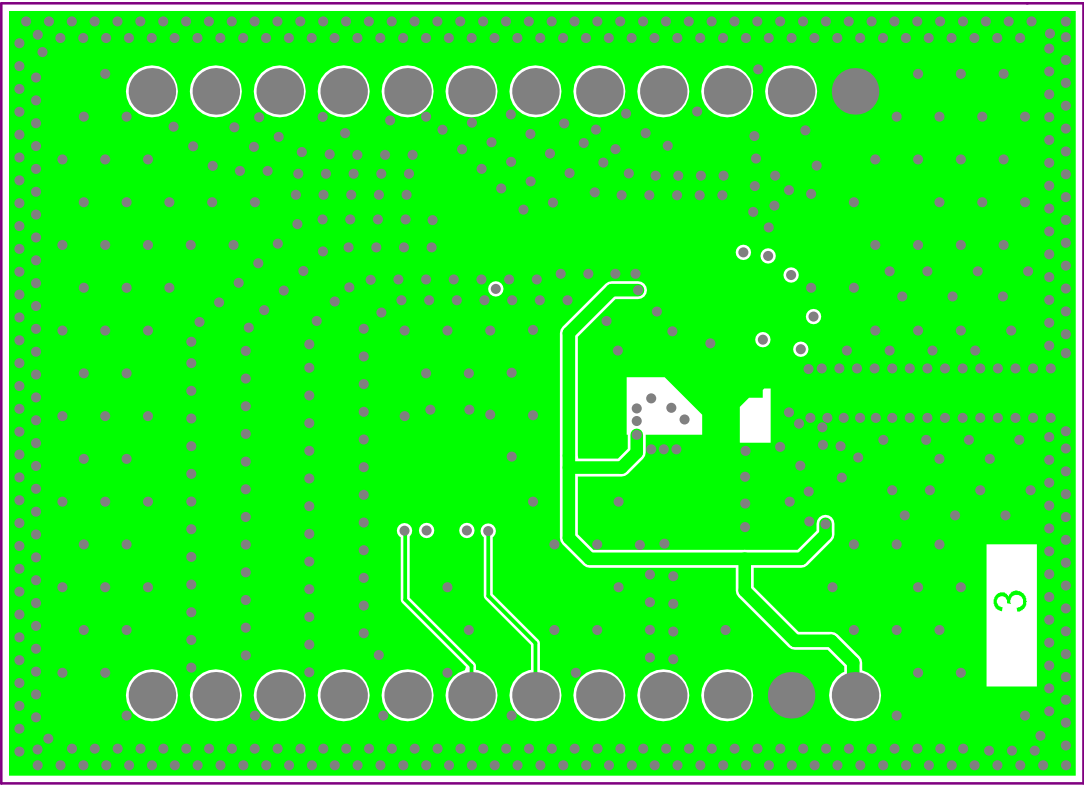
Project: Reference design for STM32WB09TEF - IPD		
Layer: Top Solder	Gerber: .GTS	
Variant: [No Variations]	MB2202	
Date: 18-12-2025	Rev: B	



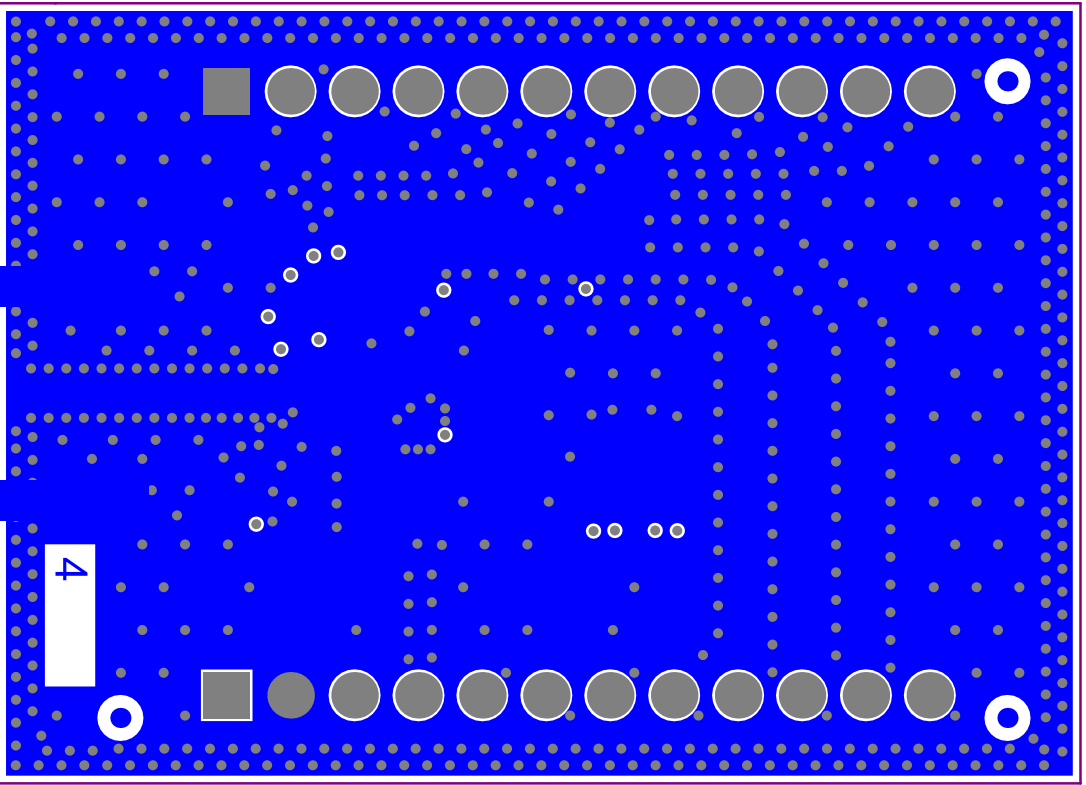
Project: Reference design for STM32WB09TEF - IPD		
Layer: Top Layer	Gerber: .GTL	
Variant: [No Variations]	MB2202	
Date: 18-12-2025	Rev: B	



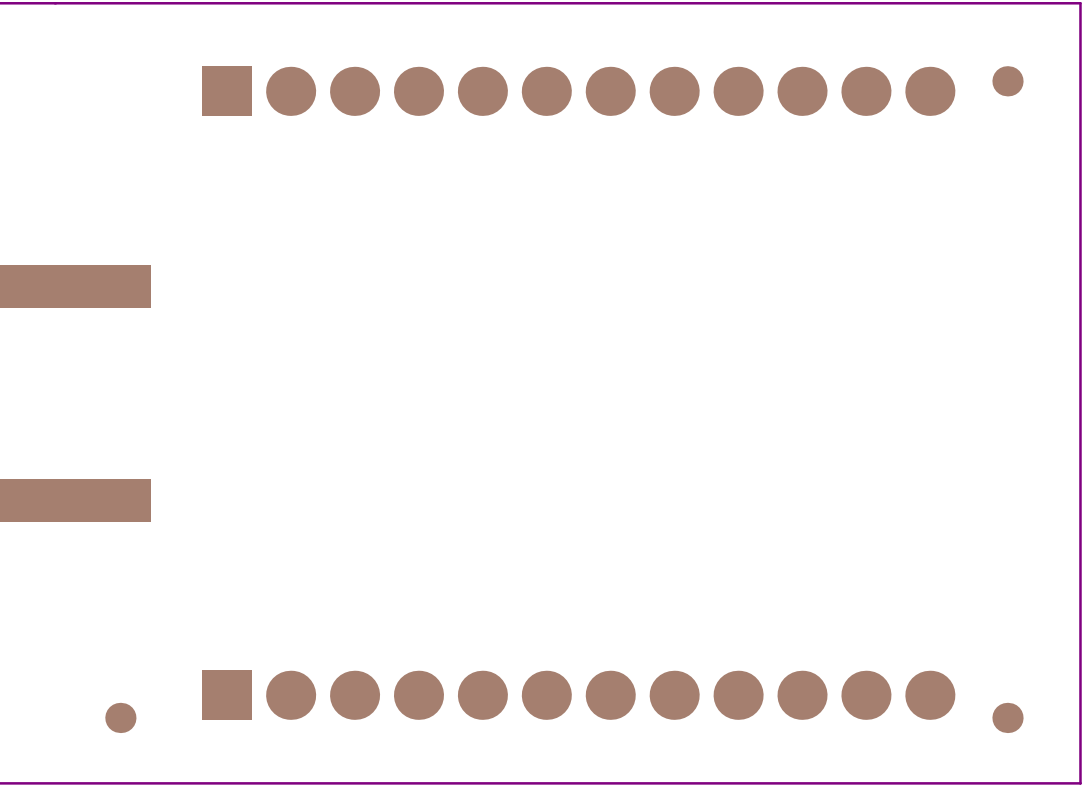
Project: Reference design for STM32WB09TEF - IPD		
Layer: Signal Layer 1	Gerber: .G1	
Variant: [No Variations]	MB2202	
Date: 18-12-2025	Rev: B	



Project: Reference design for STM32WB09TEF - IPD		
Layer: Signal Layer 2	Gerber: .G2	
Variant: [No Variations]	MB2202	
Date: 18-12-2025	Rev: B	



Project: Reference design for STM32WB09TEF - IPD		
Layer: Bottom Layer	Gerber: .GBL	
Variant: [No Variations]	MB2202	
Date: 18-12-2025	Rev: B	



Project: Reference design for STM32WB09TEF - IPD

Layer: Bottom Solder

Gerber: .GBS

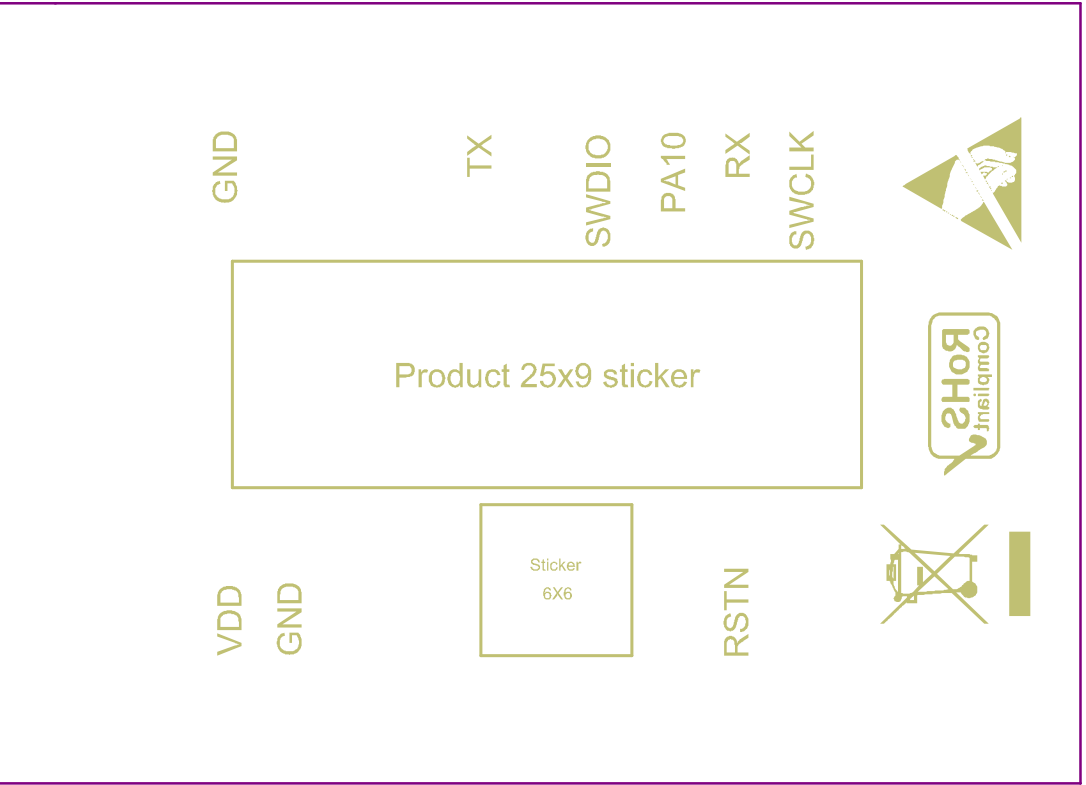
Variant: [No Variations]

MB2202

Date: 18-12-2025

Rev: B





Project: Reference design for STM32WB09TEF - IPD		
Layer: Bottom Overlay	Gerber: .GBO	
Variant: [No Variations]	MB2202	
Date: 18-12-2025	Rev: B	

PCB SPECIFICATIONS :

A. MATERIAL :

FR-4

☐ TG-170

☒ TG-150

☐ TG-140

B. MATERIAL FAMILY :

N/A

C. SOLDERMASK COLOR :

☒ GREEN

☐ WHITE

☐ RED

☐ BLACK

D. SILKSCREEN COLOR :

☒ WHITE

☐ YELLOW

☐ BLACK

☐ Blue ink PANTONE 2955

E. SURFACE FINISH :

☒ ENIG

☐ IMMERSION SILVER

☐ IMMERSION TIN

☐ HASL

☐ HASL (PB-FREE)

☐ GOLDEN FINGER

☐ IMPEDANCE CONTROL :

☐ NO

☒ YES (SEE IMPEDANCE TABLE FOR DETAIL INFORMATION)

G. THROUGH VIA :

PLUG THE VIAS WHICH ARE COVERED WITH SOLDERMASK ONE OR TWO SIDE.

PLUG MATERIAL : ☒ SOLDERMASK

☐ NON-CONDUCTIVE EPOXY.

☐ STACK-UP :

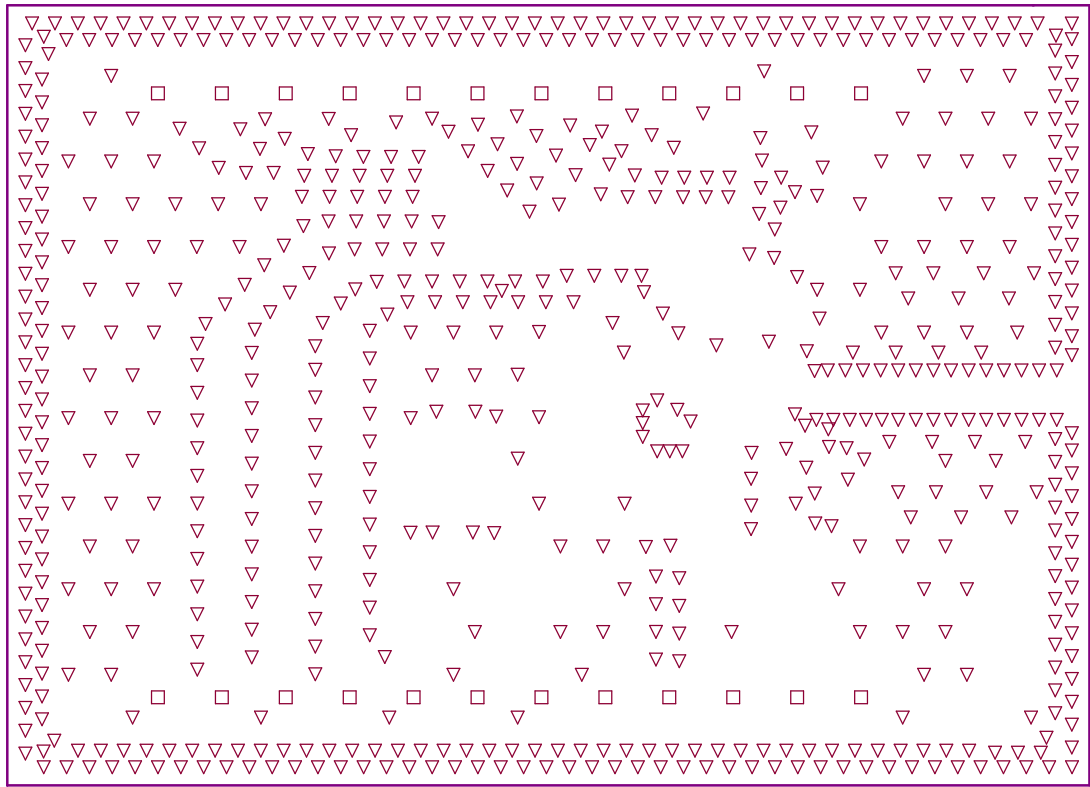
SEE LAYER STACK-UP SEQUENCE FOR OVERALL THICKNESS.

PCB : TYPE 3

ASPECT-RATIO, AXE Z :
6:1 to 8:1
LEVEL "B"

MINIMUM PARAMETERS

DEFAULT
TRACKS : 0.1mm
GAPS : 0.1mm



Layer	Name	Material	Thickness	Constant
	Top Overlay			
	Top Solder	Solder Resist	0,020mm	3.5
1	Top Layer		0,035mm	
	Dielectric 1	TU-768 (1x2113)	0,102mm	4.2
2	Signal Layer 1		0,036mm	
	Dielectric2	Tu-768 (2x2113)	0,254mm	4.3
3	Signal Layer 2		0,036mm	
	Dielectric3	TU-768 (1x2113)	0,102mm	4.2
4	Bottom Layer		0,035mm	
	Bottom Solder	Solder Resist	0,020mm	3.5
	Bottom Overlay			

Total board thickness: 0,639mm

Symbol	Count	Hole Size	Plated	Hole Type	Drill Layer Pair	Via/Pad	Pad Shape	Template	Hole Length	Routed Path Length
○	14	0.100mm (3.94mil)	PTH	Round	[uVia] Top Layer - Signal Layer 1	Via	Rounded	v25h10m0	-	-
□	24	1.000mm (39.37mil)	PTH	Round	Top Layer - Bottom Layer	Pad	Rounded	(Mixed)	-	-
▽	684	0.200mm (7.87mil)	PTH	Round	Top Layer - Bottom Layer	Via	Rounded	(Mixed)	-	-
	722 Total									

Project: Reference design for STM32WB09TEF - PD

Layer: Drill Drawing

Variant: [No Variations]

Date: 18-12-2025

Gerber: .DRL

MB2202

Rev: B

