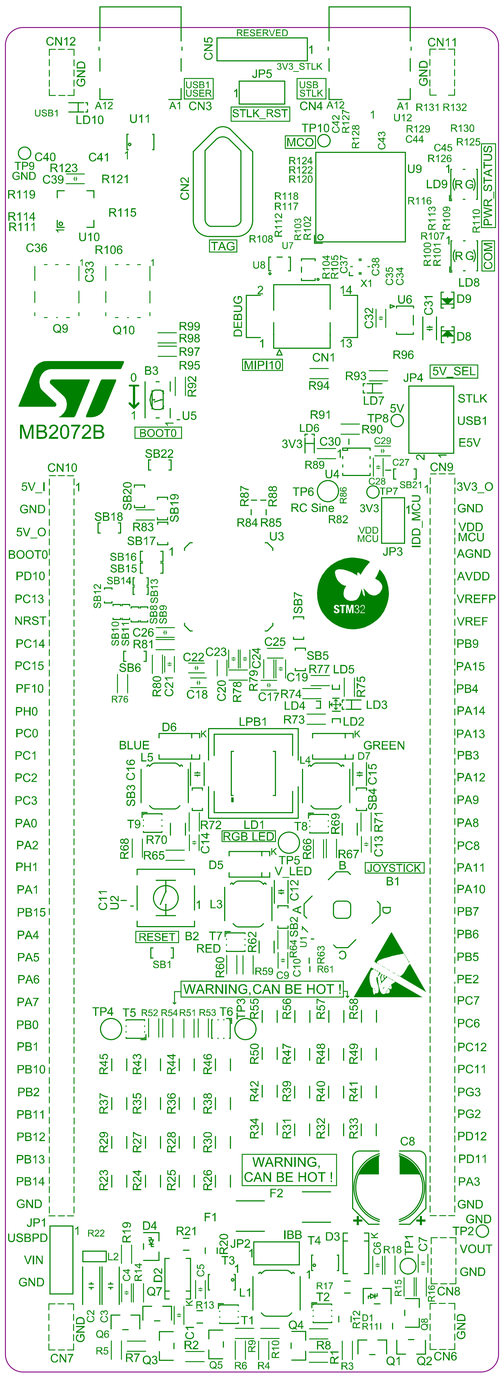
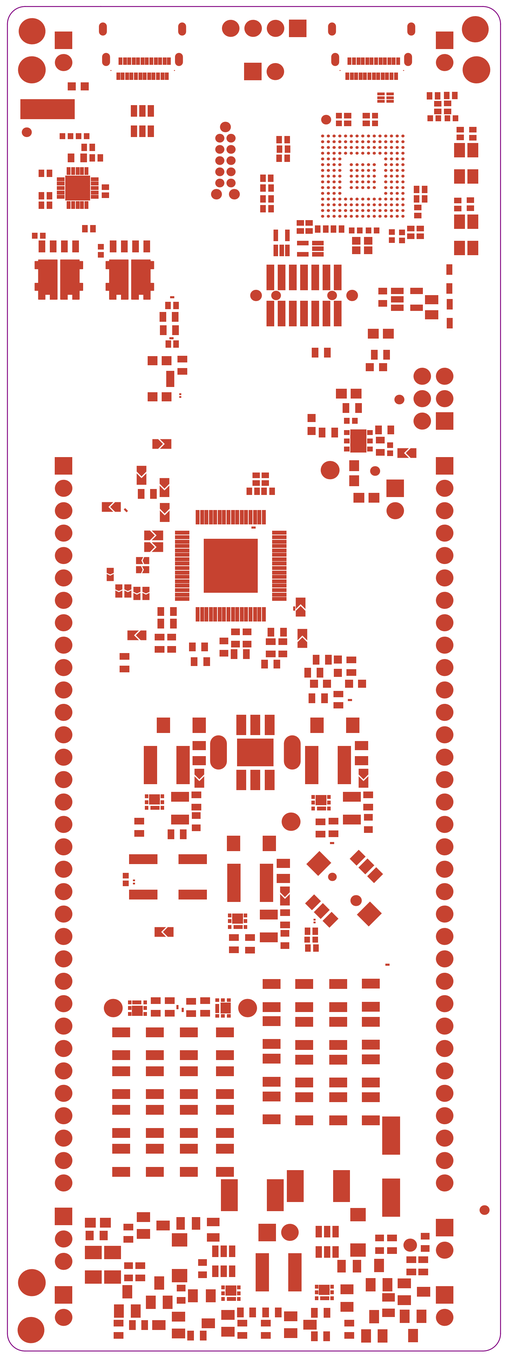
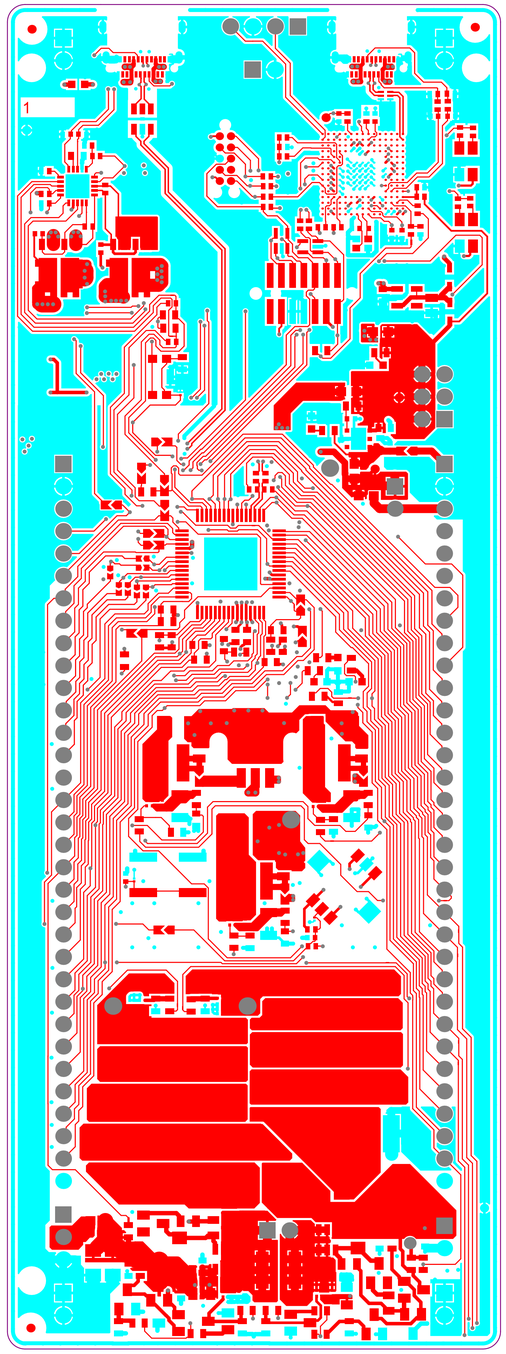


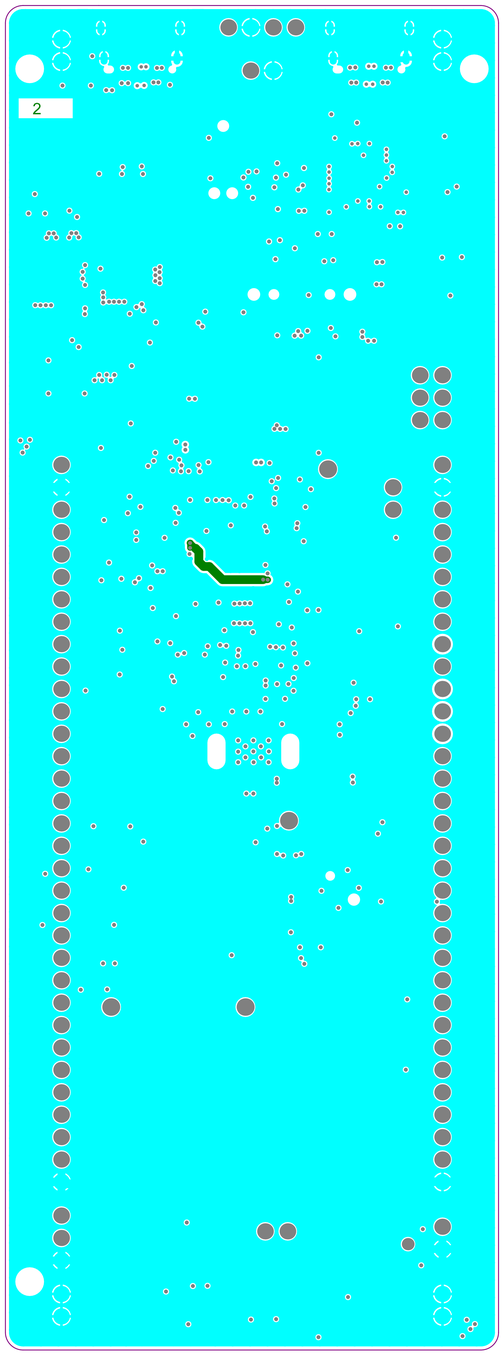
Project: STM32G5 DPOW Discovery	
Layer: Top Overlay	Gerber: .GTO
Variant: [No Variations]	Ref: MB2072
Date: 02-July-26	Rev: B



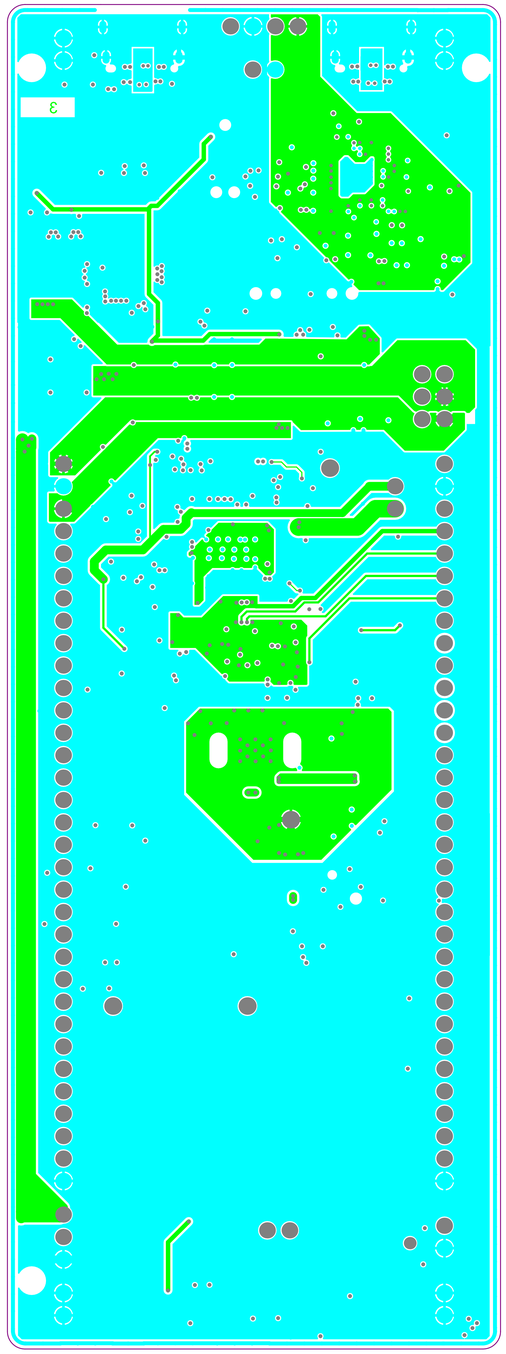
Project: STM32G5 DPOW Discovery	
Layer: Top Solder	Gerber: .GTS
Variant: [No Variations]	Ref: MB2072
Date: 02-July-26	Rev: B



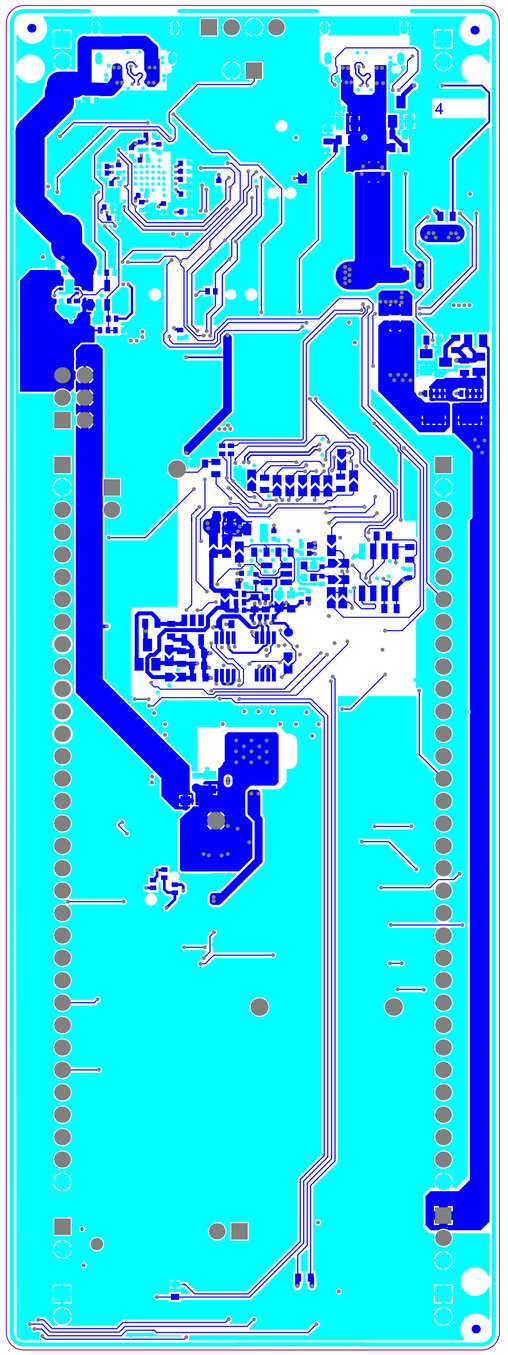
Project: STM32G5 DPOW Discovery	
Layer: Top Layer	Gerber: .GTL
Variant: [No Variations]	Ref: MB2072
Date: 02-July-26	Rev: B



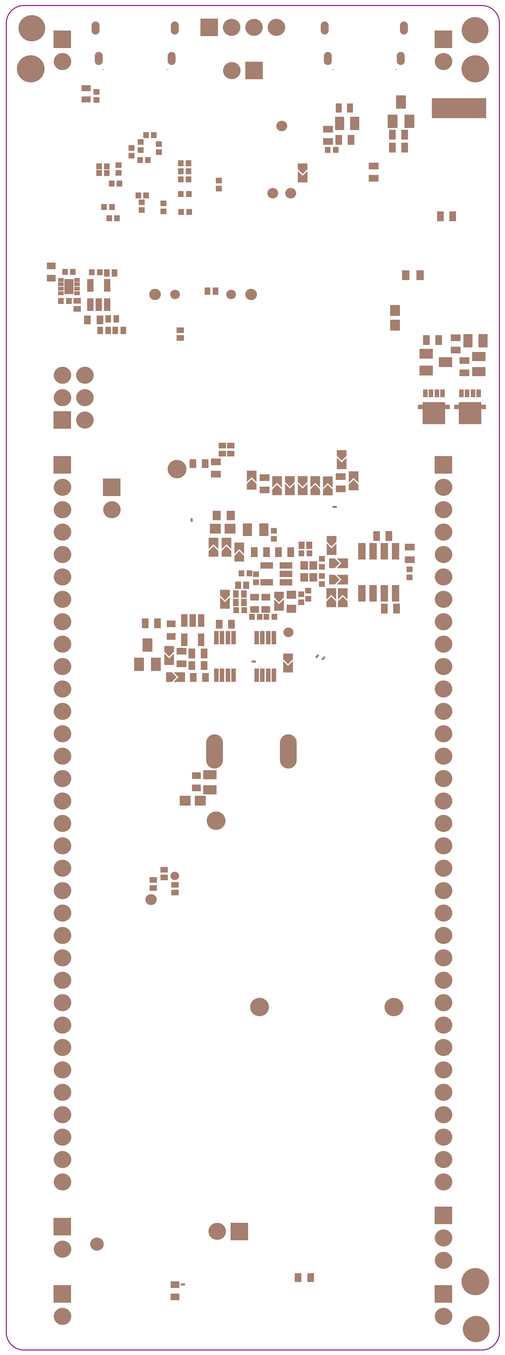
Project: STM32G5 DPOW Discovery	
Layer: Signal Layer 1	Gerber: .G1
Variant: [No Variations]	Ref: MB2072
Date: 02-July-26	Rev: B



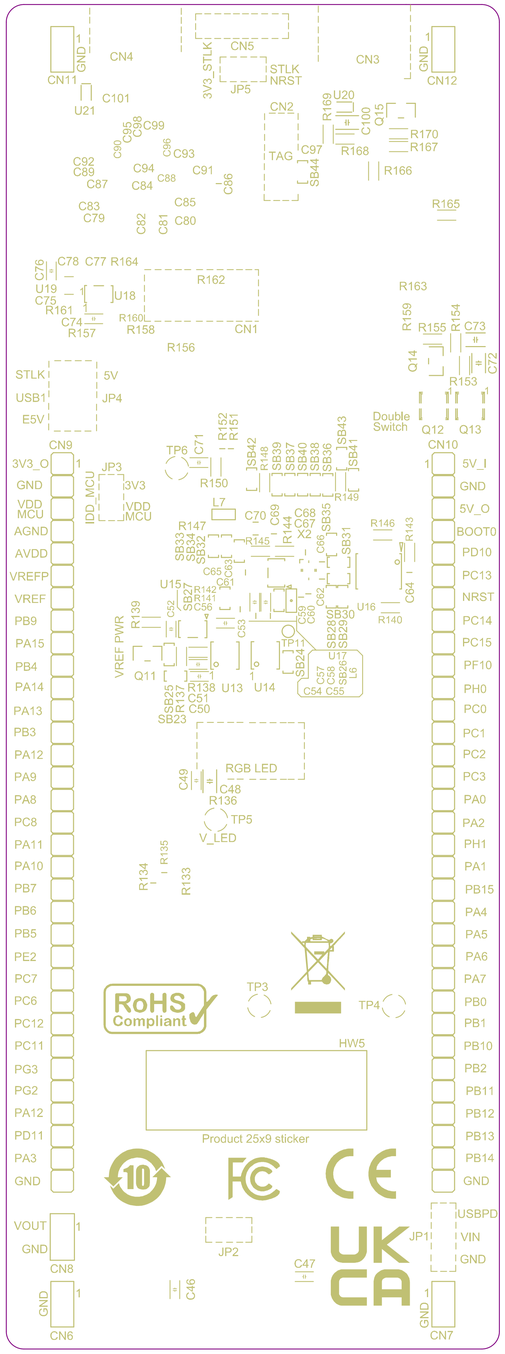
Project: STM32G5 DPOW Discovery	
Layer: Signal Layer 2	Gerber: .G2
Variant: [No Variations]	Ref: MB2072
Date: 02-July-26	Rev: B



Project: STM32G5 DPOW Discovery	
Layer: Bottom Layer	Gerber:.GBL
Variant: [No Variations]	Ref: MB2072
Date: 02-July-26	Rev: B



Project: STM32G5 DPOW Discovery	
Layer: Bottom Solder	Gerber:.GBS
Variant: [No Variations]	Ref: MB2072
Date: 02-July-26	Rev: B



Project: STM32G5 DPOW Discovery	
Layer: Bottom Overlay	Gerber: .GBO
Variant: [No Variations]	Ref: MB2072
Date: 02-July-26	Rev: B

THE COMPONENTS WITH PLATED THROUGH HOLE (PTH) MAY BE WELDED (CABLED) IN "PIN-IN-PASTE" MODE (IF NECESSARY)

PCB SPECIFICATIONS :

A. MATERIAL :	FR-4	☐ TG-170	☒ TG-150	☐ TG-140	
B. MATERIAL FAMILY :	N/A				
C. SOLDERMASK COLOR :	☐ GREEN	☐ WHITE	☐ RED	☒ Blue ink PANTONE 2955	
D. SILKSCREEN COLOR :	☒ WHITE	☐ YELLOW	☐ BLACK	☐ BLUE	
E. SURFACE FINISH :	☒ ENIG	☐ IMMERSION SILVER		☐ IMMERSION TIN	
	☐ HASL	☐ HASL (PB-FREE)		☐ GOLDEN FINGER	
F. IMPEDANCE CONTROL :	☐ NO	☒ YES (SEE IMPEDANCE TABLE FOR DETAIL INFORMATION)			
G. THROUGH VIA :	PLUG THE VIAS WHICH ARE COVERED WITH SOLDERMASK ONE OR TWO SIDE.				
	PLUG MATERIAL : ☒ SOLDERMASK	☐ NON-CONDUCTIVE EPOXY.			
H. STACK-UP :	SEE LAYER STACK-UP SEQUENCE FOR OVERALL THICKNESS.				

PCB : TYPE 3

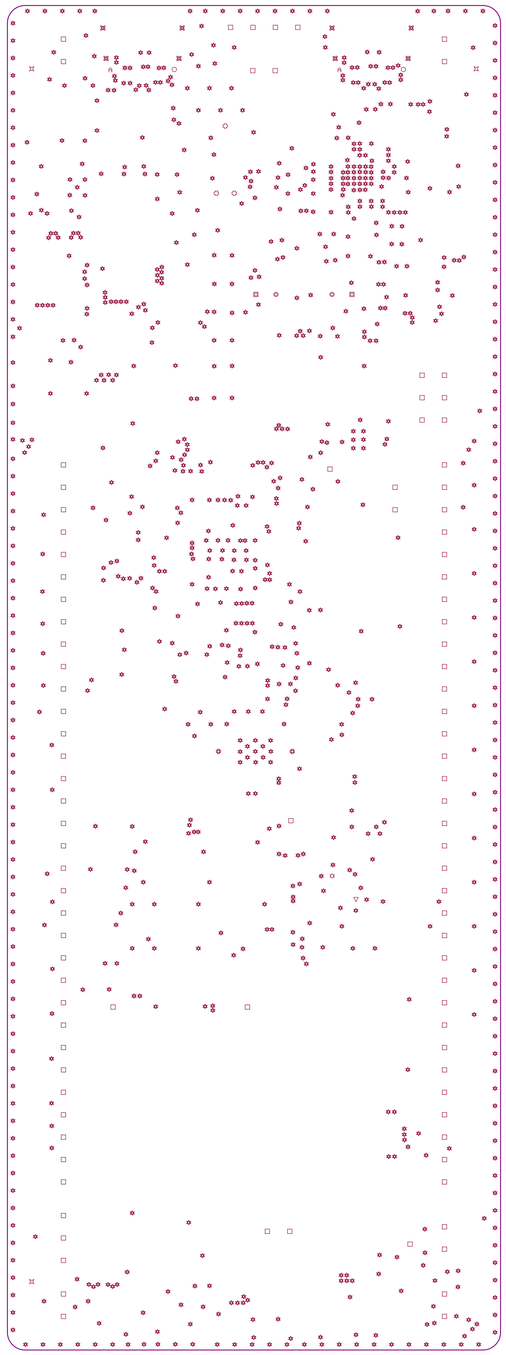
ASPECT-RATIO, AXE Z :

6:1 to 8:1
LEVEL "B"

MINIMUM PARAMETERS

DEFAULT
TRACKS : 0.120mm
GAPS : 0.120mm

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	0,015mm	3.5	
1	Top Layer		0,050mm		
	Dielectric 1	PP-IT-180A	0,100mm	4.2	
2	Signal Layer 1		0,035mm		
	Dielectric 2	FR4	1,200mm	4.2	
3	Signal Layer 2		0,035mm		
	Dielectric 3	PP-IT-180A	0,100mm	4.2	
4	Bottom Layer		0,050mm		
	Bottom Solder	Solder Resist	0,015mm	3.5	
	Bottom Overlay				



Symbol	Count	Hole Size	Plated	Hole Type	Drill Layer Pair	Via/Pad	Hole Length	Routed Path Length
	1000	0.200mm (7.87mil)	PTH	Round	Top Layer - Bottom Layer	Via	-	-
	8	0.500mm (19.69mil)	PTH	Slot	Top Layer - Bottom Layer	Pad	1.100mm (43.31mil)	0.600mm (23.62mil)
	2	0.650mm (25.59mil)	NPTH	Round	Top Layer - Bottom Layer	Pad	-	-
	2	0.650mm (25.59mil)	NPTH	Slot	Top Layer - Bottom Layer	Pad	0.950mm (37.40mil)	0.300mm (11.81mil)
	1	0.850mm (33.47mil)	NPTH	Round	Top Layer - Bottom Layer	Pad	-	-
	2	0.970mm (38.19mil)	NPTH	Round	Top Layer - Bottom Layer	Pad	-	-
	100	1.000mm (39.37mil)	PTH	Round	Top Layer - Bottom Layer	Pad	-	-
	3	1.100mm (43.31mil)	NPTH	Round	Top Layer - Bottom Layer	Pad	-	-
	1	1.150mm (45.28mil)	NPTH	Round	Top Layer - Bottom Layer	Pad	-	-
	2	1.190mm (46.85mil)	NPTH	Round	Top Layer - Bottom Layer	Pad	-	-
	2	1.800mm (70.87mil)	NPTH	Slot	Top Layer - Bottom Layer	Pad	3.800mm (149.61mil)	2.000mm (78.74mil)
	3	3.000mm (118.11mil)	NPTH	Round	Top Layer - Bottom Layer	Pad	-	-
	1126 Total							

Slot definitions : Routed Path Length = Calculated from tool start centre position to tool end centre position.
Hole Length = Routed Path Length + Tool Size = Slot length as defined in the PCB layout

IMPEDANCE TABLE PIOxx & Others (DBG.SWDIO / DBG.SWO / DBG.SWCLK / DBG.JTDI and T_SWO / T_SWCLK / T_SWDIO / T_JTDI and signals PB3 / PA15 / PA14 / PA13 & PC0 / PC1 / PC2 / PC3 / PF10 / PH0 and NetSB13_2)

LAYER "Routing"	LAYER "Ref GND"	TRACE "Width mm"	NET "Lenght mm"	SPACING "Intra Diff. Pair mm"	SPACING "Others Net mm"	SPACING "GND mm"	IMPEDANCE (Single ended)	IMPEDANCE (Differential)	TOL.
L1 (Top_Lay)	L2 (Sig_Lay1)	0.125	Minimum	n/a	0.250 Min.	0.250 Min.	56 Ohms	n/a	+/- 10%
L4 (Bot_Lay)	L3 (Sig_Lay2)	0.125	Minimum	n/a	0.250 Min.	0.250 Min.	56 Ohms	n/a	+/- 10%

IMPEDANCE TABLE USB_USER1 (USB1_CN_FS, USB1.FS and USB1_FS) & USB_STLK (STLK_USB_CN and STLK_USB)

LAYER "Routing"	LAYER "Ref GND"	TRACE "Width mm"	NET "Lenght mm"	SPACING "Intra Diff. Pair mm"	SPACING "Others Net mm"	SPACING "GND mm"	IMPEDANCE (Single ended)	IMPEDANCE (Differential)	TOL.
L1 (Top_Lay)	L2 (Sig_Lay1)	0.160	Minimum	0.200	0.4 Min.	0.4 Min.	n/a	90 Ohms	+/- 10%
L4 (Bot_Lay)	L3 (Sig_Lay2)	0.160	Minimum	0.200	0.4 Min.	0.4 Min.	n/a	90 Ohms	+/- 10%

Project: STM32G5 DPOW Discovery	
Layer: Drill Drawing	Gerber: .DRL
Variant: [No Variations]	Ref: MB2072
Date: 02-July-26	Rev: B