
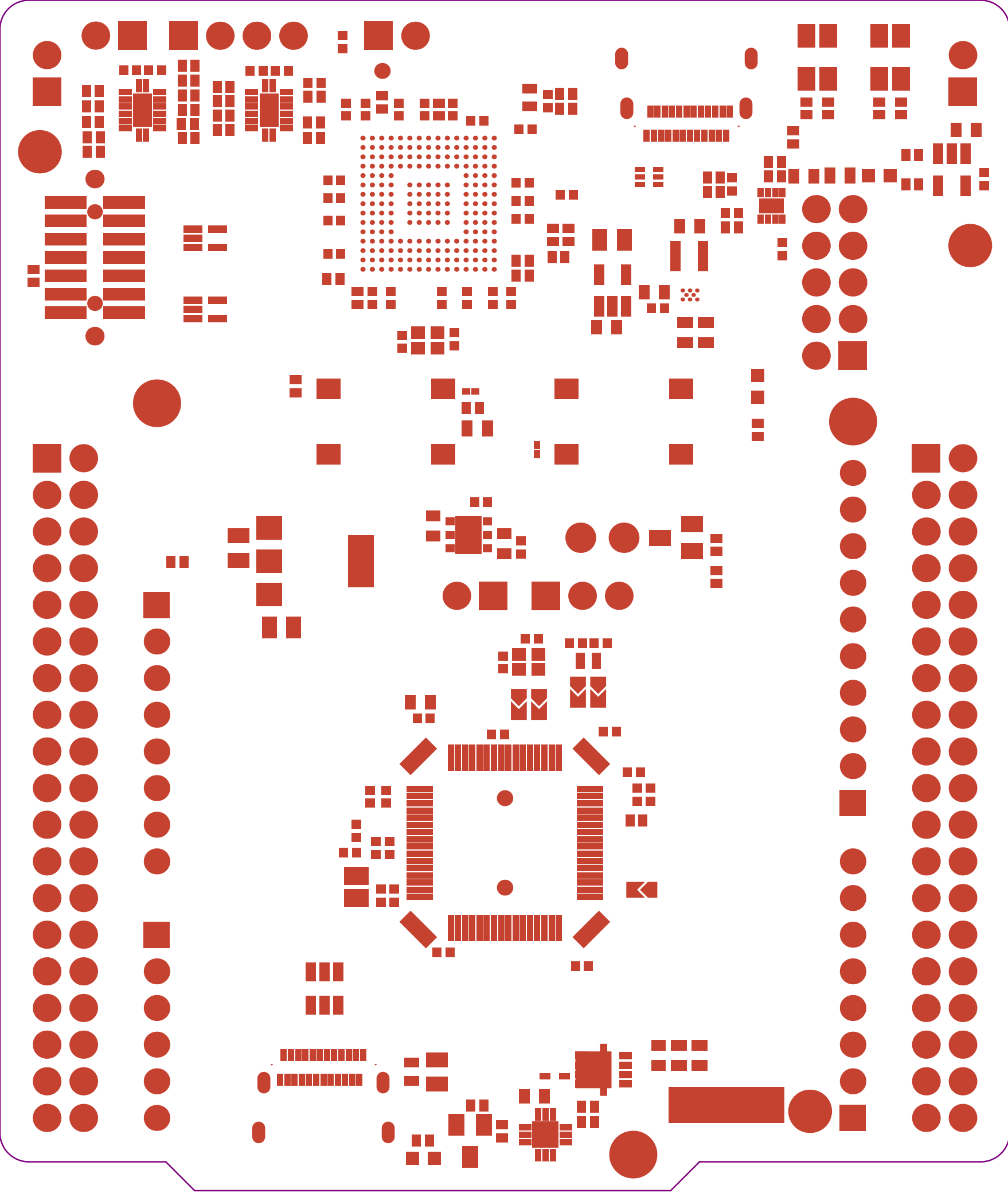

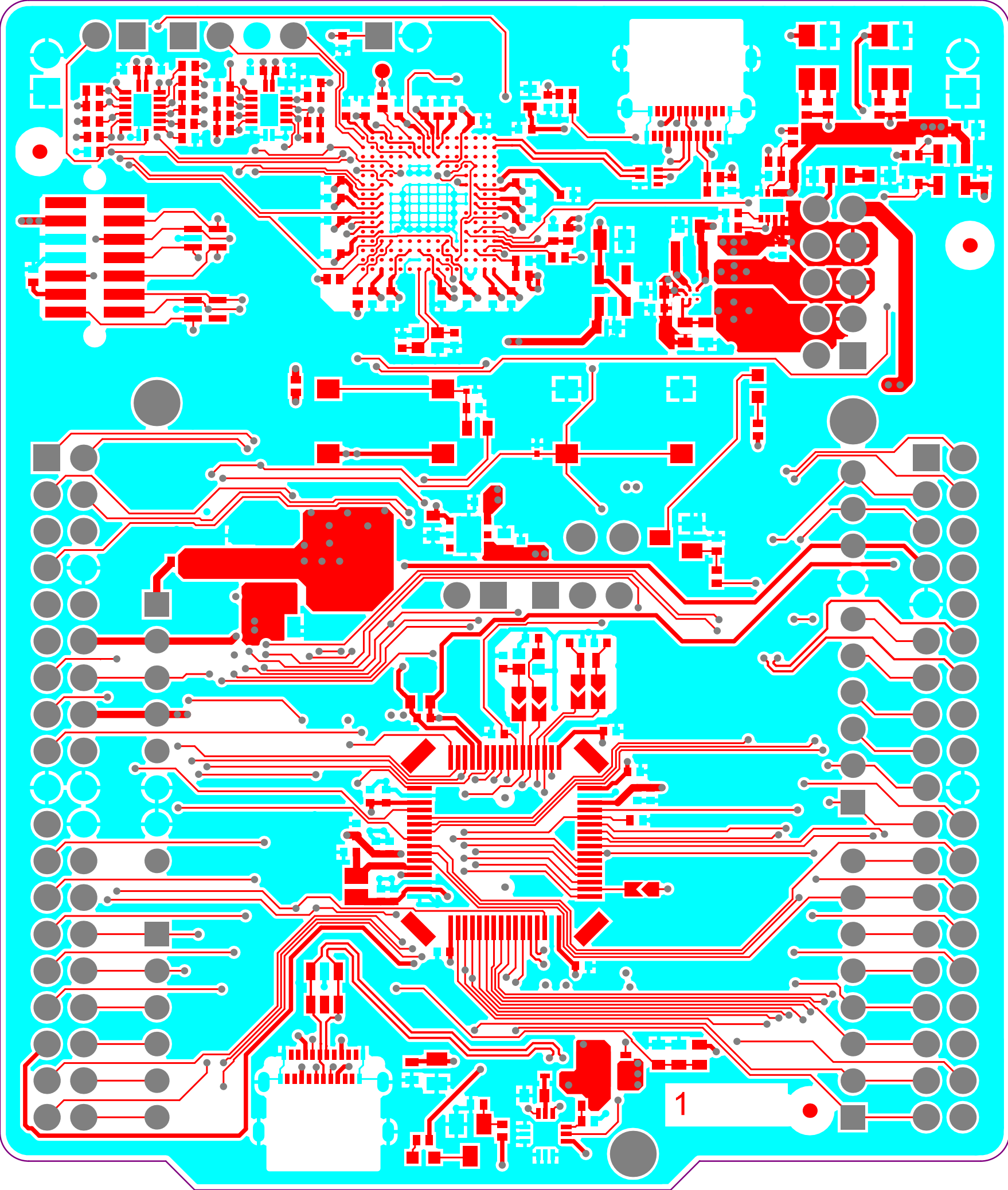



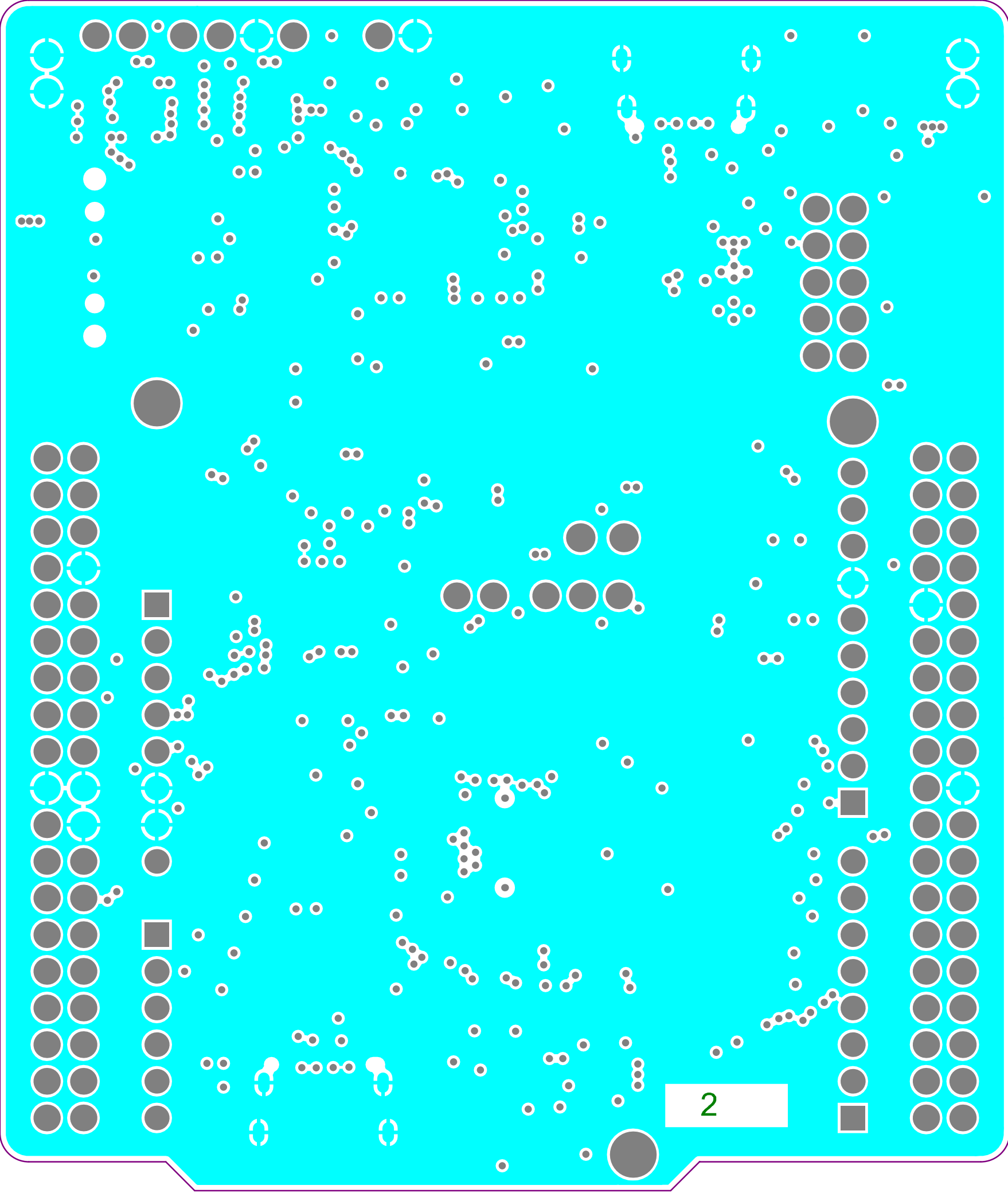
Project: Nucleo-64 SMPS		
Layer: Top Overlay	Gerber: .GTO	
Variant: [No Variations]	MB1841	
Date: 29-JUL-24	Rev: F	




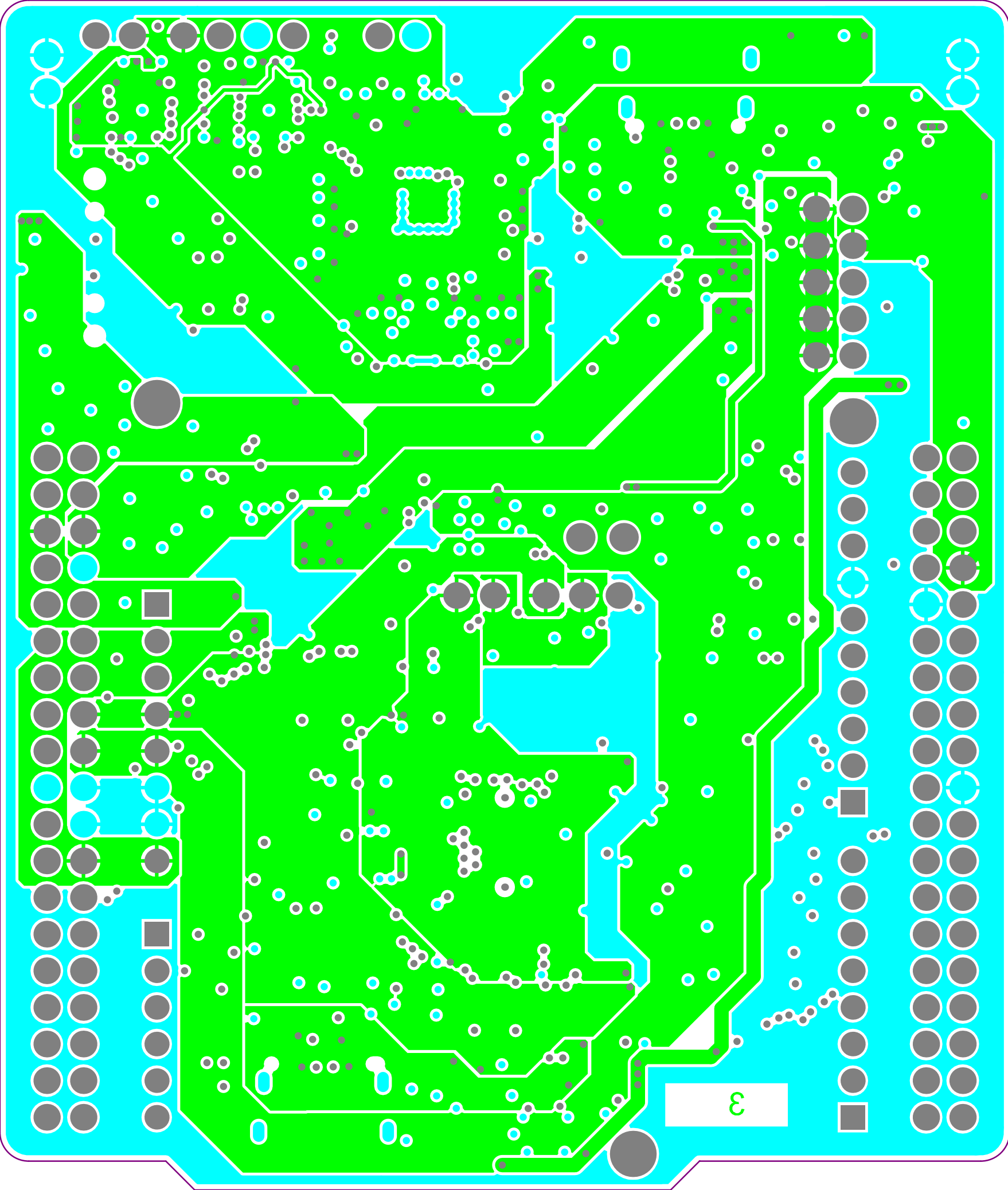
Project: Nucleo-64 SMPS		
Layer: Top Solder	Gerber: .GTS	
Variant: [No Variations]	MB1841	
Date: 29-JUL-24	Rev: F	




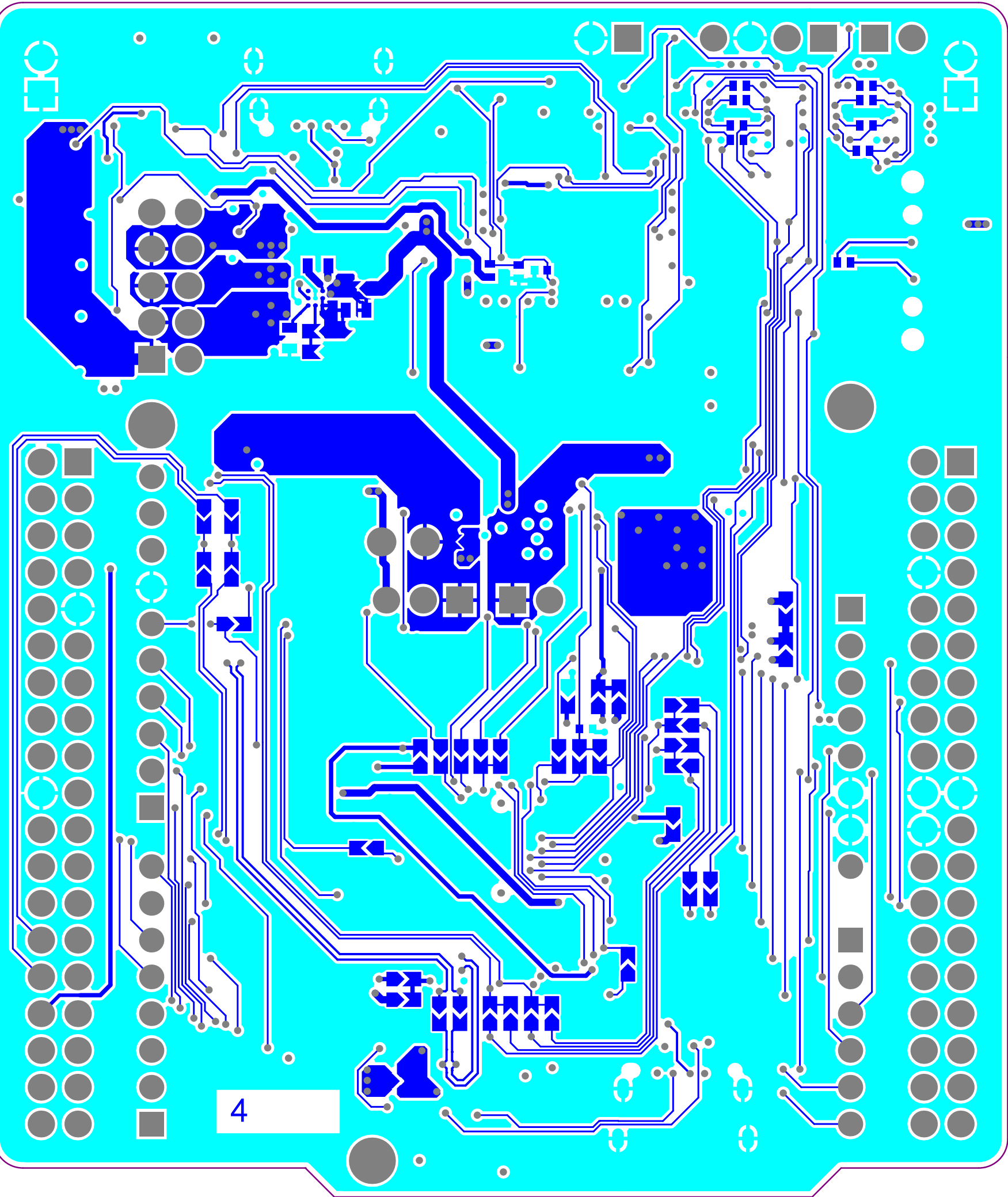
Project: Nucleo-64 SMPS		
Layer: Top Layer	Gerber: .GTL	
Variant: [No Variations]	MB1841	
Date: 29-JUL-24	Rev: F	




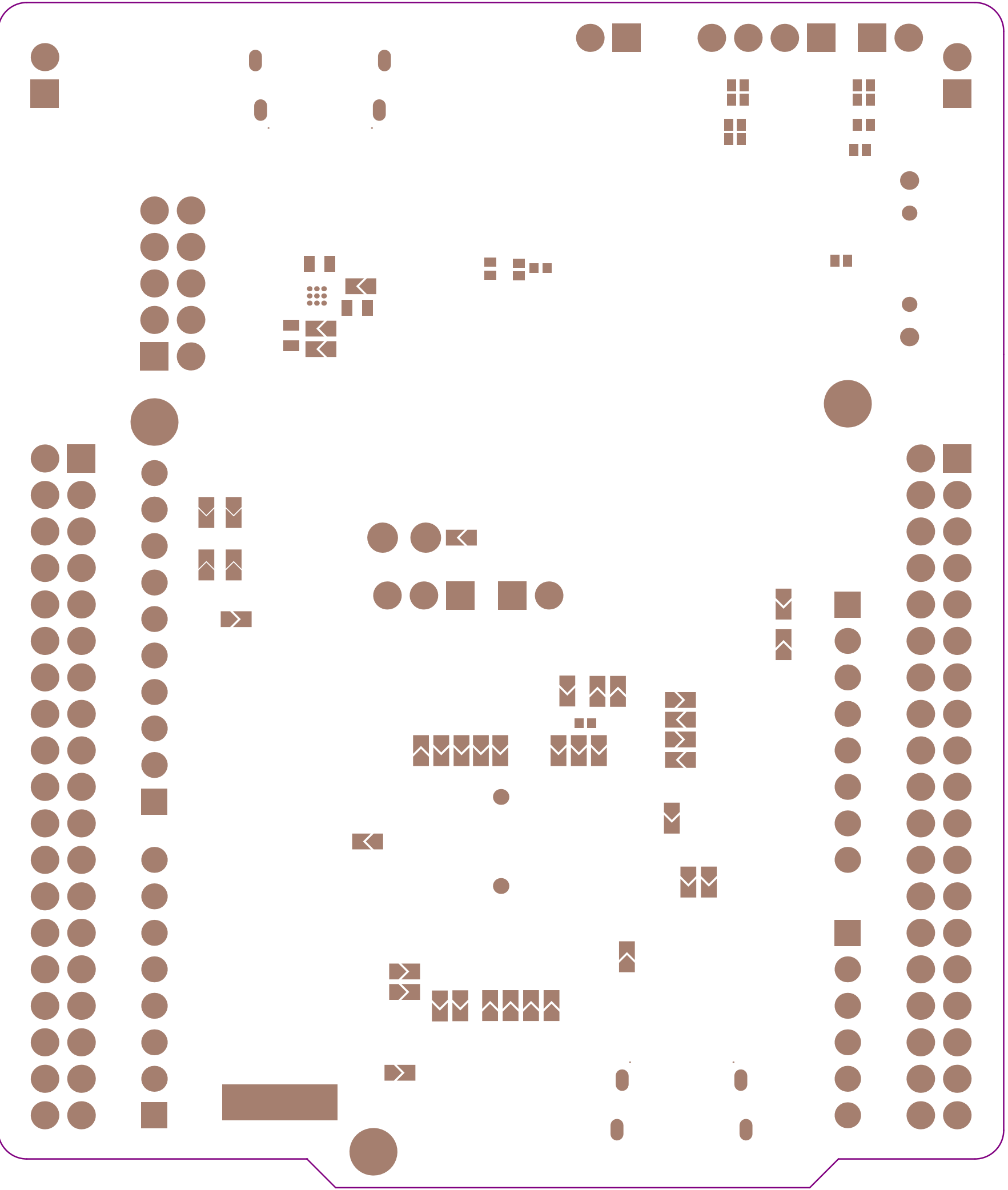
Project: Nucleo-64 SMPS		
Layer: Signal Layer 1	Gerber: .G1	
Variant: [No Variations]	MB1841	
Date: 29-JUL-24	Rev: F	




Project: Nucleo-64 SMPS		
Layer: Signal Layer 2	Gerber: .G2	
Variant: [No Variations]	MB1841	
Date: 29-JUL-24	Rev: F	




Project: Nucleo-64 SMPS		
Layer: Bottom Layer	Gerber:.GBL	
Variant: [No Variations]	MB1841	
Date: 29-JUL-24	Rev: F	



Project: Nucleo-64 SMPS		
Layer: Bottom Solder	Gerber: .GBS	
Variant: [No Variations]	MB1841	
Date: 29-JUL-24	Rev: F	



Project: Nucleo-64 SMPS		
Layer: Bottom Overlay	Gerber: .GBO	
Variant: [No Variations]	MB1841	
Date: 29-JUL-24	Rev: F	

« THE COMPONENTS WITH PLATED THROUGH HOLE (PTH) MAY BE WELDED (CABLED) IN "PIN-IN-PASTE" MODE (IF NECESSARY) »

PCB SPECIFICATIONS :

A. MATERIAL :

B. MATERIAL FAMILY :

C. SOLDERMASK COLOR :

D. SILKSCREEN COLOR :

E. SURFACE FINISH :

F. IMPEDANCE CONTROL :

G. THROUGH VIA :

H. STACK-UP :

FR-4

N/A

☐ GREEN

☒ WHITE

☐ HASL

☐ NO

☒ ENIG

☐ HASL (PB-FREE)

☐ YES (SEE IMPEDANCE TABLE FOR DETAIL INFORMATION)

☐ TG-170

☒ TG-150

☐ TG-140

☐ RED

☐ BLACK

☒ Blue ink PANTONE 2955

☐ IMMERSION SILVER

☐ IMMERSION TIN

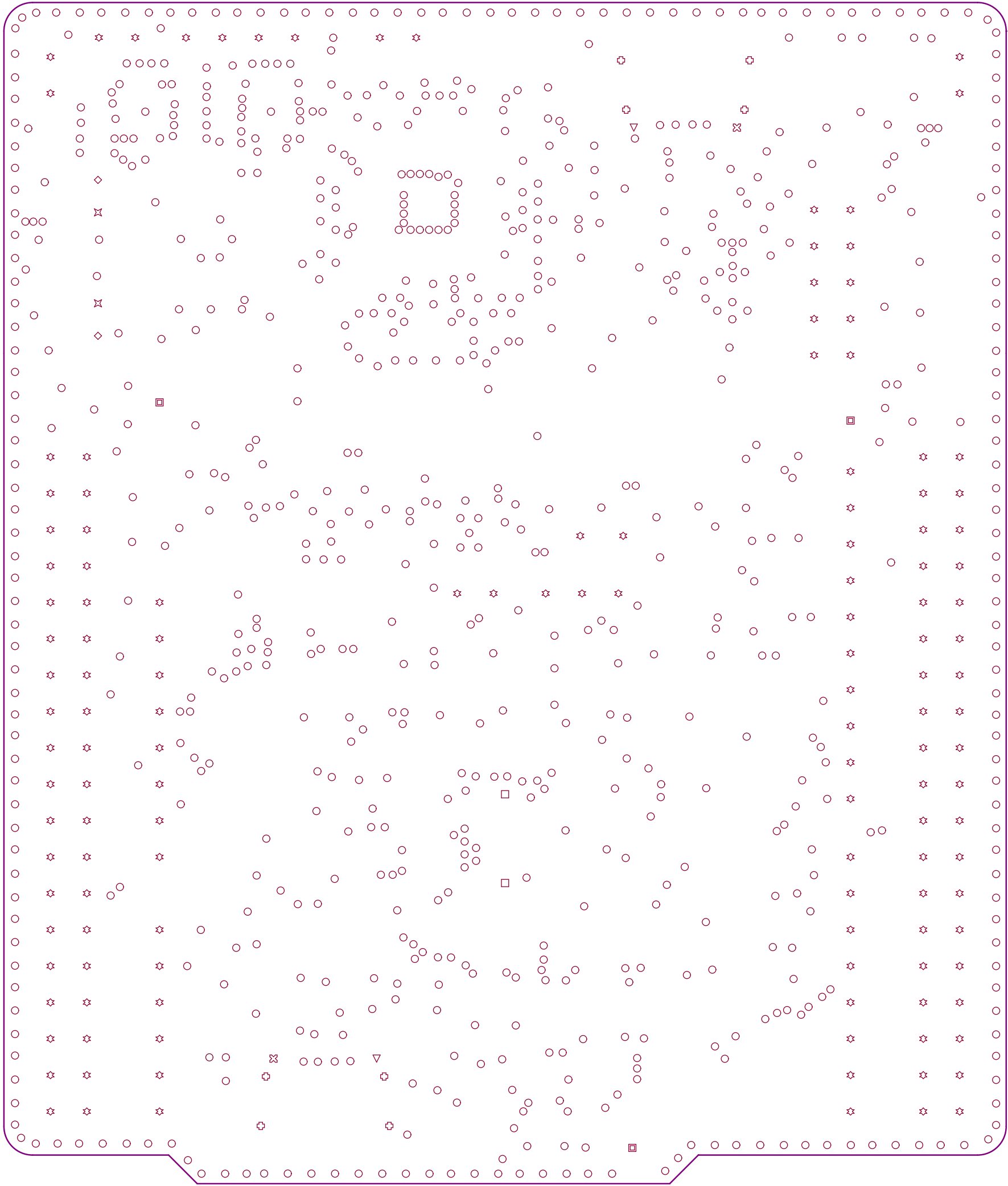
☐ GOLDEN FINGER

☐ SOLDERMASK

☐ NON-CONDUCTIVE EPOXY.

**Plating type :

lead Gold



Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	0.015mm	3.5	
1	Top Layer		0.035mm		
	Dielectric 1		0.108mm	4.2	
2	Signal Layer 1		0.035mm		
	Dielectric 2	FR4	1.134mm	4.2	
3	Signal Layer 2		0.035mm		
	Dielectric 3		0.108mm	4.2	
4	Bottom Layer		0.035mm		
	Bottom Solder	Solder Resist	0.015mm	3.5	
	Bottom Overlay				

PCB : TYPE 3

ASPECT-RATIO, AXE Z :
6:1 to 8:1
LEVEL "B"

MINIMUM PARAMETERS

DEFAULT
TRACKS : 0.120mm
GAPS : 0.120mm

Symbol	Count	Hole Size	Plated	Hole Type	Drill Layer Pair	Via/Pad	Hole Length	Routed Path Length
○	796	0.250mm (9.84mil)	PTH	Round	Top Layer - Bottom Layer	Via	-	-
⊕	8	0.500mm (19.69mil)	PTH	Slot	Top Layer - Bottom Layer	Pad	1.100mm (43.31mil)	0.600mm (23.62mil)
⊗	2	0.650mm (25.59mil)	NPTH	Round	Top Layer - Bottom Layer	Pad	-	-
▽	2	0.650mm (25.59mil)	NPTH	Slot	Top Layer - Bottom Layer	Pad	0.950mm (37.40mil)	0.300mm (11.81mil)
⊗	2	0.970mm (38.19mil)	NPTH	Round	Top Layer - Bottom Layer	Pad	-	-
□	2	1.000mm (39.37mil)	NPTH	Round	Top Layer - Bottom Layer	Pad	-	-
⊗	137	1.000mm (39.37mil)	PTH	Round	Top Layer - Bottom Layer	Pad	-	-
◇	2	1.190mm (46.85mil)	NPTH	Round	Top Layer - Bottom Layer	Pad	-	-
▣	3	3.200mm (125.98mil)	NPTH	Round	Top Layer - Bottom Layer	Pad	-	-
	954 Total							

Slot definitions : Routed Path Length = Calculated from tool start centre position to tool end centre position.
Hole Length = Routed Path Length + Tool Size = Slot length as defined in the PCB layout