
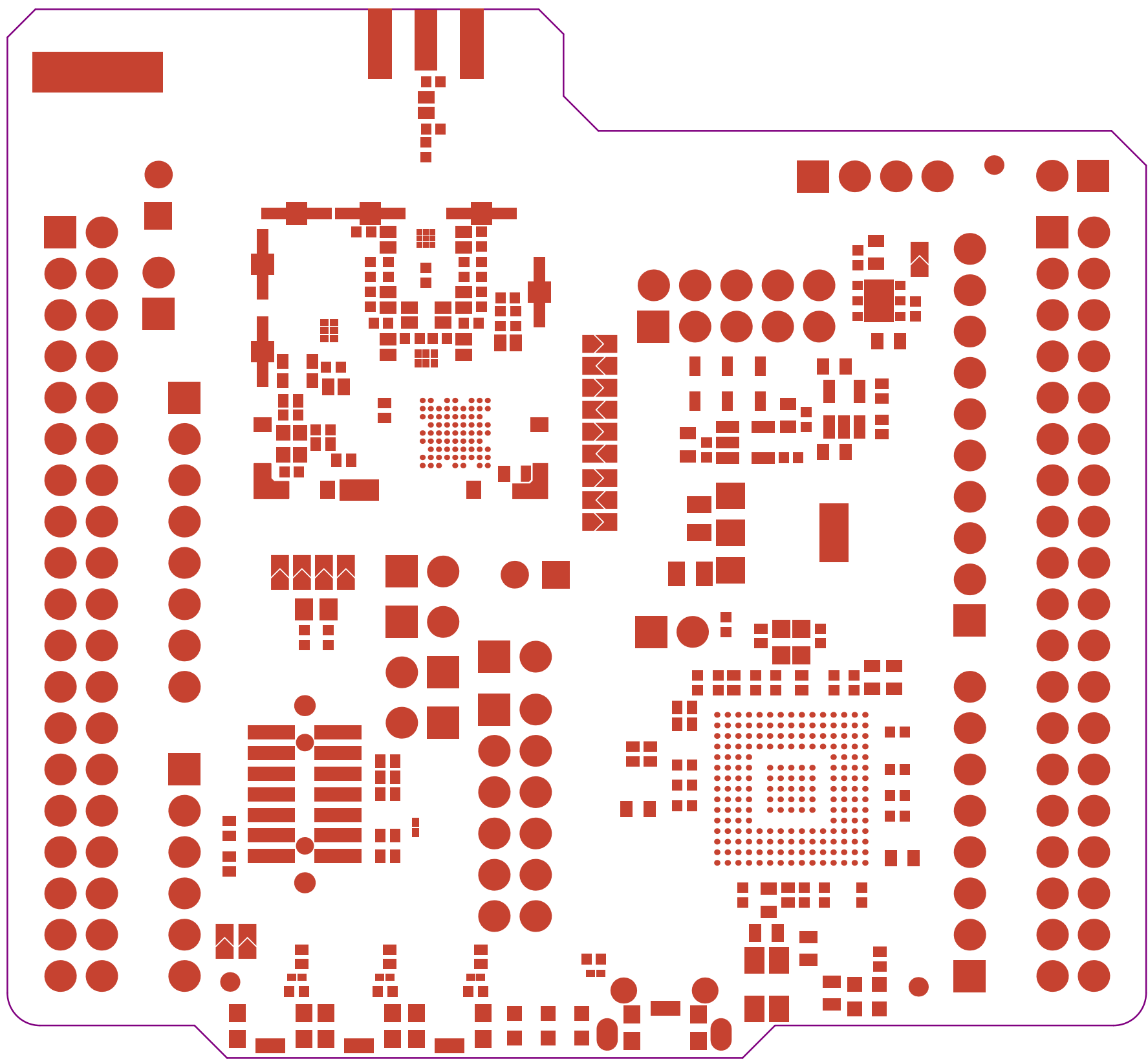

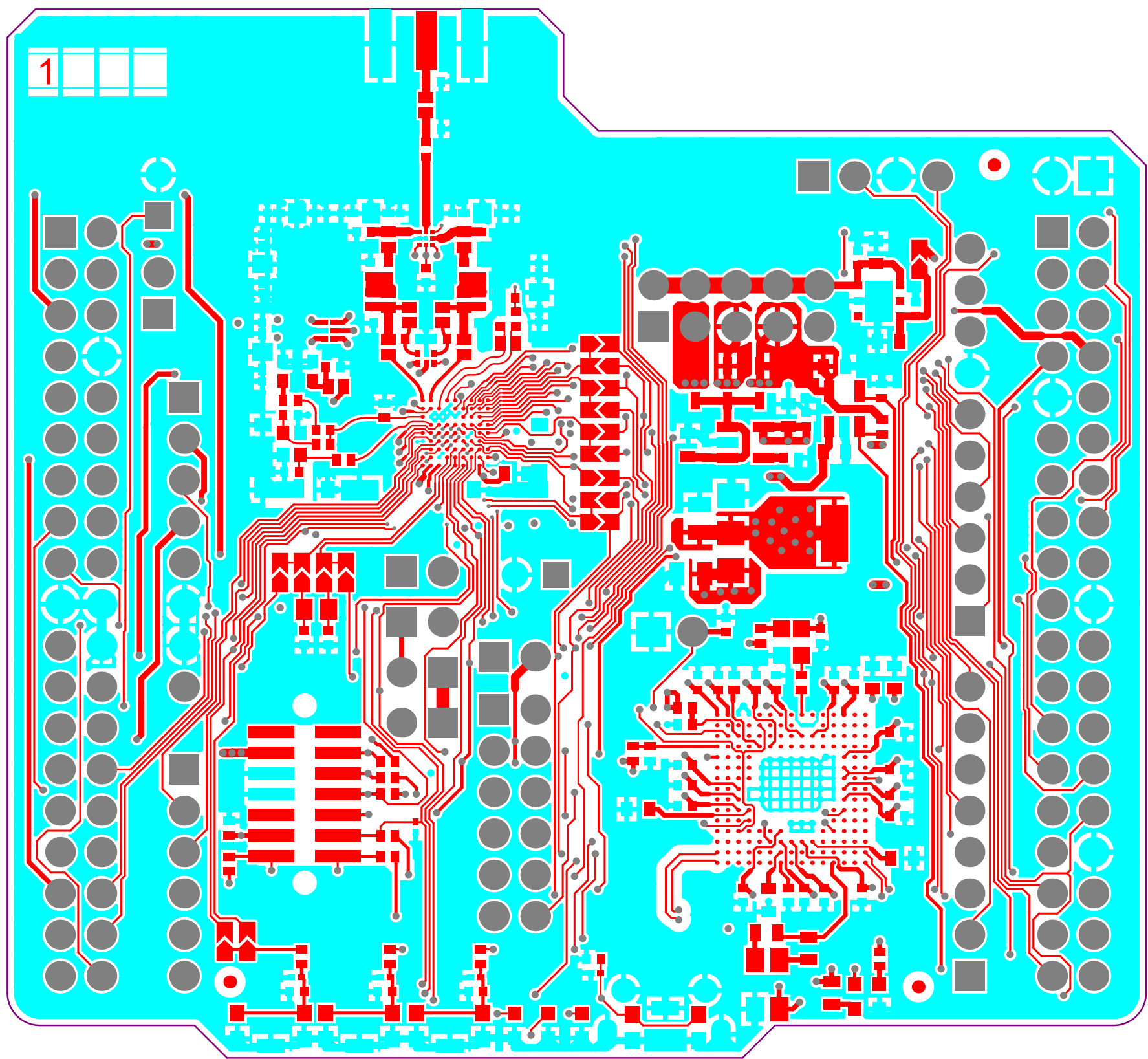



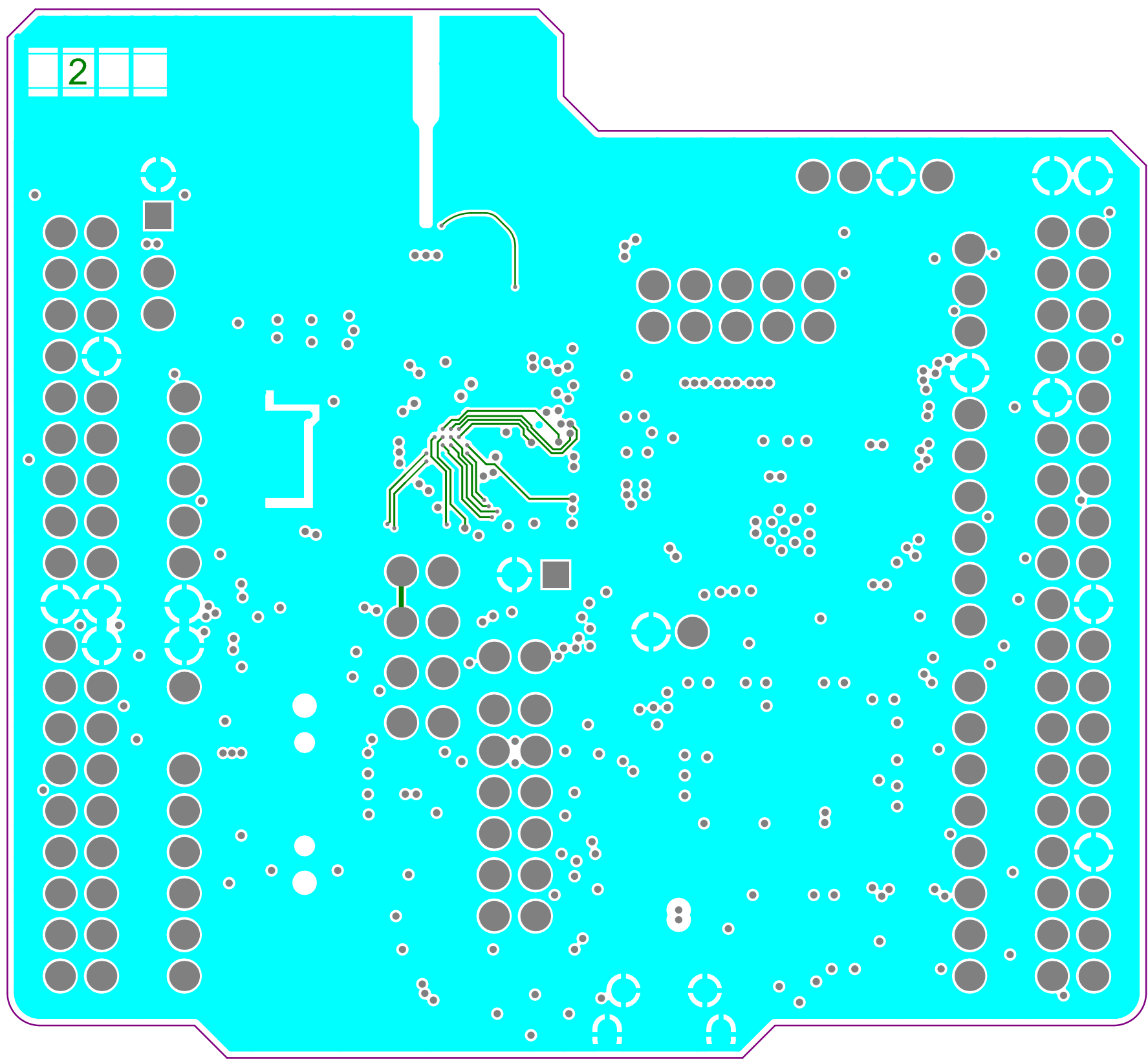
Project: NUCLEO73 STM32WL5		
Layer: Top Overlay	Gerber: .GTO	
Variant: [No Variations]	Ref: MB1389	
Date: 20-April-23	Rev: D	




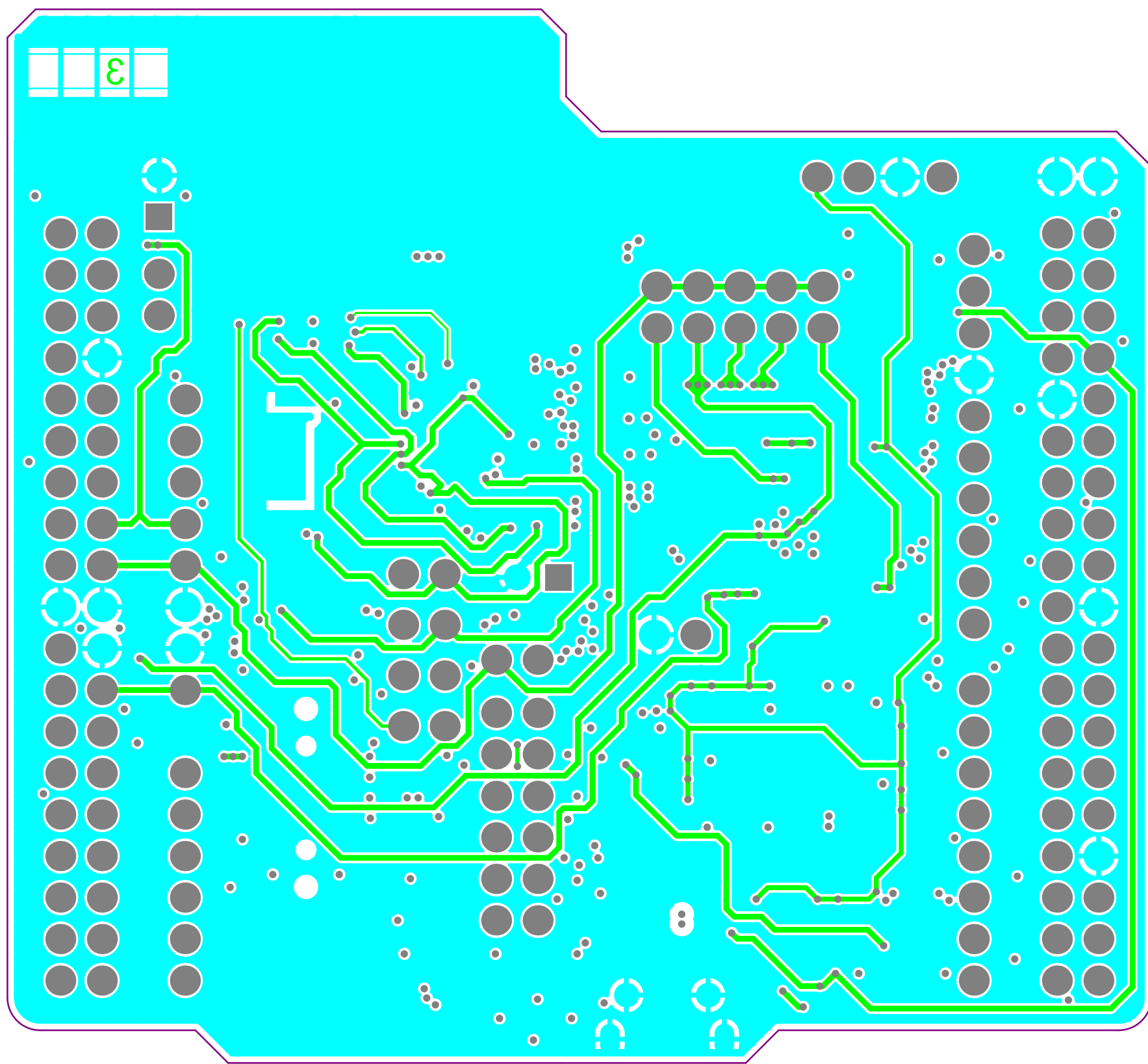
Project: NUCLEO73 STM32WL5		
Layer: Top Solder	Gerber: .GTS	
Variant: [No Variations]	Ref: MB1389	
Date: 20-April-23	Rev: D	




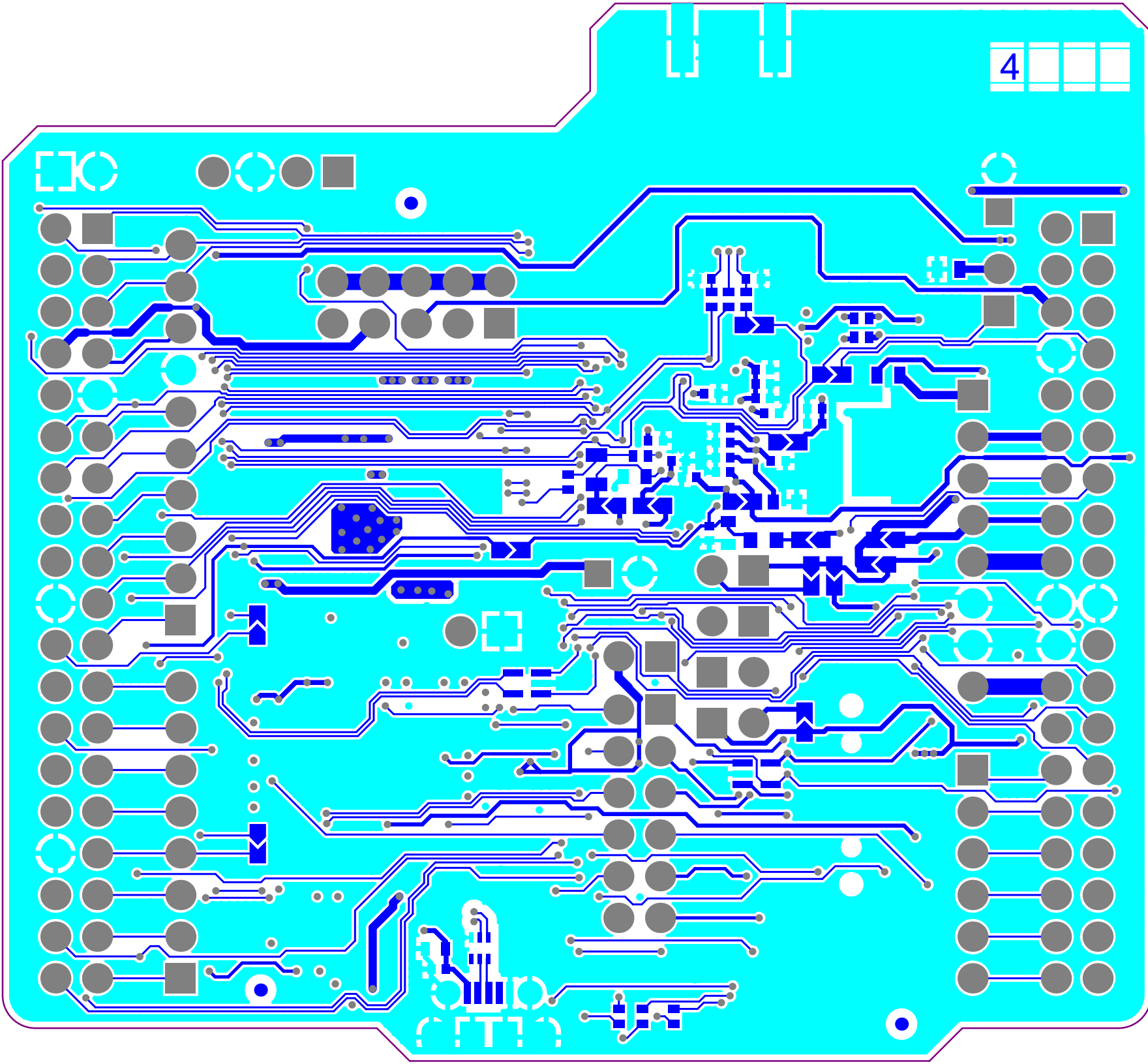
Project: NUCLEO73 STM32WL5		
Layer: Top Layer	Gerber: .GTL	
Variant: [No Variations]	Ref: MB1389	
Date: 20-April-23	Rev: D	




Project: NUCLEO73 STM32WL5		
Layer: Signal Layer 1	Gerber: .G1	
Variant: [No Variations]	Ref: MB1389	
Date: 20-April-23	Rev: D	



Project: NUCLEO73 STM32WL5		
Layer: Signal Layer 2	Gerber: .G2	
Variant: [No Variations]	Ref: MB1389	
Date: 20-April-23	Rev: D	



Project: NUCLEO73 STM32WL5		
Layer: Bottom Layer	Gerber:.GBL	
Variant: [No Variations]	Ref: MB1389	
Date: 20-April-23	Rev: D	



Project: NUCLEO73 STM32WL5

Layer: Bottom Solder

Variant: [No Variations]

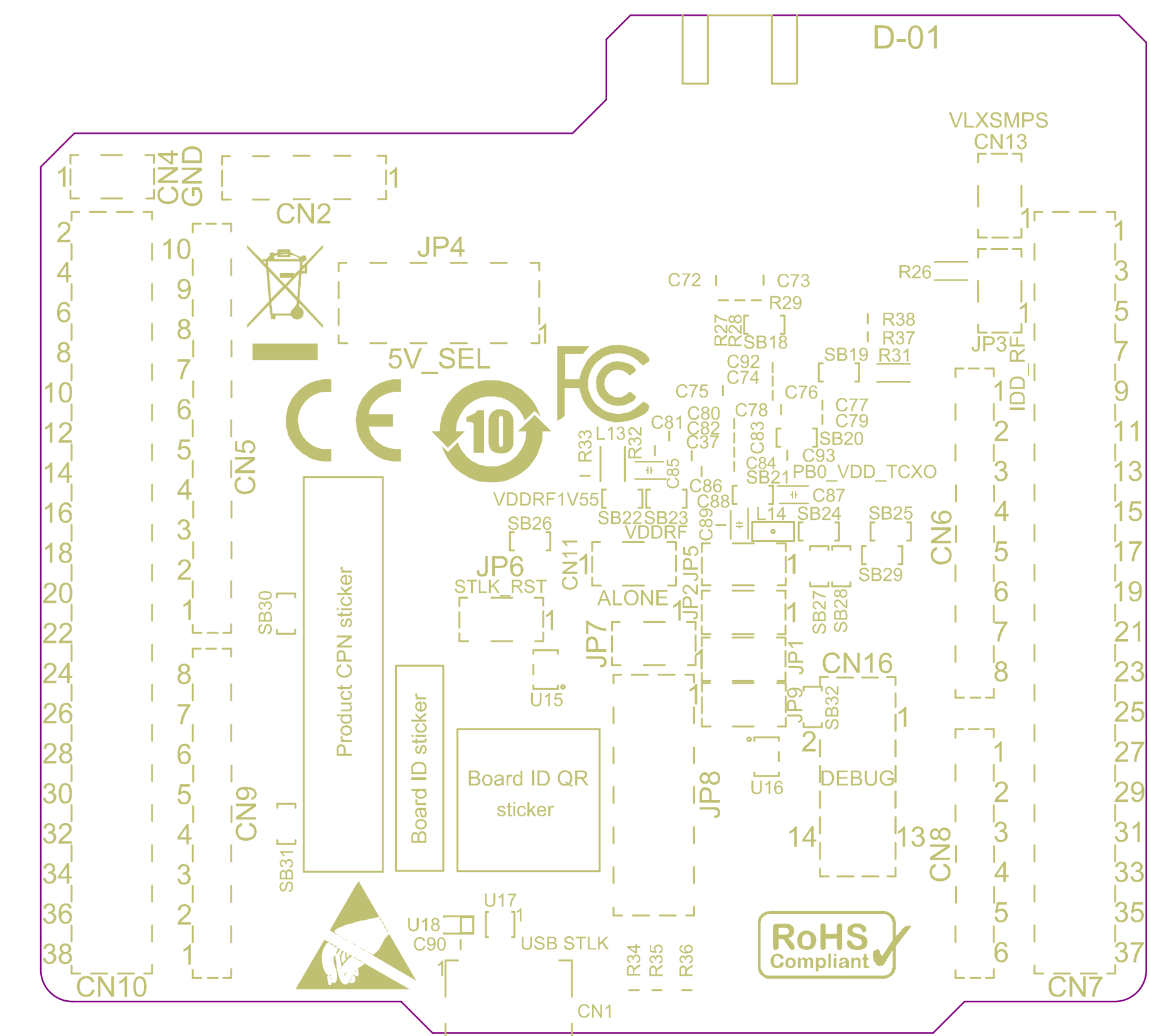
Date: 20-April-23


Gerber:.GBS

Ref: MB1389

Rev: D





Project: NUCLEO73 STM32WL5		
Layer: Bottom Overlay	Gerber:.GBO	
Variant: [No Variations]	Ref: MB1389	
Date: 20-April-23	Rev: D	

THE COMPONENTS WITH PLATED THROUGH HOLE (PTH) MAY BE WELDED (CABLED) IN "PIN-IN-PASTE" MODE (IF NECESSARY)

""BOTTOM PASTE""

PCB SPECIFICATIONS :

A. MATERIAL :

FR-4

☐TG-170

☒TG-150

☐TG-140

B. MATERIAL FAMILY :

N/A

C. SOLDERMASK COLOR :

☐GREEN

☒WHITE

☐RED

☐BLACK

D. SILKSCREEN COLOR :

☐WHITE

☐YELLOW

☐BLACK

☒Blue ink PANTONE 2955

E. SURFACE FINISH :

☒ENIG

☐IMMERSION SILVER

☐IMMERSION TIN

☐HASL

☐HASL (PB-FREE)

☐GOLDEN FINGER

F. IMPEDANCE CONTROL :

☐NO

☒YES (SEE IMPEDANCE TABLE FOR DETAIL INFORMATION)

G. THROUGH VIA :

PLUG THE VIAS WHICH ARE COVERED WITH SOLDERMASK ONE OR TWO SIDE.

PLUG MATERIAL : ☒SOLDERMASK

☐NON-CONDUCTIVE EPOXY.

H. STACK-UP :

SEE LAYER STACK-UP SEQUENCE FOR OVERALL THICKNESS.

PCB : TYPE 3

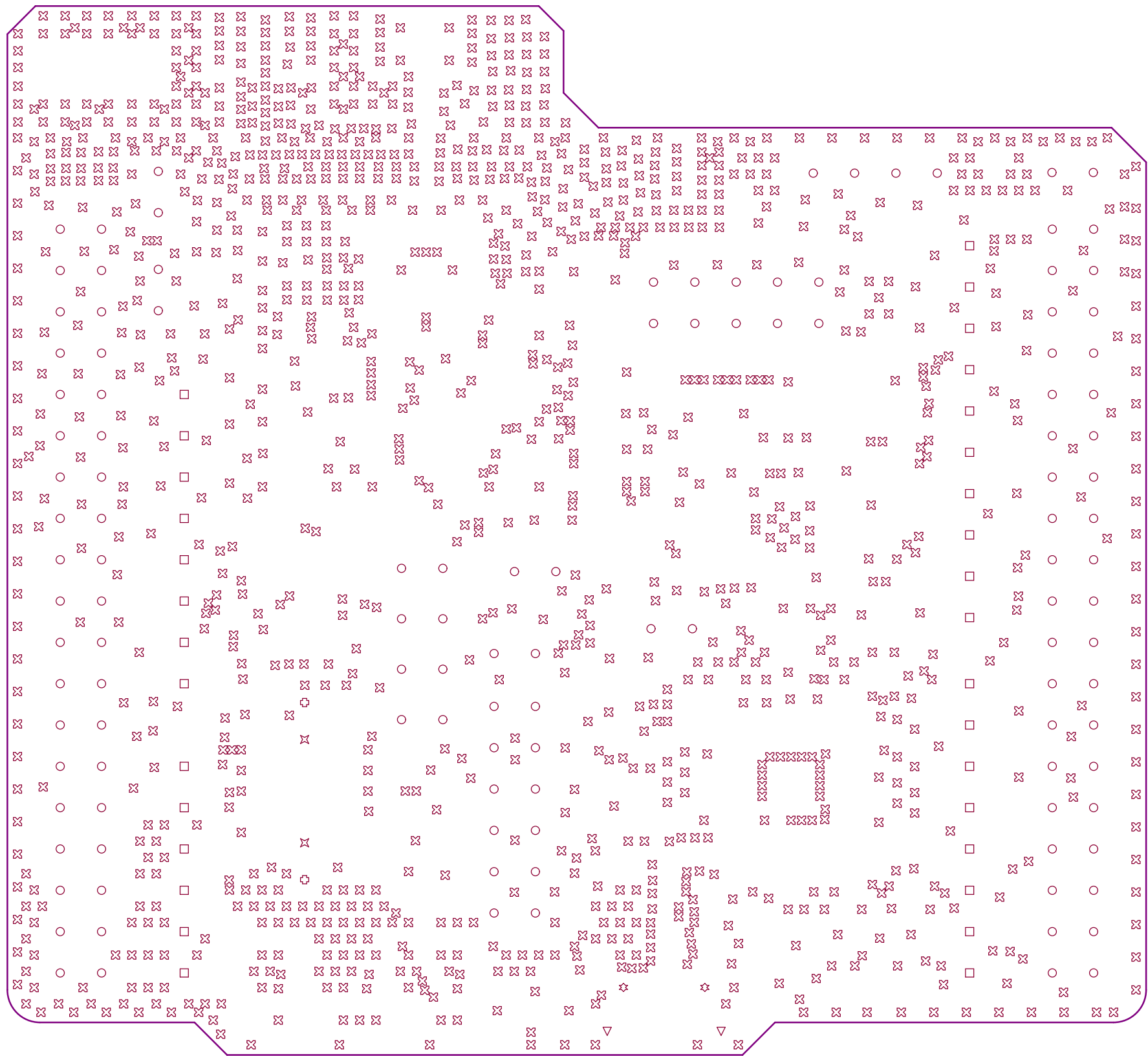
ASPECT-RATIO, AXE Z :
6:1 to 8:1
LEVEL "B"

MINIMUM PARAMETERS

DEFAULT
TRACKS : 0.120mm
GAPS : 0.120mm


EXCEPT BGA PITCH 0.5MM U13
TRACKS : 0.090mm
GAPS : 0.090mm

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0,020mm	3,5	
3	Top Layer	Copper	0,035mm		
4	Dielectric 1	1080HR RC68	0,076mm	4,18	
5	Signal Layer 1	Copper	0,035mm		
6	Dielectric 2	7 x 7628	1,268mm	4,74	
7	Signal Layer 2	Copper	0,035mm		
8	Dielectric 3	1080HR RC68	0,076mm	4,18	
9	Bottom Layer	Copper	0,035mm		
10	Bottom Solder	Solder Resist	0,020mm	3,5	
11	Bottom Overlay				



Symbol	Count	Hole Size	Plated	Hole Type	Drill Layer Pair	Via/Pad	Pad Shape	Hole Length	Routed Path Length
▽	2	0,600mm (23,62mil)	PTH	Slot	Top Layer - Bottom Layer	Pad	Rounded	1,300mm (51,18mil)	0,700mm (27,56mil)
☆	2	0,900mm (35,43mil)	PTH	Round	Top Layer - Bottom Layer	Pad	Rounded	-	-
✧	2	0,970mm (38,19mil)	NPTH	Round	Top Layer - Bottom Layer	Pad	Rounded	-	-
⊕	2	1,190mm (46,85mil)	NPTH	Round	Top Layer - Bottom Layer	Pad	Rounded	-	-
□	32	1,100mm (43,31mil)	PTH	Round	Top Layer - Bottom Layer	Pad	Rounded	-	-
○	122	1,000mm (39,37mil)	PTH	Round	Top Layer - Bottom Layer	Pad	(Mixed)	-	-
⊗	1295	0,200mm (7,87mil)	PTH	Round	Top Layer - Bottom Layer	Via	Rounded	-	-
	1457 Total								

Slot definitions : Routed Path Length = Calculated from tool start centre position to tool end centre position.
Hole Length = Routed Path Length + Tool Size = Slot length as defined in the PCB layout

Project: NUCLEO73 STM32WL5		
Layer: Drill Drawing	Gerber: .DRL	
Variant: [No Variations]	Ref: MB1389	
Date: 20-April-23	Rev: D	