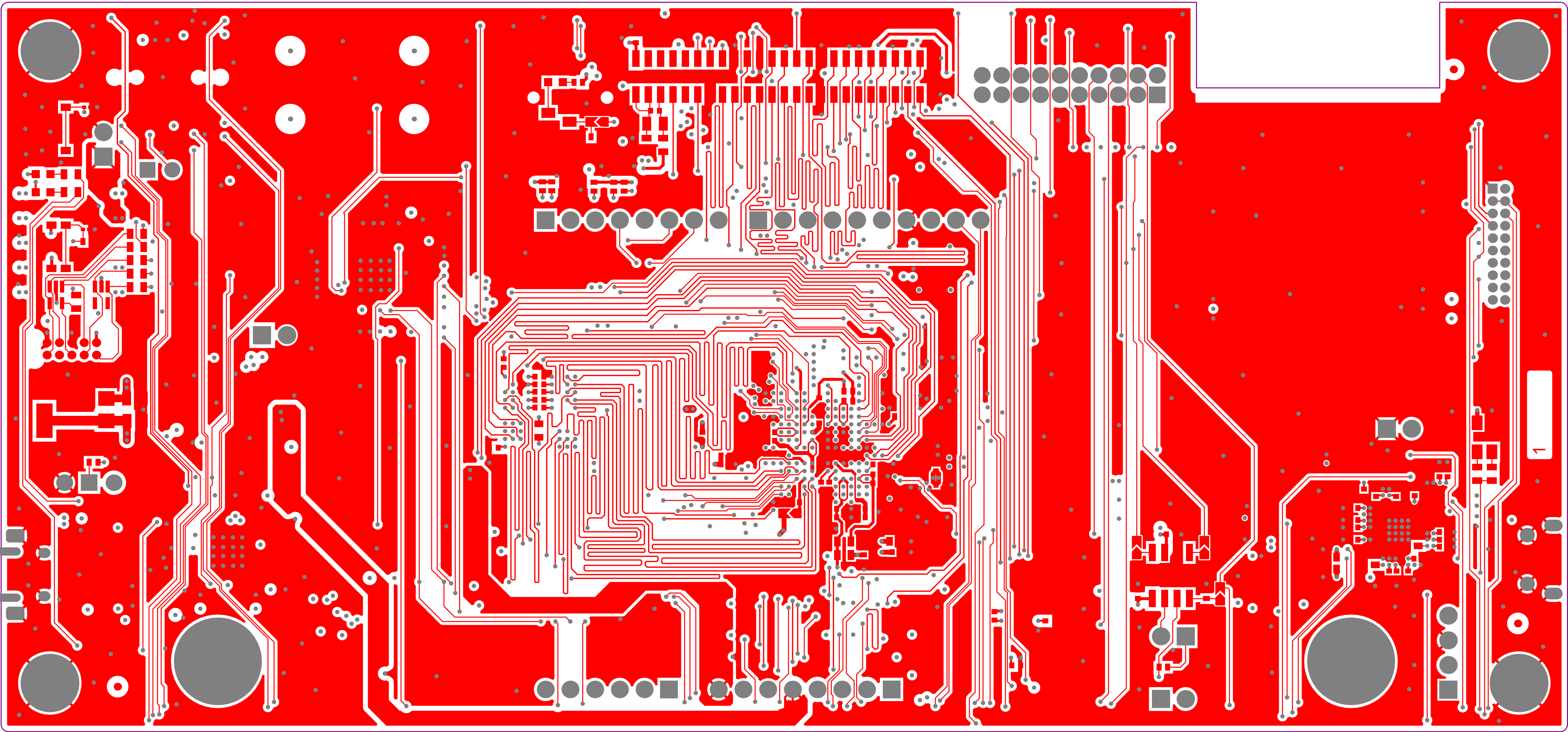


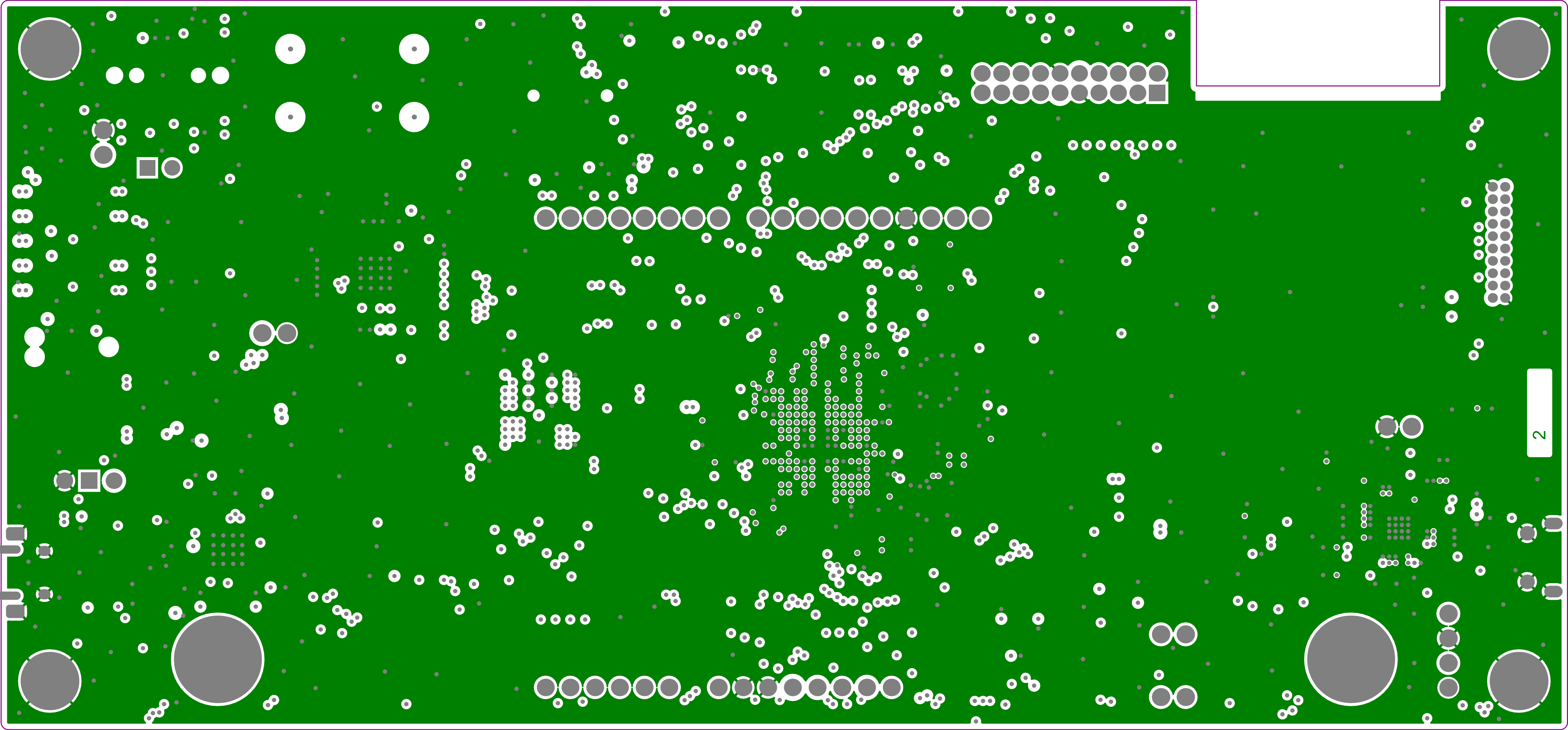
Top Overlay

.GTO



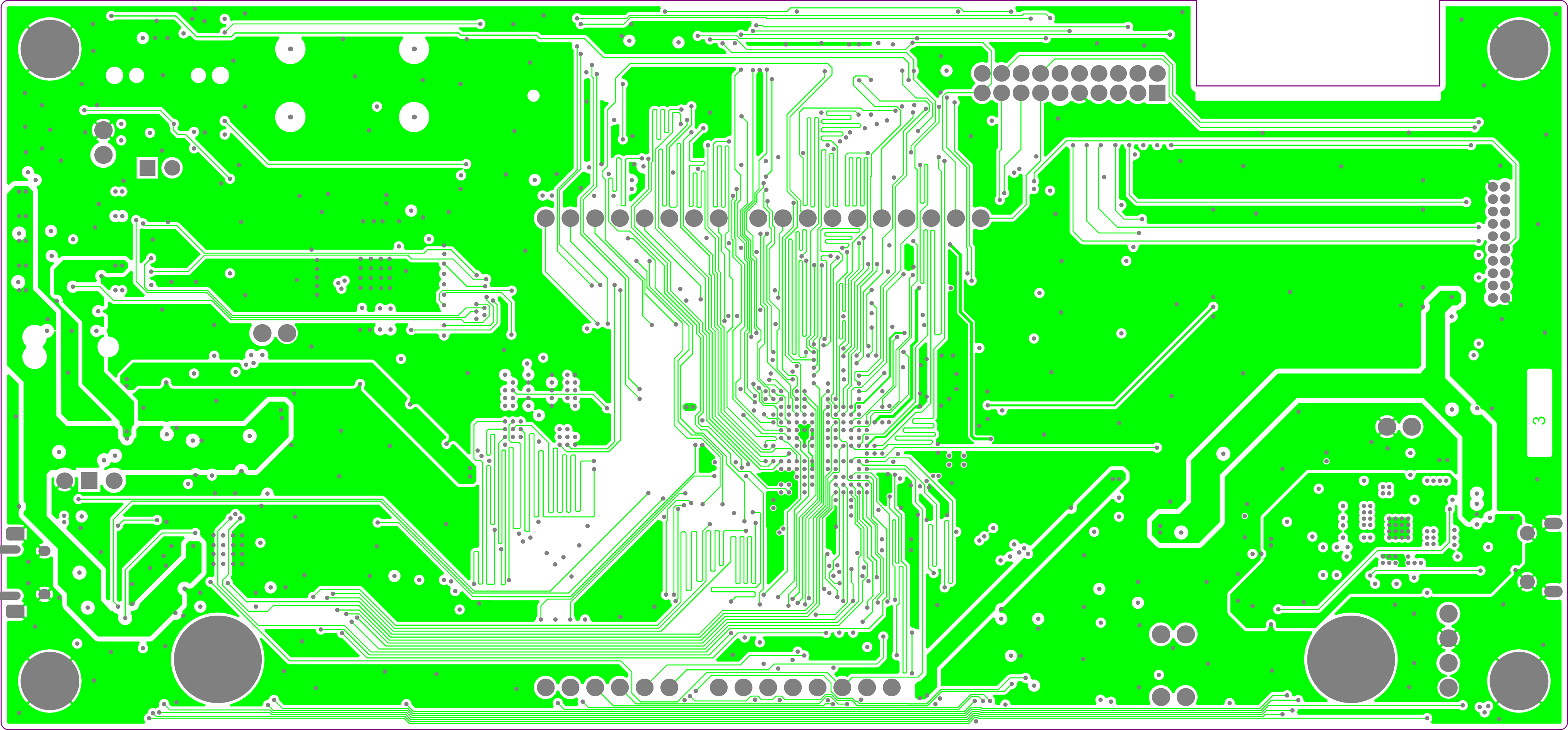
Top Layer

.GTL



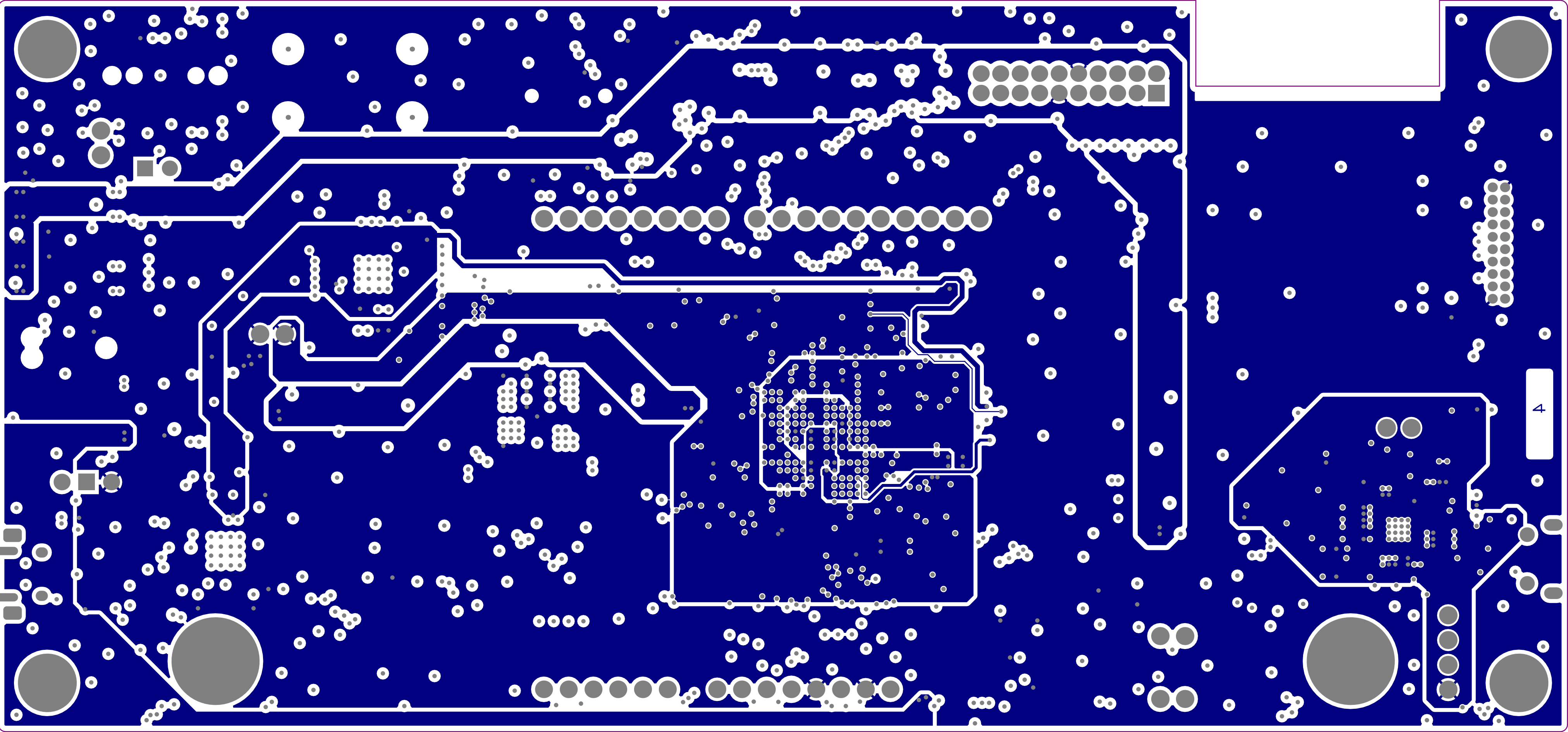
Signal Layer 1

.G1



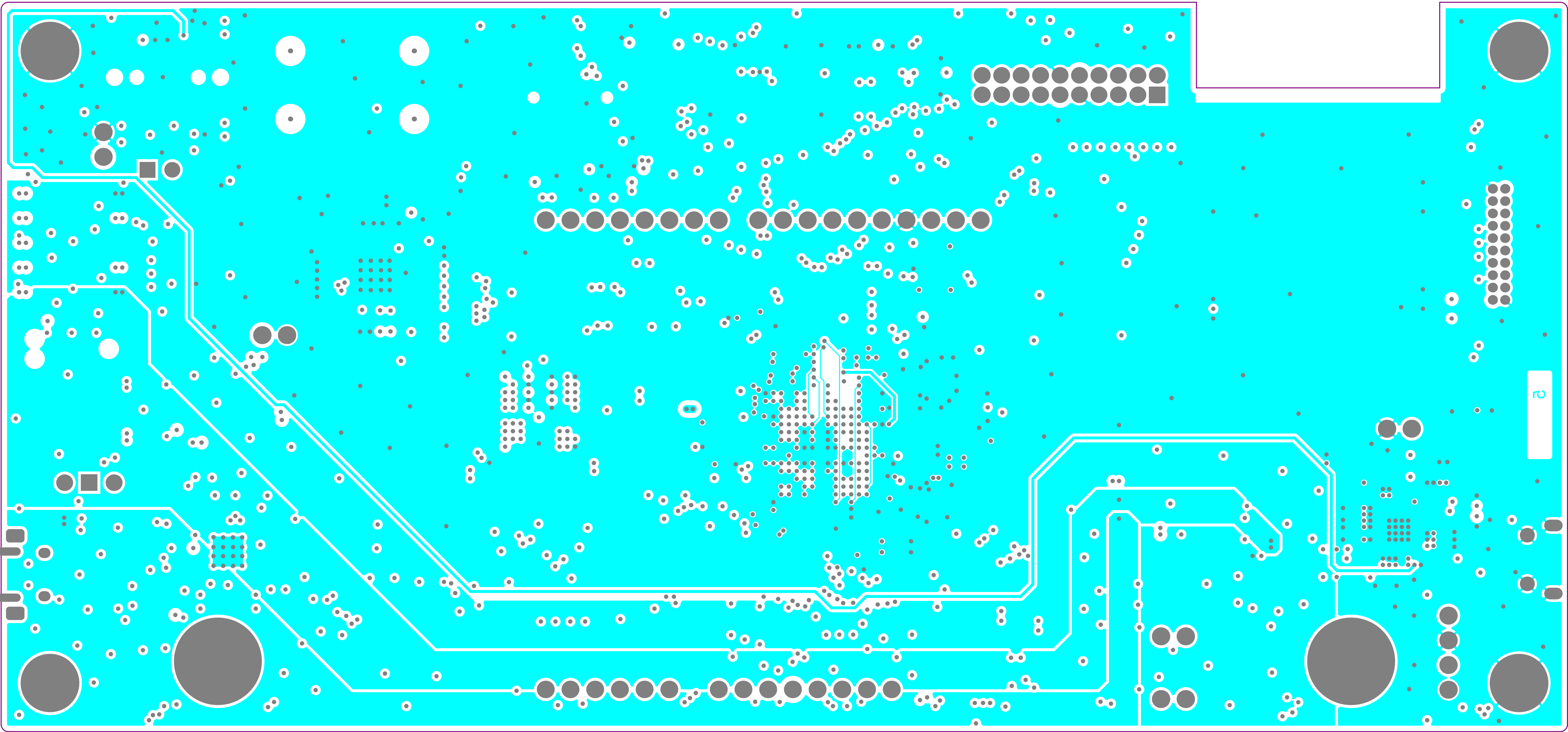
Signal Layer 2

.G2



Signal Layer 3

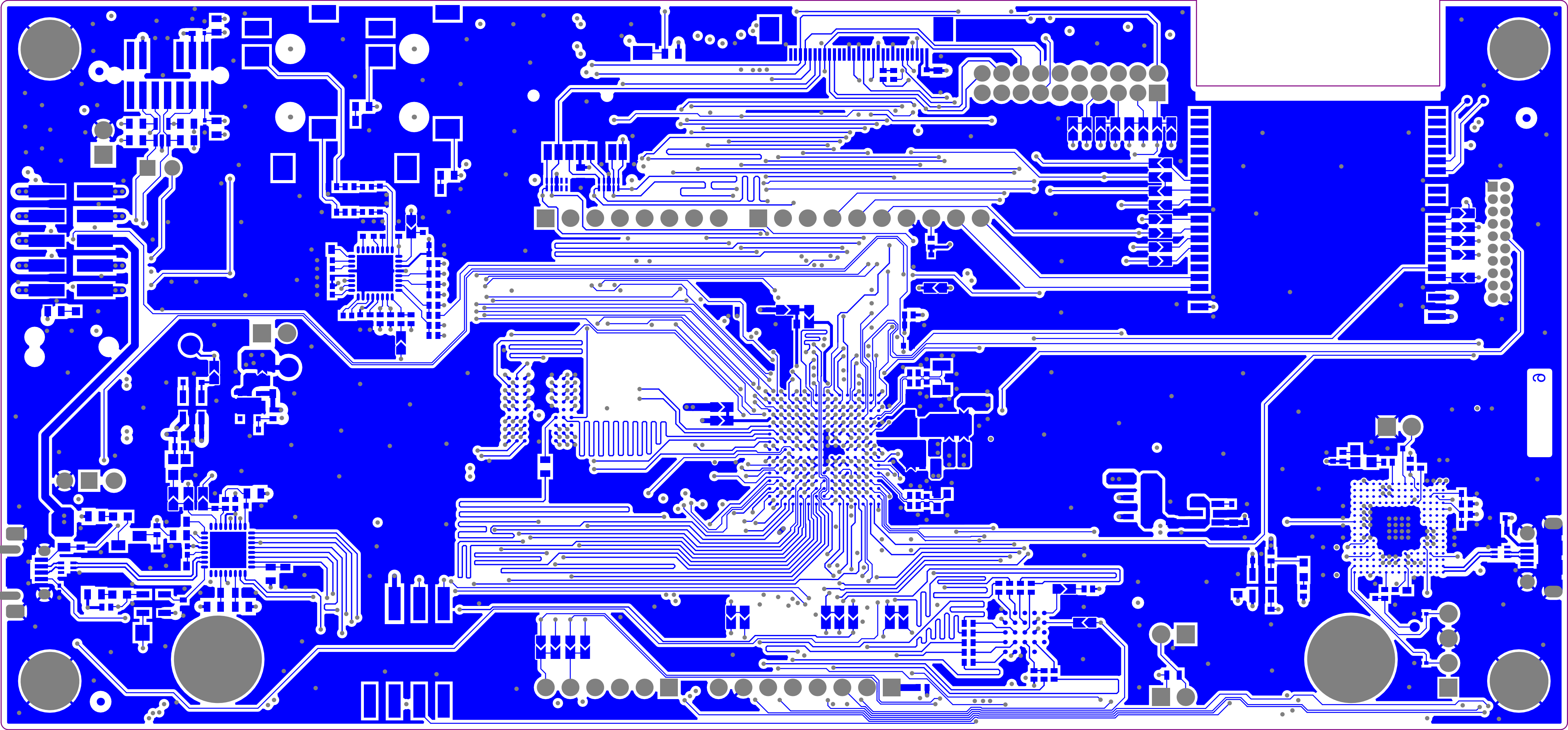
.G3

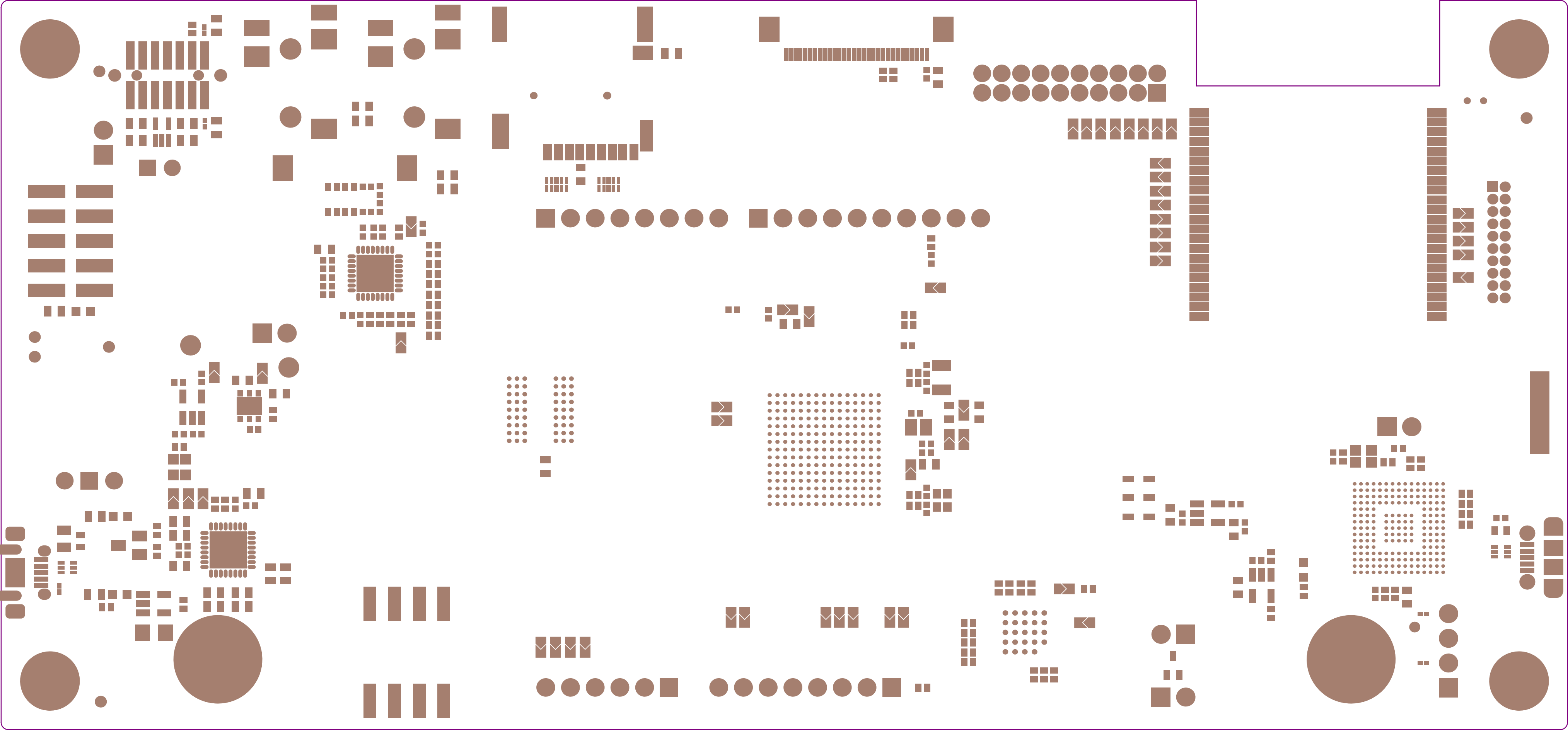


Signal Layer 4

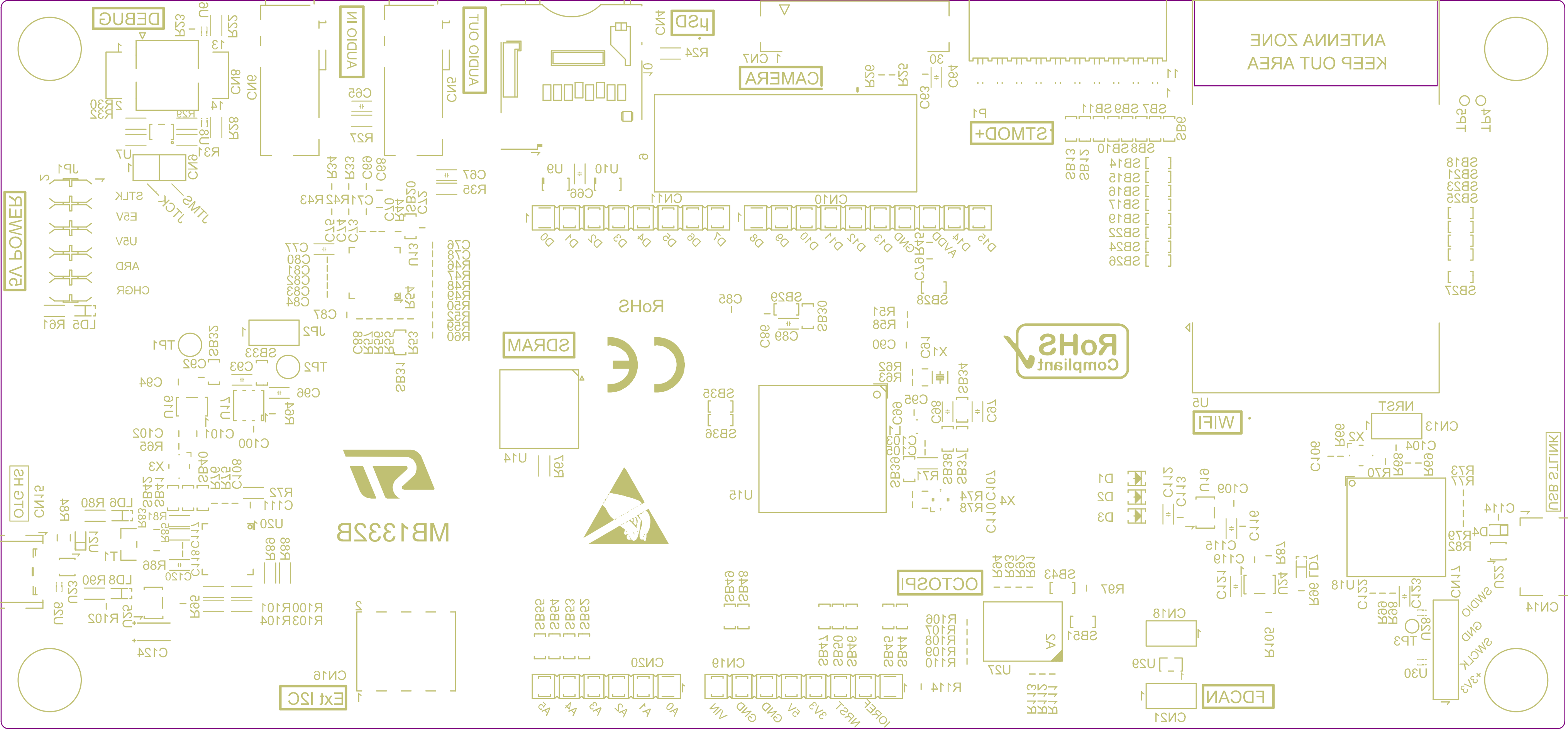
.G4

Bottom Layer .GBL





Bottom Solber .GBS



Bottom Overlay
.GBO

PCB SPECIFICATIONS :

A. MATERIAL :

B. MATERIAL FAMILY :

C. SOLDERMASK COLOR :

D. SILKSCREEN COLOR :

E. SURFACE FINISH :

F

IMPEDANCE CONTROL :

G. THROUGH VIA :

H

STACK-UP :

FR-4

N/A

☐GREEN

☒WHITE

☒ENIG

☐HASL

☐NO

☐TG-170

☒TG-150

☐TG-140

☐WHITE

☐YELLOW

☐IMMERSION SILVER

☐HASL (PB-FREE)

☒YES (SEE IMPEDANCE TABLE FOR DETAIL INFORMATION)

☐BLACK

☐Blue ink PANTONE 2955

☐IMMERSION TIN

☐GOLDEN FINGER

PLUG THE VIAS WHICH ARE COVERED WITH SOLDERMASK ONE OR TWO SIDE.

PLUG MATERIAL :

☒SOLDERMASK

☐NON-CONDUCTIVE EPOXY.

SEE LAYER STACK-UP SEQUENCE FOR OVERALL THICKNESS.

PCB : TYPE 3

ASPECT-RATIO, AXE Z :
6:1 to 8:1
LEVEL "B"

MINIMUM PARAMETERS

DEFAULT
TRACKS : 0.1mm
GAPS : 0.1mm

IMPEDANCE TABLE : SDRAM, SD CARD, ULPI, CAMERA					
LAYER	TRACE (mm)	SPACING (mm)	IMPEDANCE (Single ended)	IMPEDANCE (Differential)	TOL.
TOP/BOTTOM	0.127	n/a	55 ohm	n/a	+/- 15%
LAYER 3	0.102	n/a	55 ohm	n/a	+/- 15%

IMPEDANCE TABLE USB OTG HS, USB HS STLINK V3E					
LAYER	TRACE (mm)	SPACING (mm)	IMPEDANCE (Single ended)	IMPEDANCE (Differential)	TOL.
TOP/BOTTOM	0.155	0.226	n/a	90 ohm	+/- 15%
LAYER 3	0.130	0.251	n/a	90 ohm	+/- 15%

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0,015mm	3,5	
3	Top Layer	Copper	0,042mm		
4	Dielectric 1	FR-4	0,099mm	4,2	
5	Signal Layer 1	Copper	0,035mm		
6	Dielectric 2		0,102mm	4,2	
7	Signal Layer 2	Copper	0,035mm		
8	Dielectric 3		0,946mm	4,2	
9	Signal Layer 3	Copper	0,035mm		
10	Dielectric 4		0,102mm	4,2	
11	Signal Layer 4	Copper	0,035mm		
12	Dielectric 5		0,099mm	4,2	
13	Bottom Layer	Copper	0,042mm		
14	Bottom Solder	Solder Resist	0,015mm	3,5	
15	Bottom Overlay				

Symbol	Count	Hole Size	Plated	Hole Type	Drill Layer Pair	Hole Length	Routed Path Length
O	1170	0,200mm (7,87mil)	PTH	Round	Top Layer - Bottom Layer	-	-
T	4	0,600mm (23,62mil)	PTH	Slot	Top Layer - Bottom Layer	1,300mm (51,18mil)	0,700mm (27,56mil)
U	2	0,650mm (25,59mil)	PTH	Slot	Top Layer - Bottom Layer	0,850mm (33,47mil)	0,200mm (7,88mil)
R	1	0,650mm (25,59mil)	NPTH	Round	Top Layer - Bottom Layer	-	-
S	1	0,700mm (27,56mil)	NPTH	Round	Top Layer - Bottom Layer	-	-
Q	20	0,700mm (27,56mil)	PTH	Round	Top Layer - Bottom Layer	-	-
U	2	0,850mm (33,47mil)	NPTH	Slot	Top Layer - Bottom Layer	2,425mm (95,47mil)	1,575mm (62,01mil)
K	57	0,900mm (35,43mil)	PTH	Round	Top Layer - Bottom Layer	-	-
⌘	2	0,970mm (38,19mil)	NPTH	Round	Top Layer - Bottom Layer	-	-
N	16	1,000mm (39,37mil)	PTH	Round	Top Layer - Bottom Layer	-	-
O	3	1,100mm (43,31mil)	NPTH	Round	Top Layer - Bottom Layer	-	-
▽	2	1,190mm (46,85mil)	NPTH	Round	Top Layer - Bottom Layer	-	-
M	4	2,000mm (78,74mil)	NPTH	Round	Top Layer - Bottom Layer	-	-
P	4	3,500mm (137,80mil)	PTH	Round	Top Layer - Bottom Layer	-	-
□	2	4,500mm (177,17mil)	PTH	Round	Top Layer - Bottom Layer	-	-
	1290 Total						

Slot definitions : Routed Path Length = Calculated from tool start centre position to tool end centre position.
Hole Length = Routed Path Length + Tool Size = Slot length as defined in the PCB layout

A detailed drill drawing (DRL) of a PCB. The drawing shows a rectangular board with various sized holes (vias and through-holes) distributed across its surface. Some holes are marked with letters like 'P', 'H', 'R', 'S', 'K', 'N', 'U', 'T', 'M', and 'Q'. The drawing is a technical representation of the physical drilling process, showing the exact locations and sizes of all holes to be drilled into the board material.

Drill Drawing

.DRL