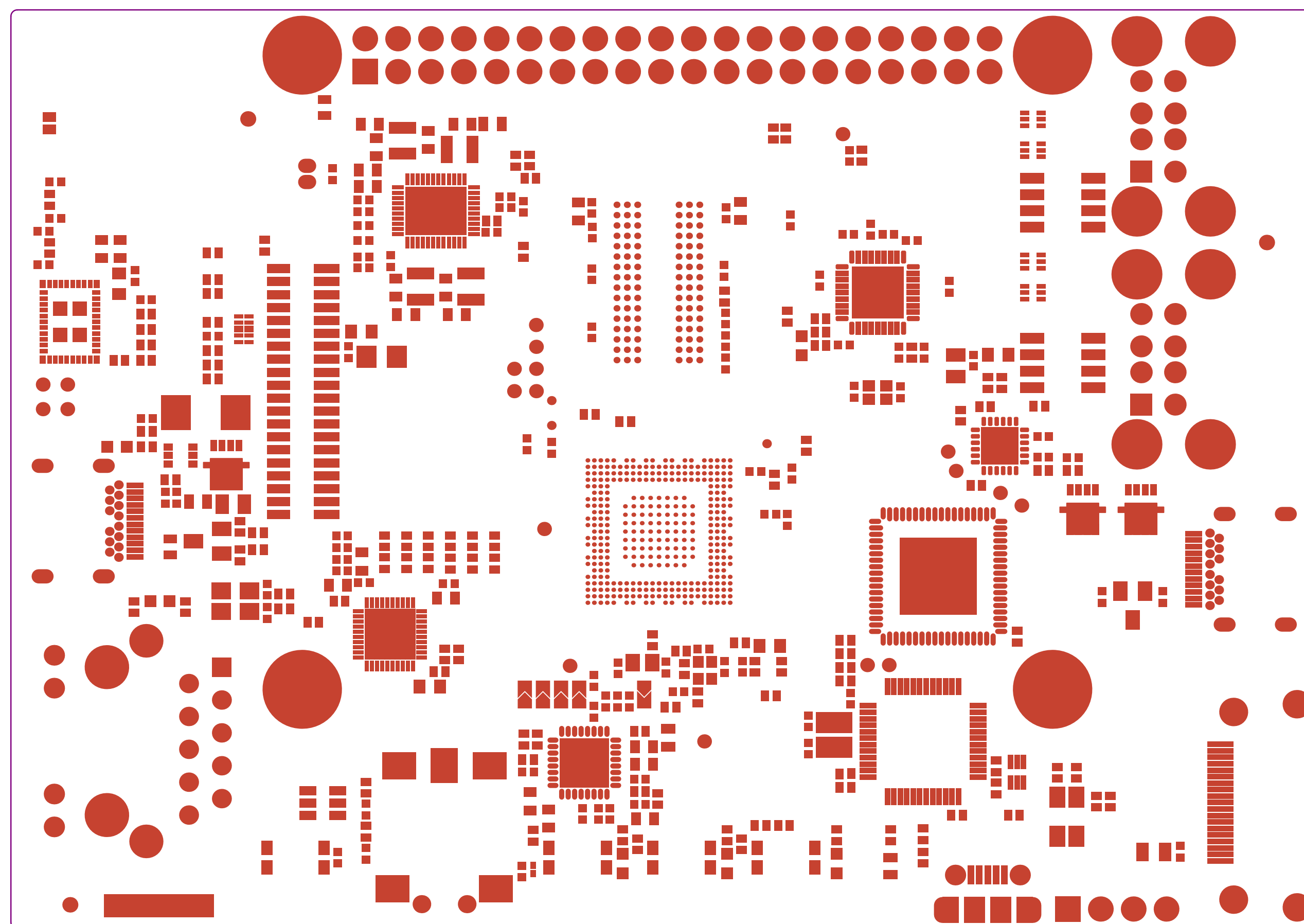


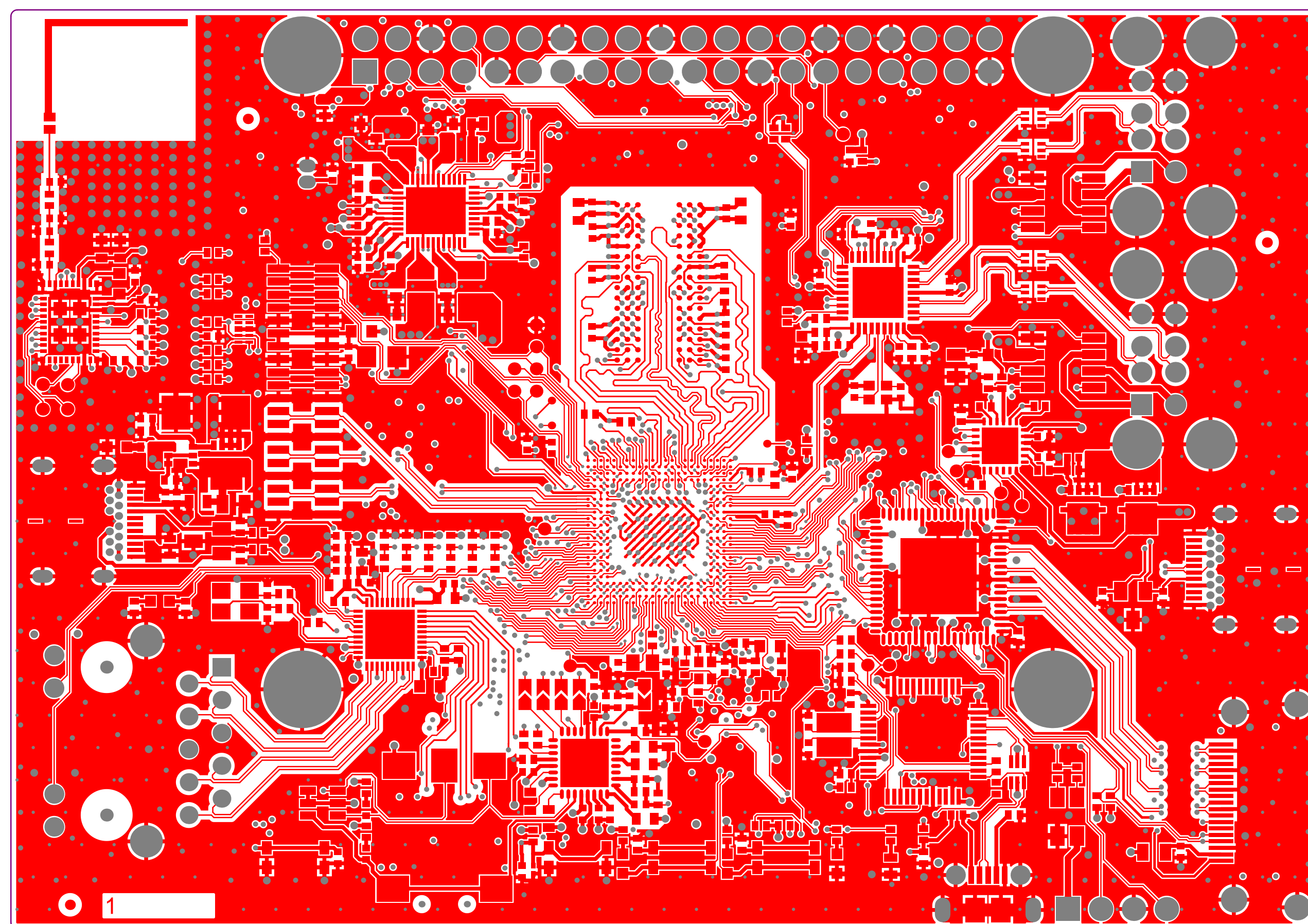
Top Overlay

.GTO



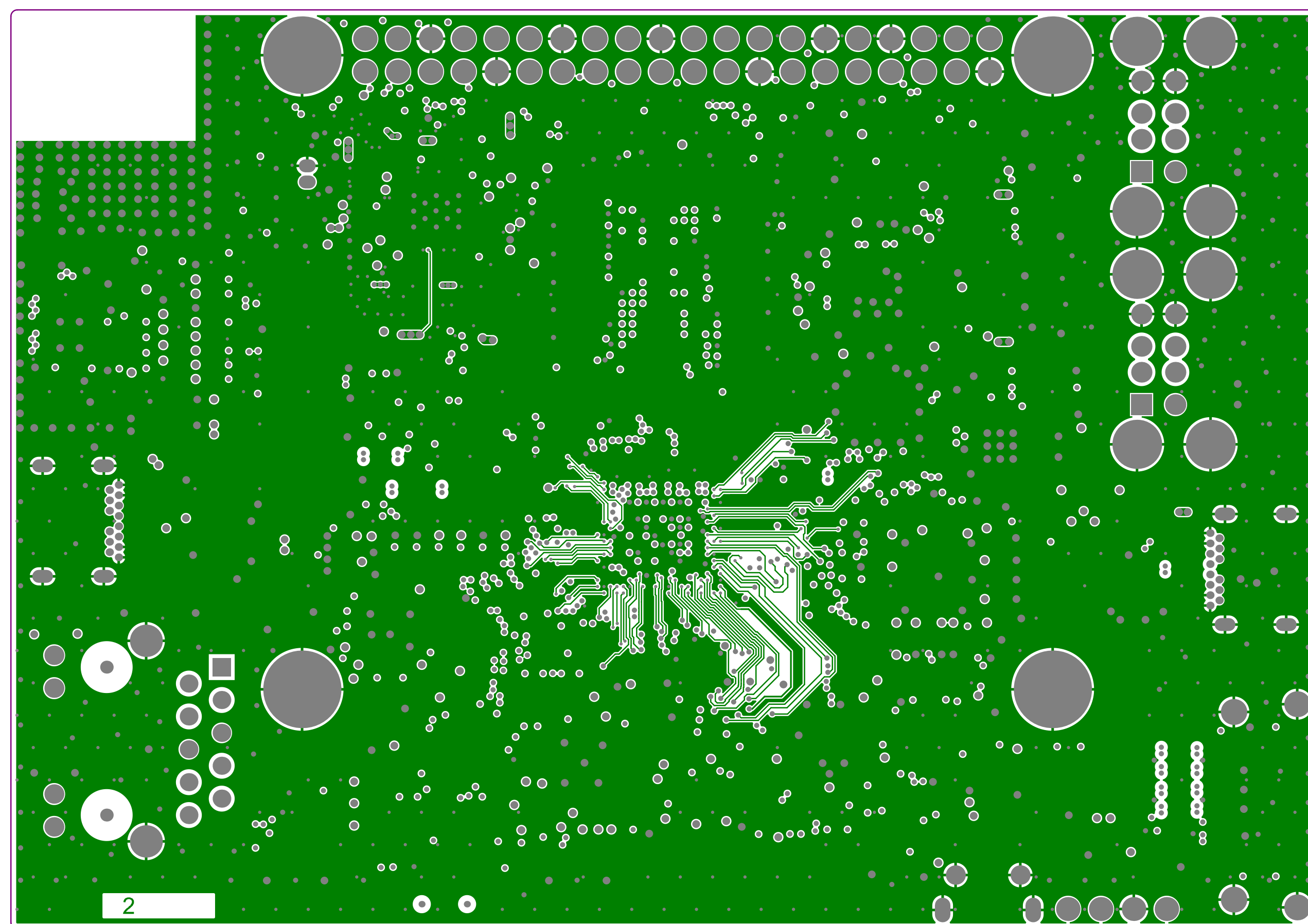
Top Solder

.GTS



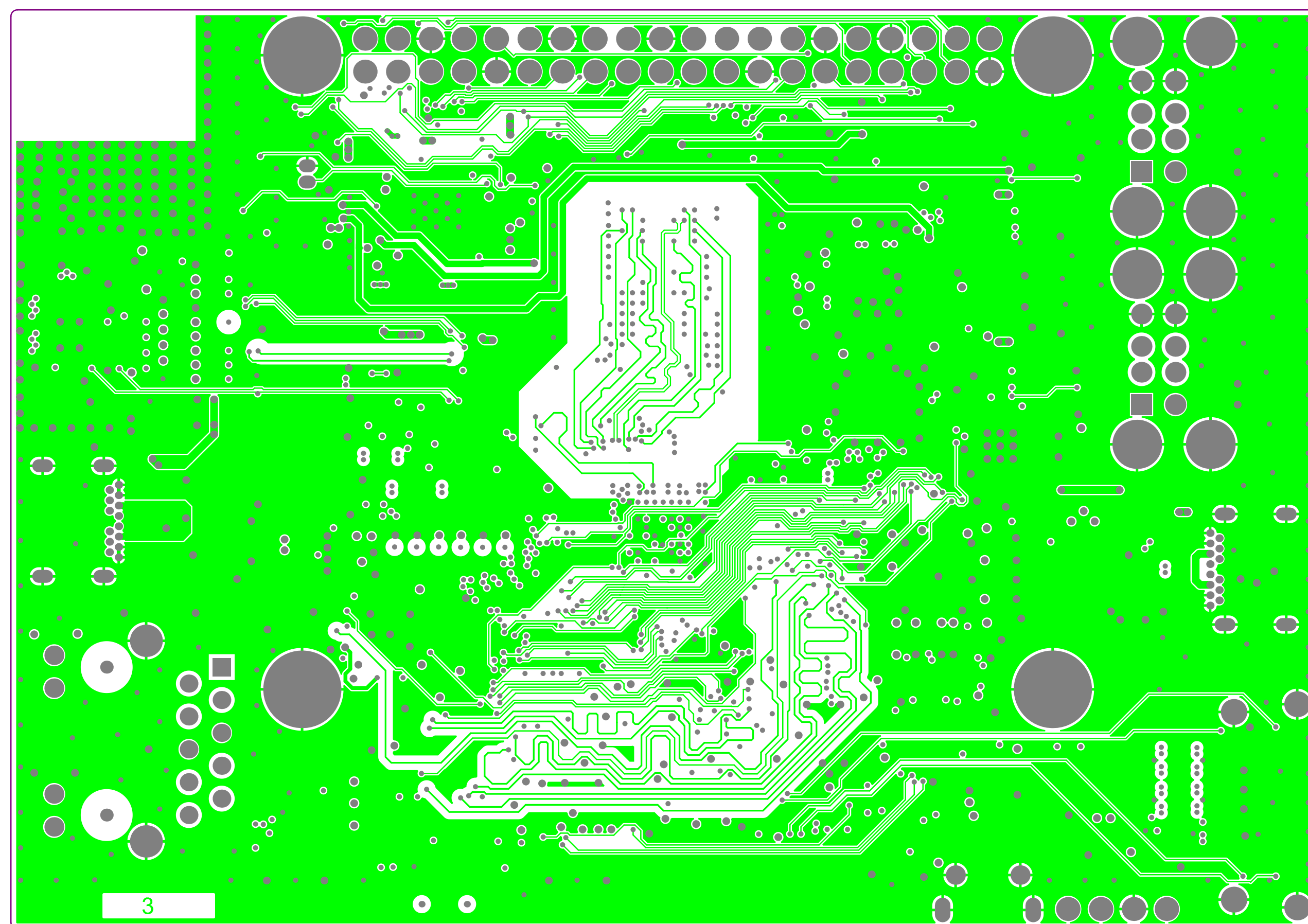
Top Layer

.GTL



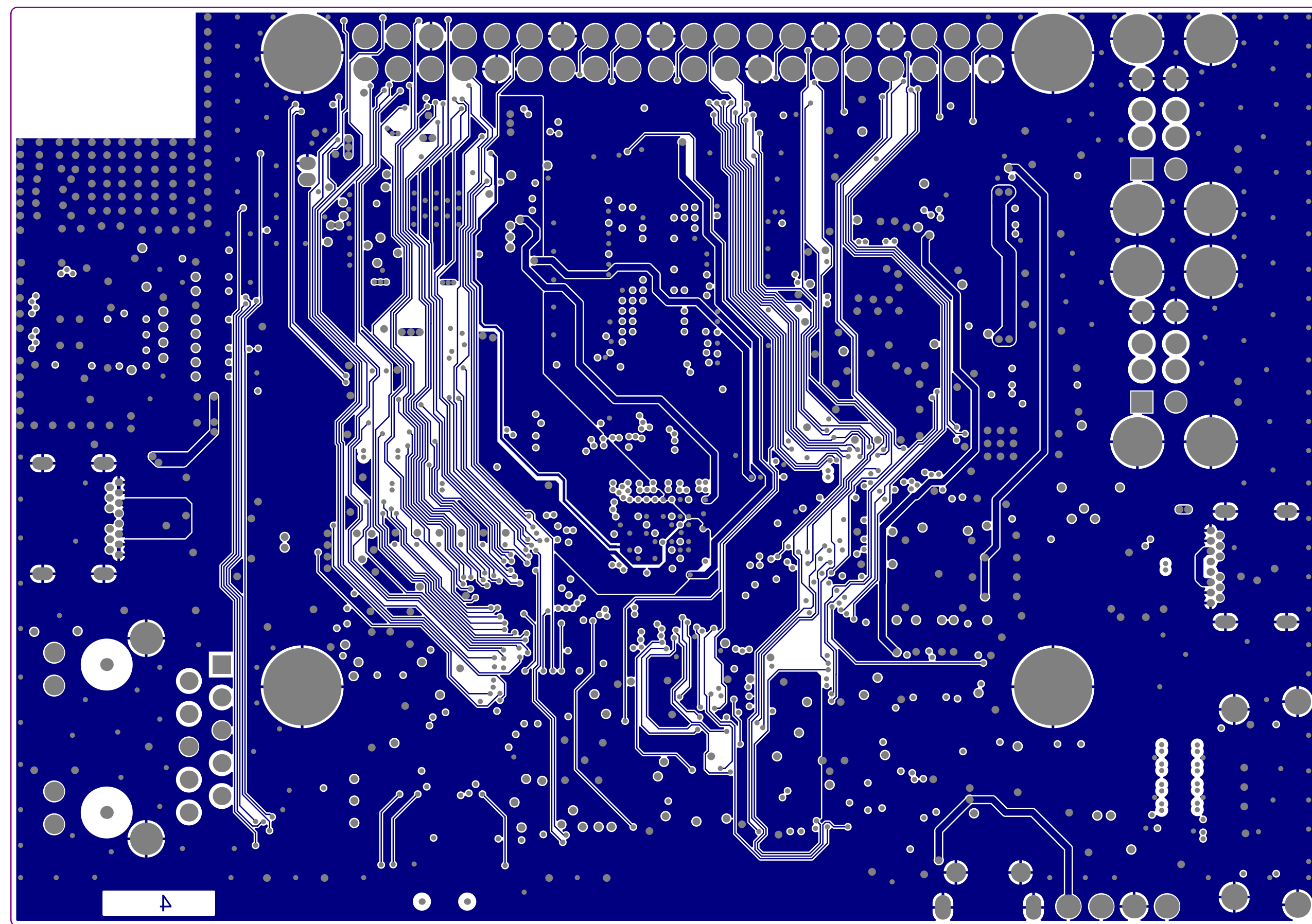
Signal Layer 1

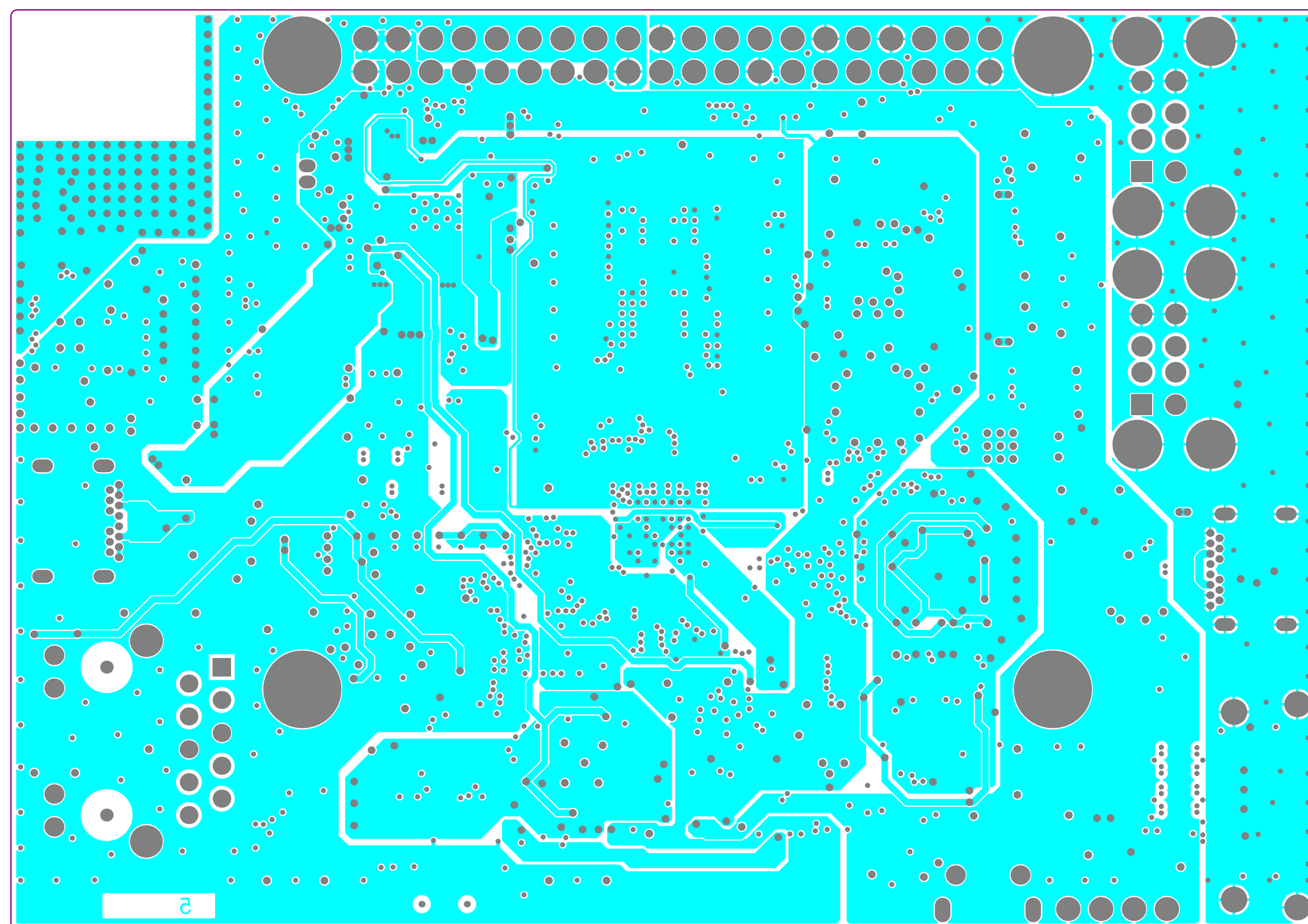
.G1



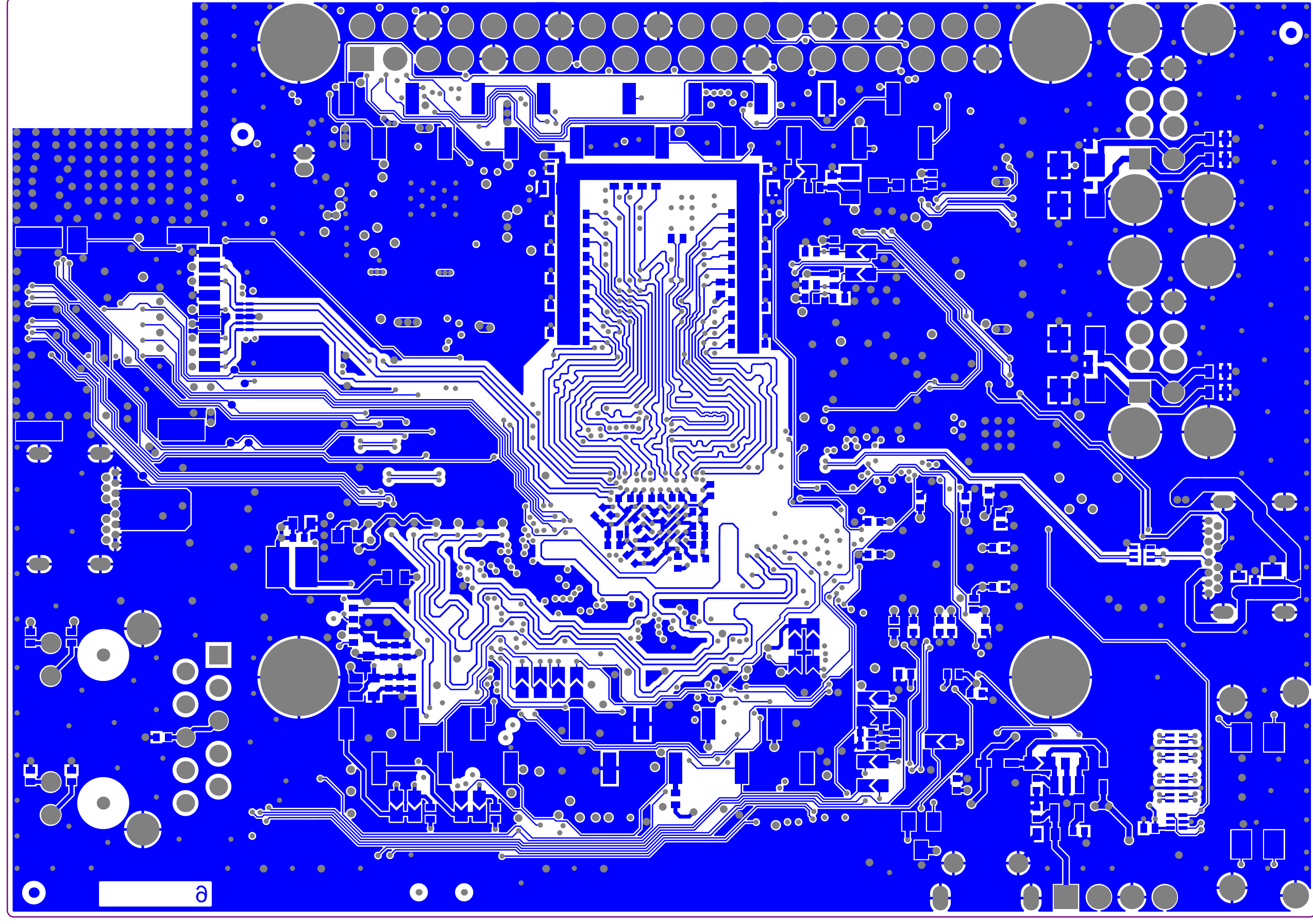
Signal Layer 2

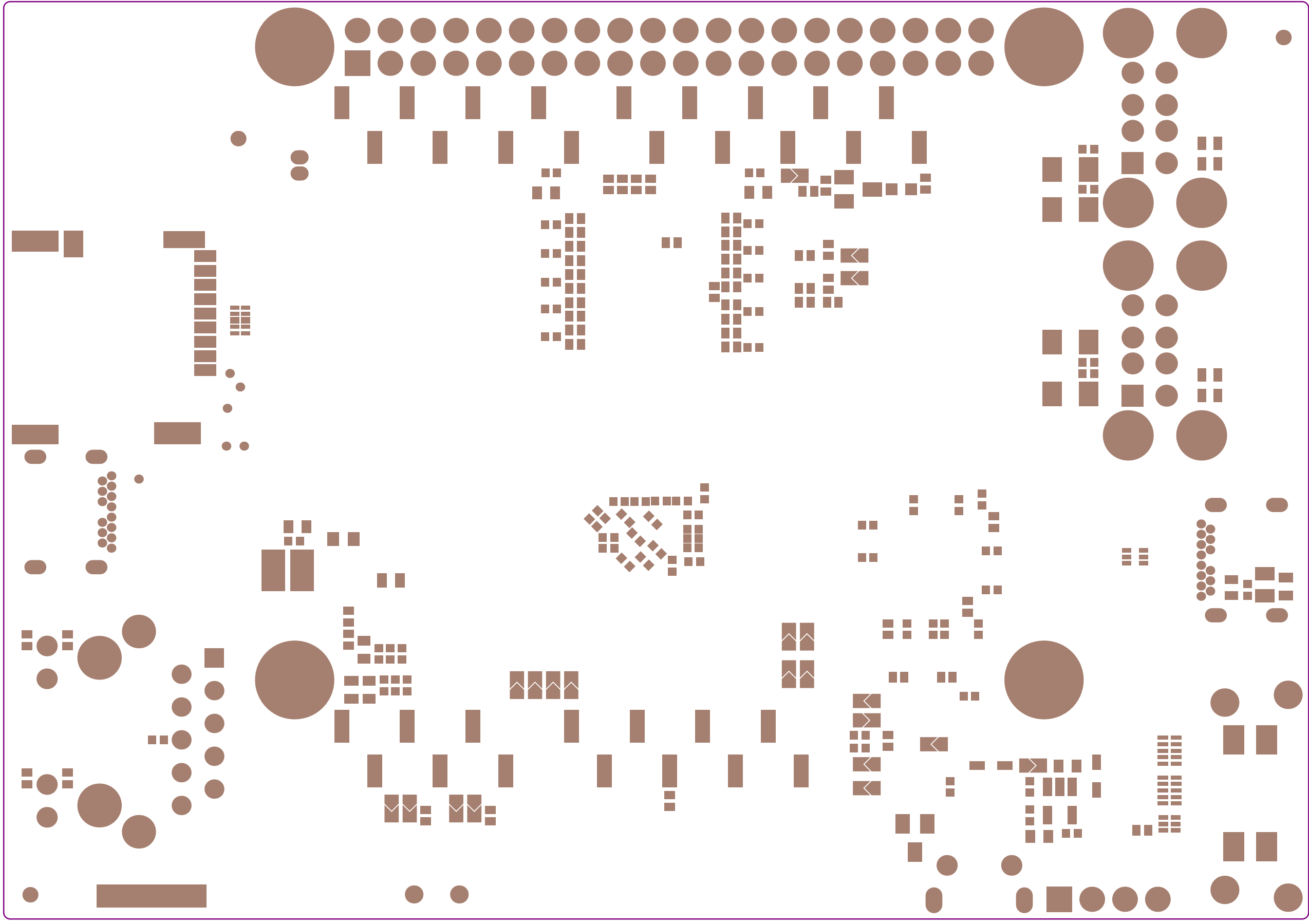
.G2





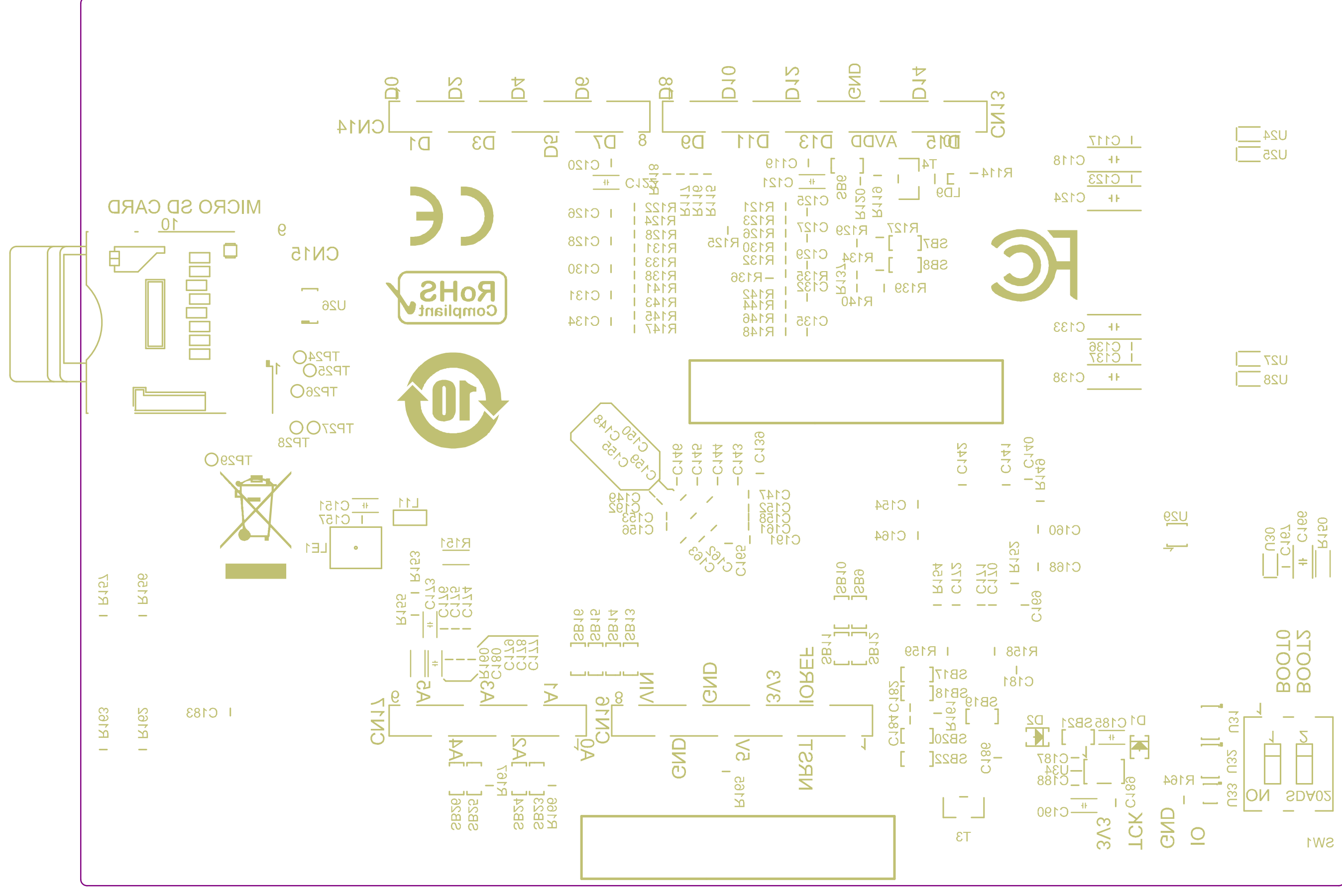
Bottom Layer
.GBL





.GBS

Bottom Solder



PCB SPECIFICATIONS :

A. MATERIAL :

B. MATERIAL FAMILY :

C. SOLDERMASK COLOR :

D. SILKSCREEN COLOR :

E. SURFACE FINISH :

F. IMPEDANCE CONTROL :

G. THROUGH VIA :

H. STACK-UP :

FR-4

N/A

☒BLUE

☐WHITE

☐YELLOW

☒WHITE

☒ENIG

☐HASL

☐NO

☐TG-170

☒TG-150

☐TG-140

☐BLACK

☐Blue ink PANTONE 2955

☐IMMERSION SILVER

☐HASL (PB-FREE)

☒YES (SEE IMPEDANCE TABLE FOR DETAIL INFORMATION)

☐NON-CONDUCTIVE EPOXY.

SEE LAYER STACK-UP SEQUENCE FOR OVERALL THICKNESS.

PCB : TYPE 4

ASPECT-RATIO, AXE Z :
6:1 to 8:1
LEVEL "B"

MINIMUM PARAMETERS

DEFAULT
TRACKS : 0.090mm
GAPS : 0.090mm
MCU
TRACKS : 0.090mm
GAPS : 0.080mm

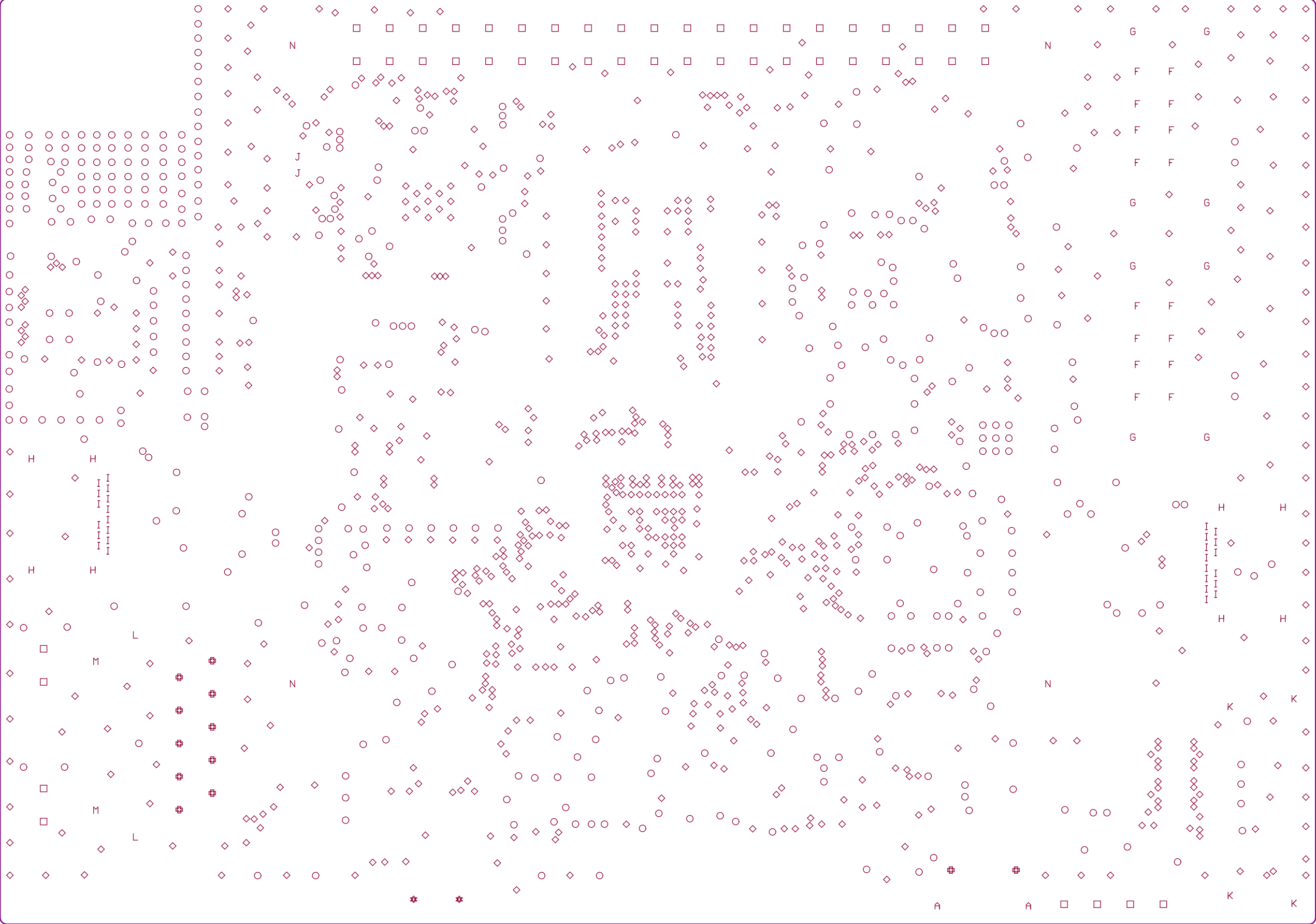
IMPEDANCE TABLE DDR					
LAYER	TRACE (mm)	SPACING (mm)	IMPEDANCE (Single ended)	IMPEDANCE (Differential)	TOL.
TOP	0.120	0.300	55 ohm	NA	+/- 10%
	0.100/0.130/0.100		NA	100 ohm	+/- 10%
LAYER 2	0.127	0.300	55 ohm	NA	+/- 10%
	0.090/0.140/0.090		NA	100 ohm	+/- 10%
BOTTOM	0.120	0.300	55 ohm	NA	+/- 10%
	0.100/0.130/0.100		NA	100 ohm	+/- 10%

IMPEDANCE TABLE SDMMC1					
LAYER	TRACE (mm)	SPACING (mm)	IMPEDANCE (Single ended)	IMPEDANCE (Differential)	TOL.
TOP/BOTTOM	0.130	0.260	50 ohm	NA	+/- 15%
LAYER 2	0.090	0.260	50 ohm	NA	+/- 15%

IMPEDANCE TABLE USB					
LAYER	TRACE (mm)	SPACING (mm)	IMPEDANCE (Single ended)	IMPEDANCE (Differential)	TOL.
TOP/BOTTOM	0.100	0.090	NA	90 ohm	+/- 15%

IMPEDANCE TABLE DSI					
LAYER	TRACE (mm)	SPACING (mm)	IMPEDANCE (Single ended)	IMPEDANCE (Differential)	TOL.
TOP/BOTTOM	0.100	0.130	NA	100 ohm	+/- 15%

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0,020mm	3,5	
3	Top Layer	Copper	0,035mm		
4	Dielectric 1	IT-180A 3313H	0,099mm	4,2	
5	Signal Layer 1	Copper	0,035mm		
6	Dielectric 2	IT-180A	0,130mm	4,2	
7	Signal Layer 2	Copper	0,035mm		
8	Dielectric 3	IT-180A 1080*2	0,885mm	4,25	
9	Signal Layer 3	Copper	0,035mm		
10	Dielectric 4	IT-180A	0,130mm	4,2	
11	Signal Layer 4	Copper	0,035mm		
12	Dielectric 5	IT-180A 3313H	0,099mm	4,2	
13	Bottom Layer	Copper	0,035mm		
14	Bottom Solder	Solder Resist	0,020mm	3,5	
15	Bottom Overlay				



Drill Drawing

.DRL

Symbol	Count	Hole Size	Plated	Hole Type	Drill Layer Pair	Hole Length	Routed Path Length
▽	530	0,100mm (3,94mil)	PTH	Round	Top Layer - Signal Layer 1	-	-
◇	912	0,200mm (7,87mil)	PTH	Round	Top Layer - Bottom Layer	-	-
○	452	0,300mm (11,81mil)	PTH	Round	Top Layer - Bottom Layer	-	-
I	28	0,400mm (15,75mil)	PTH	Round	Top Layer - Bottom Layer	-	-
J	2	0,500mm (19,69mil)	PTH	Round	Top Layer - Bottom Layer	-	-
H	8	0,600mm (23,62mil)	PTH	Slot	Top Layer - Bottom Layer	1,200mm (47,24mil)	0,600mm (23,62mil)
A	2	0,600mm (23,62mil)	PTH	Slot	Top Layer - Bottom Layer	1,300mm (51,18mil)	0,700mm (27,56mil)
⊕	12	0,900mm (35,43mil)	PTH	Round	Top Layer - Bottom Layer	-	-
F	16	0,920mm (36,22mil)	PTH	Round	Top Layer - Bottom Layer	-	-
□	48	1,000mm (39,37mil)	PTH	Round	Top Layer - Bottom Layer	-	-
☆	2	1,200mm (47,24mil)	NPTH	Round	Top Layer - Bottom Layer	-	-
K	4	1,350mm (53,15mil)	PTH	Round	Top Layer - Bottom Layer	-	-
L	2	1,700mm (66,93mil)	PTH	Round	Top Layer - Bottom Layer	-	-
G	8	2,330mm (91,73mil)	PTH	Round	Top Layer - Bottom Layer	-	-
M	2	3,200mm (125,98mil)	NPTH	Round	Top Layer - Bottom Layer	-	-
N	4	3,500mm (137,80mil)	PTH	Round	Top Layer - Bottom Layer	-	-
	2032 Total						

Slot definitions : Routed Path Length = Calculated from tool start centre position to tool end centre position.
Hole Length = Routed Path Length + Tool Size = Slot length as defined in the PCB layout