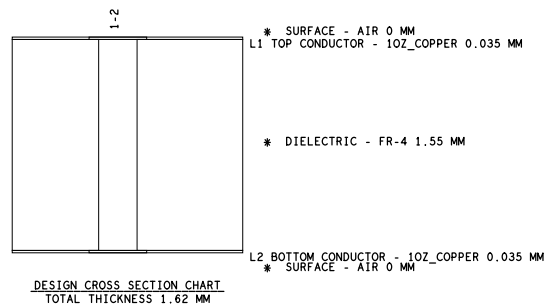


FABRICATION NOTES:

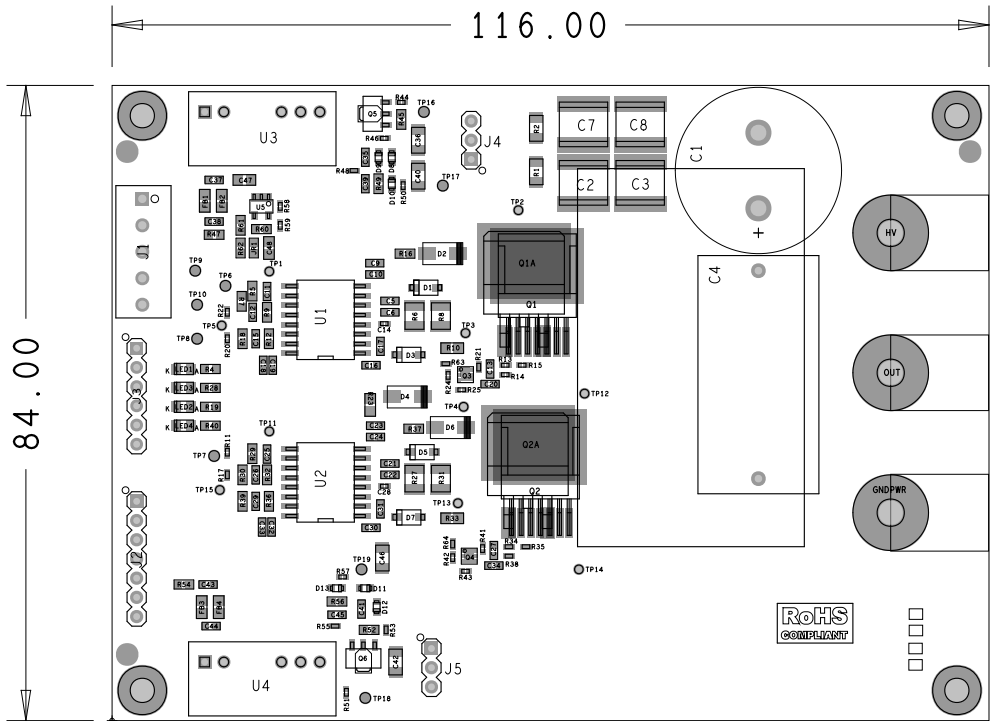
- 1:FABRICATE USING LATEST REVISION OF STM SPECIFICATION.
- 2:FABRICATE USING MASTER ARTWORK EVLSTGAP3S6R2 FOR CIRCUIT PATTERN.
NO DEVIATION FROM MASTER ARTWORK ARE PERMITTED WITHOUT WRITTEN APPROVAL FROM AN AUTHORIZED STM REPRESENTATIVE.
- 3:VENDOR MUST BE UL QUALIFIED AND BOARDS MUST BE IDENTIFIED WITH APPROPRIATE VENDOR UL IDENTIFICATION MARK, LOT OR JOB NUMBER AND PCB MATERIAL FLAMMABILITY RATING (94V-0) MINIMUM.
- 4:MATERIAL - FR4 RoHS COMPLIANT MINIMUM 125 C.
SEE "Cross Section Chart" FOR BOARD THICKNESS, COPPER WEIGHT AND LAYER CONSTRUCTION.
- 5:GREEN SOLDER MASK BOTH SIDE OF BOARD WITH LIQUID PHOTO IMAGEABLE SOLDERMASK.
- 6:FINISH - ELECTROLITYC NICKEL AND GOLD Au:0.7um Ni:4um
- 7:FOR SMT COMPONENTS WITH PIN PITCH OF 0.019 INCH OR MORE NO GANG RELIEF OF SOLDER MASK IS ALLOWED.
- 8:SILKSCREEN TO BE WHITE, NON CONDUCTIVE, EPOXY INK OR EQUIVALENT.
- 9:THIS IS NOT A CONTROLLED IMPEDANCE BOARD.
- 10:DESIGNATED AREA OR INSPECTION AND TEST STAMP.
- 11:ON SMB PCB MUST BE IDENTIFIED MANUFACTURER LOGO AND PCB TYPE (MEANS OF MATERIAL TYPE INDICATED ON THE YELLOW CARD DOCUMENT).
- 12:TEARDROPPING OF VIAS AND PADS ALLOWED AT PAD TO TRACE INTERSECTION TO INSURE A 2 MILS ANULAR RING AT THE JUNCTION.
- 13:REMOVE SILKSCREEN FROM SOLDERABLE SURFACES.
- 14:ALL BOARD TO BE 100% ELECTRICALLY NETLIST TESTED FOR OPENS AND ON SHORTS.APPLY TEST STAMP IN REFERENCED AREA.
- 15:THIS BOARD SHALL BE FULLY COMPLIANT WITH UL796.

DRILL CHART: TOP to BOTTOM			
ALL UNITS ARE IN MILLIMETERS			
FIGURE	SIZE	PLATED	QTY
A	0.25	PLATED	107
B	0.3	PLATED	236
C	0.8	PLATED	10
D	0.9	PLATED	29
E	1.0	PLATED	2
F	1.1	PLATED	5
H	2.1	PLATED	2
I	3.2	PLATED	7



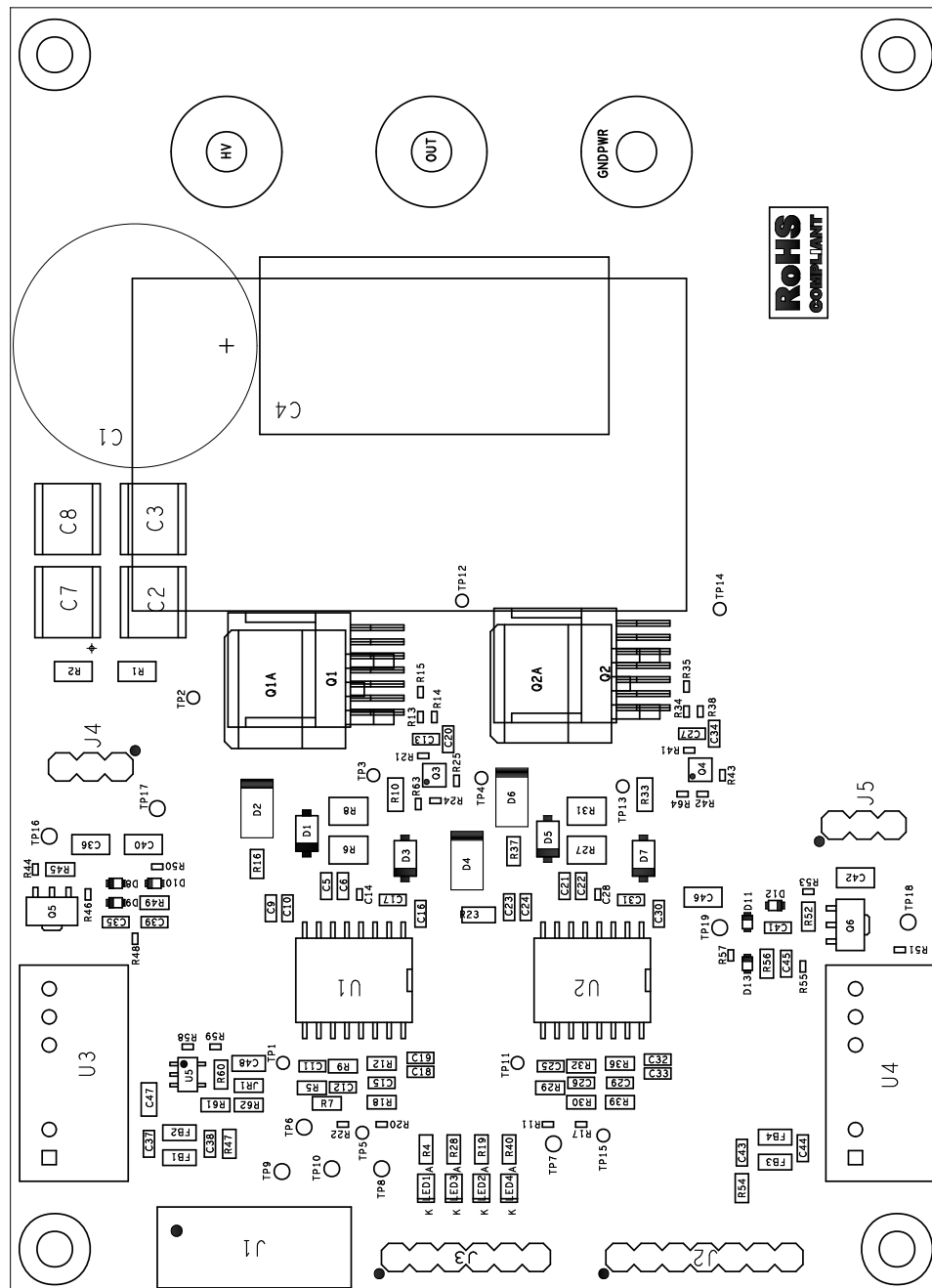
REVISION DATE

		Description DRILLING AND PROFILING					Symbol STGAP3S6	
							Group EVLSTGAP3S6	
ALL RIGHTS STRICTLY RESERVED. REPRODUCTION OR ISSUE TO THIRD PARTIES IN ANY FORM WHATEVER IS NOT PERMITTED WITHOUT WRITTEN AUTHORIZATION FROM STM		TOLERANCE UNLESS NOTED UNIT=MM					ISO	SCALE: 1:1
		linear	0 <10	>10 <50	>50 <200	>200	ANG. LES.	REV. 2.0
		midle	±0.1	±0.2	±0.3	±0.5	±1°	
Drawn D.PANZERI	date 10-01-2025	accurate	±0.05	±0.1	±0.15	±0.25	±30°	
Approved	date	Material Treatment and surface finishing						



CODICE PRODOTTO		EVLSTGAP3S6I			
CLIENTE		STM			
DESCRIZIONE VISTA		ASSEMBLY TOP			
DATA	10-01-2025	REVISIONE	2.0	DISEGNATORE	D.PANZERI
NOTE	NON USARE PER LA COSTRUZIONE DEL PCB				
RISERVATO - CONFIDENZIALE Questo documento e' di proprieta di STM che se ne riserva tutti i diritti Eventuali divulgazioni non autorizzate a terze parti saranno perseguite nei termini di legge.					

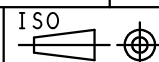
CIPIERRE
ELETTRONICA



REVISION DATE

Description
PIANO DI MONTAGGIOSymbol
STGAP3S6Group
EVLSTGAP3S6

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TOLERANCE UNLESS NOTED
UNIT=MM

SCALE:

REV.
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linear	0 <10	>10 <50	>50 <200	>200	ANG. LES.
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Material

Treatment and surface finishing

Drawn D.PANZERI	date 10-01-2025
Approved	date