12 V battery management system IC VCORE parasitic impact

Introduction

The **STSW-L9988VCORE** tool is a calculation utility developed to help users evaluate the impact of parasitic resistances on the VCORE buck regulator performance.

In a real application, the regulator performance is affected not only by the ideal design values, but also by the resistive parasitic introduced by:

- Internal switches,
- PCB copper paths,
- Ground return paths,
- Output inductor series resistance.

These parasitic contributions can reduce the available load capability and may cause the regulator to operate outside its intended range.

The tool allows the user to enter the relevant application parameters and determine whether a given parasitic resistance combination is acceptable over the required load current range.

The tool is intended to provide a simple and practical way to evaluate whether the selected parasitic resistances degrade the VCORE regulator performance.

More specifically, the tool helps the user to:

- Estimate the influence of parasitic resistance on regulator operation,
- Identify the maximum load current that can be supported without performance degradation,
- Compare the behavior across multiple VCORE output voltages,
- Export the calculated results for documentation or design review.

The tool does **not** replace detailed hardware validation, but it is a useful aid during:

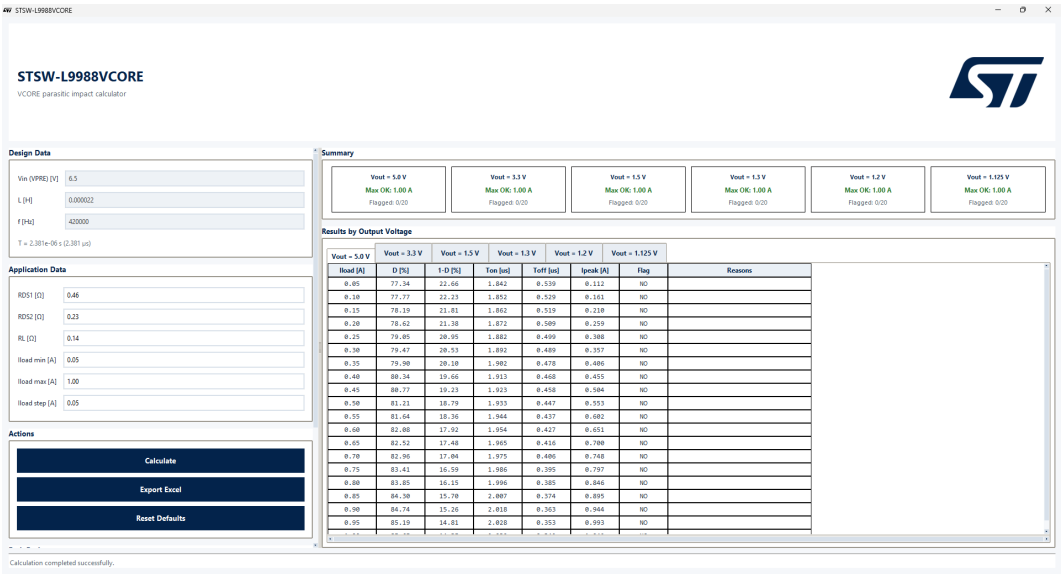
- Schematic definition,
- PCB layout review,
- Inductor selection,
- Sensitivity analysis on path resistances.

The **STSW-L9988VCORE** tool is available online on www.st.com.

1 L9988 - VCORE parasitic impact tool

The Figure 1 shows the **STSW-L9988VCORE tool** user interface designed to analyze the parasitic resistance impact on the VCORE regulator performance.

Figure 1. L9988 - VCORE parasitic impact tool user interface



The GUI is organized into the following sections:

- **Design data**
- **Application data**
- **Actions**
- **Summary**
- **Results by output voltage**
- **Path resistances**

Each section has a specific purpose, described below.

1.1 Design data section

The **design data** section contains the fixed regulator design parameters used by the tool. These values are predefined and are not intended to be modified by the user. The section includes:

- **Vin (VPRE) [V]:** input voltage of the VCORE buck regulator (that corresponds to **VPRE**).
- **L [H]:** buck inductance.
- **f [Hz]:** switching frequency of the regulator.

The tool also shows the computed switching period:

- **T = 1/f**: this period is displayed for user reference and is used in the internal checks for Ton and Toff.

This section defines the fixed operating environment of the regulator. All subsequent calculations depend on these values.

1.2 Application data section

The **application data** section contains the parameters that the user can change to model the actual application. The user can enter:

RDS1 [Ω]: This is the total resistance between **VIN** and the **software node**. It includes both:

- External PCB contribution,
- Internal HS switch ON resistance.

RDS2 [Ω]: this is the total resistance between the **software node** and **GND**. It includes both:

- External PCB ground return contribution,
- Internal LS switch ON resistance.

RL [Ω]: this is total resistance between **software node** and **VOUT**. It includes both:

- External PCB contribution,
- ESR of Buck inductance.

Iload min [A]: minimum load current considered in the analysis.

Iload max [A]: maximum load current considered in the analysis.

Iload step [A]: step used to sweep the load current between minimum and maximum values.

This section defines the actual operating conditions that are under the user's control.

By changing these values, the user can emulate different PCB implementations and component selections.

1.3 Action section

The **actions** area contains the main tool commands.

Calculate:

Runs the complete analysis using the values currently entered in the GUI. When the user presses **calculate**, the tool computes for every configured output voltage and every selected load current:

- Duty cycle,
- Complementary duty cycle,
- Ton,
- Toff,
- Inductor peak current,
- Pass/fail conditions.

Export excel:

Exports all calculated results to an excel file. The generated report includes:

- Design data,
- Application data,
- One worksheet for each output voltage.

This is useful for:

- Design reviews,
- Traceability,
- Comparison across different scenarios.

Reset defaults

Restores the default values of the application data and recalculates the results. This allows the user to quickly return to the reference configuration.

1.4 Summary section

The **summary** section gives a compact overview of the results for each supported output voltage. The tool evaluates the following VCORE output voltages:

- $5.0\,\mathrm{V}$
- $3.3\,\mathrm{V}$
- $1.5\,\mathrm{V}$
- $1.3\,\mathrm{V}$
- $1.2\,\mathrm{V}$
- $1.125\,\mathrm{V}$

For each output voltage, the summary displays:

- **Max OK**: the highest load current for which no warning or limit violation is detected.
- **Flagged**: number of load current points that violate at least one condition.

This section helps the user quickly identify:

- which output voltages are more critical,
- how much usable load current is available,
- whether the chosen parasitic resistance combination is acceptable.

1.5 Results by output voltage section

This is the main analysis area of the GUI. Each output voltage has a dedicated tab, and each tab contains a table of computed results versus load current. The table shows:

Iload [A]: load current under evaluation.

D [%]: buck duty cycle.

1-D [%]: complementary duty cycle.

Ton [us]: switch ON time.

Toff [us]: switch OFF time.

Ipeak [A]: estimated inductor peak current.

Flag: indicates whether at least one limit condition is violated.

NO: operating point considered acceptable

YES: at least one condition is violated

Reasons: detailed explanation of the violated condition(s), such as:

- D > 1
- 1-D < 0
- Ton > 1/f
- Toff < 0.24 us
- Ipeak > 1.25 A

The GUI applies visual highlighting to values that violate the limits. When a specific parameter exceeds its allowed range, its corresponding table cell is highlighted in red. This makes it easier to identify the first failing operating point.

For a given output voltage, the **maximum allowed load current** is the highest current for which:

- No red-highlighted parameter appears,
- The **flag** field remains NO.

1.6 Path resistances section

The **path resistances** section is an explanatory area of the GUI. It contains:

- a textual description of the parasitic resistance paths,
- a schematic image of the buck regulator structure.

This section is scrollable and is intended to guide the user in understanding how the resistance parameters map to the circuit. It helps relate the abstract numerical inputs of the tool to the real hardware implementation.

2 Input parameters

The tool validates the user entries before starting the calculation. The current implementation includes checks such as:

- Minimum load current must be at least $0.01\ \mathrm{A}$,
- Current step must be positive,
- Maximum current must be greater than or equal to the minimum current,
- RDS1 must not be below the internal HS switch minimum resistance,
- RDS2 must not be below the internal LS switch minimum resistance.

More specifically:

$RDS1 \geq 0.260\ \Omega$

$RDS2 \geq 0.145\ \Omega$

No fixed minimum limit is enforced by the tool on RL, because that value depends on the external inductor selected by the user.

3 Calculation outputs

For each output voltage and load current point, the tool computes the operating quantities of the buck regulator. The main computed expressions are:

- **Duty cycle:**

$$D = \frac{V_{OUT} + I_{LOAD}(RDS2 + RL)}{V_{IN} - I_{LOAD}(RDS1 - RDS2)}$$

- **Complementary duty cycle:**

$$1 - D$$

- **ON time:**

$$T_{ON} = T \cdot D$$

- **OFF time:**

$$T_{OFF} = T \cdot (1 - D)$$

Where:

$$T = \frac{1}{f}$$

- **Peak current:**

The peak inductor current is derived from the average load current and the inductor current ripple generated during the ON time of the buck converter. During the ON phase, the voltage across the inductor is:

$$V_L = V_{IN} - I_{LOAD}(R_{DS1} + R_L) - V_{OUT}$$

Where:

- V_{IN} is the buck input voltage,
- R_{DS1} is the total resistance between VIN and software,
- R_L is the total resistance between software and VOUT,
- V_{OUT} is the regulated output voltage.

From the inductor voltage-current relationship:

$$\frac{dI}{dt} = \frac{V_L}{L}$$

The current inductor increase during the ON time is:

$$\Delta I = \frac{V_L}{L} \cdot T_{ON}$$

Assuming a triangular ripple current centered around the average load current, the peak inductor current is:

$$I_{PEAK} = I_{LOAD} + \frac{\Delta I}{2}$$

Therefore, substituting ΔI:

$$I_{PEAK} = I_{LOAD} + \frac{1}{2}\left(\frac{V_L}{L} \cdot T_{ON}\right)$$

and finally:

$$I_{PEAK} = I_{LOAD} + \frac{1}{2}\left(\frac{V_{IN} - I_{LOAD}(R_{DS1} + R_L) - V_{OUT}}{L} \cdot T_{ON}\right)$$

This value is used by the GUI to verify whether the operating point exceeds the allowed peak current limit.

If the computed peak current is higher than the imposed threshold, the corresponding result is flagged and highlighted in red.

4 Result interpretation

The tool checks whether the computed operating point is still acceptable. An operating point is considered **flagged** if at least one of the following conditions occurs:

- **Duty cycle is greater than unity:**

$D > 1$

- **Negative complementary duty cycle:**

$1 - D < 0$

- **ON time greater than the switching period:**

$T_{ON} > T$

- **OFF time below minimum allowed limit:**

$T_{OFF} < 0.24\,\mu s$

- **Peak current above the allowed threshold:**

$I_{PEAK} > 1.25\,\mathrm{A}$

If one or more of these conditions is true, the tool flags the operating point and marks the corresponding cell(s) in red.

A red flag indicates that the selected parasitic resistance combination may degrade regulator performance at that current level. Therefore, the user should consider:

- Reducing PCB path resistance,
- Selecting an inductor with lower DCR,
- Reducing the required load current,
- Reviewing the output voltage operating point.

5 Path resistances

As shown in **Figure 2**, parasitic resistance contributions are subdivided into 3 segments:

RDS1 is total resistance between VIN and software node:

$R_{DS1} = R_{PCB_HS} + R_{HS_SW}$

Where:

- R_{PCB_HS} is the total path resistance from VPRE output capacitance to VPRE_CORE pin (external to device)
- R_{HS_SW} is VCORE HS switch total ON resistance (internal to device).

The internal HS switch resistance R_{HS_SW}has:

- Minimum value: $260\ \mathrm{m\Omega}$
- Maximum value: $879\ \mathrm{m\Omega}$

Therefore:

$RDS1_{min} \geq 260\ \mathrm{m\Omega}$

RDS2 is the total resistance between software node and GND:

$R_{DS2} = R_{PCB_LS} + R_{LS_SW}$

Where:

- R_{PCB_LS} is the total path resistance from VCORE_GND to GND plane (external to device)
- R_{LS_SW} is VCORE LS switch total ON resistance (internal to device).

The internal LS switch resistance has:

- Minimum value: $145\ \mathrm{m\Omega}$
- Maximum value: $385\ \mathrm{m\Omega}$

Therefore:

$RDS2_{min} \geq 145\ \mathrm{m\Omega}$

RL is the total resistance between software node and VOUT:

$R_L = R_{PCB_L} + R_{L_DCR}$

Where:

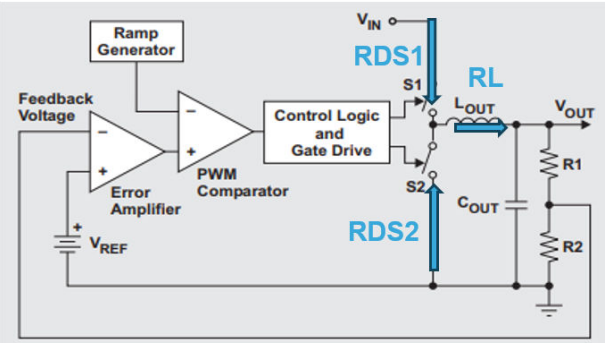
- R_{PCB_L} is the total path resistance from VCORE_SW to VCORE output capacitance (external to device)
- R_{L_DCR} is inductor series resistance (external to device)

The parameter R_{L_DCR} is external and depends on:

- Selected inductor,
- Component technology,
- Current rating,
- Inductor DCR specification from the datasheet.

It is user-defined and is not forced to a fixed minimum by the GUI, because it depends on the specific component selected for the application. The internal contribution to be considered has been indicated within the tool and the external contribution depends on the application board implementation and shall be computed.

Figure 2. Path resistance

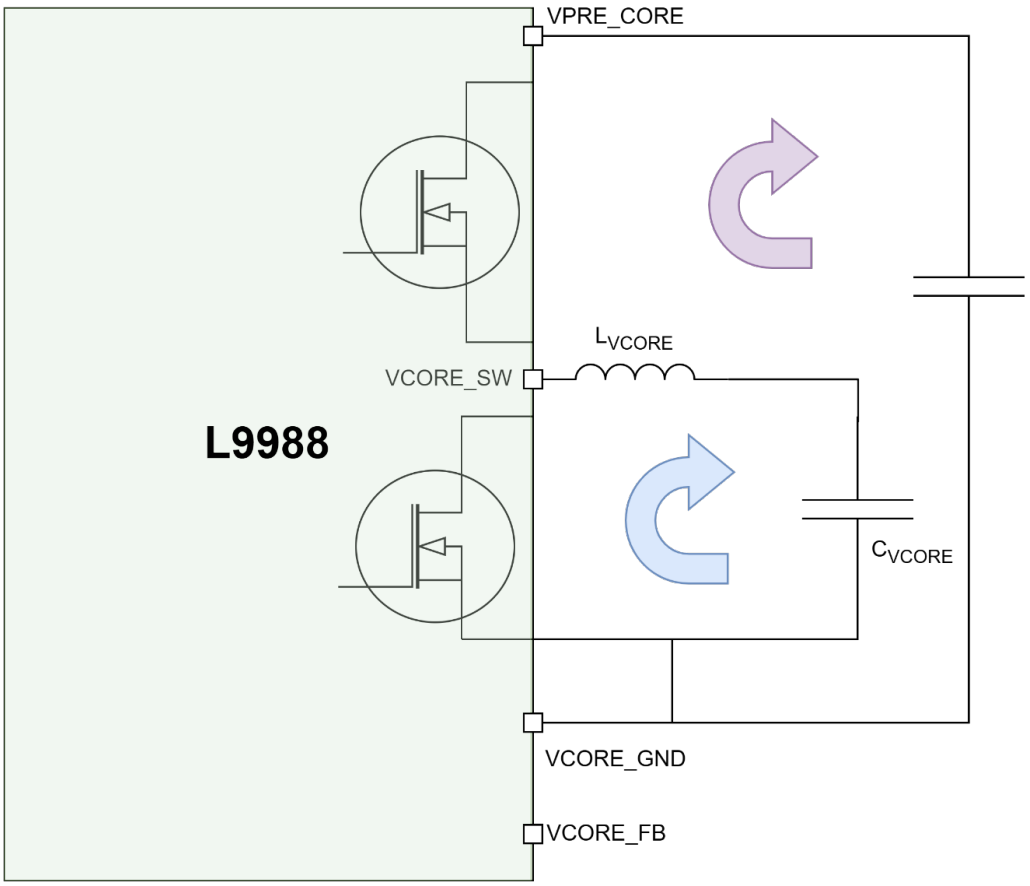


6 PCB layout recommendations

The PCB layout has a strong impact on parasitic resistance and switching behavior. The application note recommends keeping the critical current loops as small as possible.

The **Figure 3** shows a layout guideline for a buck converter, highlighting the switching node and the need to keep noisy switching traces well separated from sensitive sense/feedback nets.

Figure 3. Figure buck layout suggestions



- **High di/dt switching loop** (blue loop around BUCKSW and VCORE_GND):

the loop including the switching node and ground return should be minimized to reduce parasitic inductance and noise.

- **Input power loop** (violet loop around VPRE_CORE and VCORE_GND):

the loop around the input decoupling path should also be kept compact.

- **Feedback and sense routing**

Sensitive sense and feedback traces should be routed away from noisy switching nets such as the software node. This helps prevent:

- Noise coupling,
- Regulation errors,
- Unstable behavior.

Good layout practice directly helps reduce the parasitic terms modeled by:

- RDS1
- RDS2

and indirectly improves overall regulator robustness.

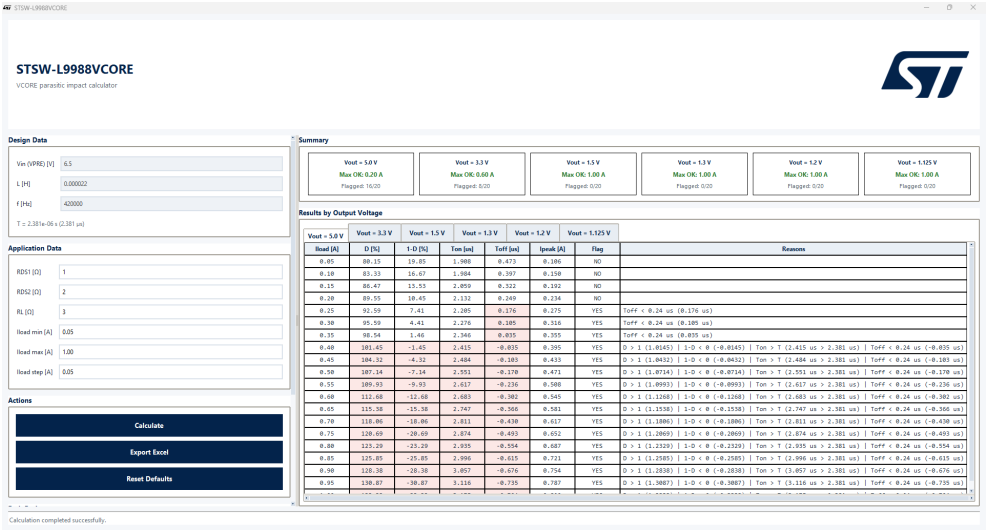
7 Example

Consider the following parasitic resistance scenario:

- $RDS1 = 1\ \Omega$
- $RDS2 = 2\ \Omega$
- $RL = 3\ \Omega$

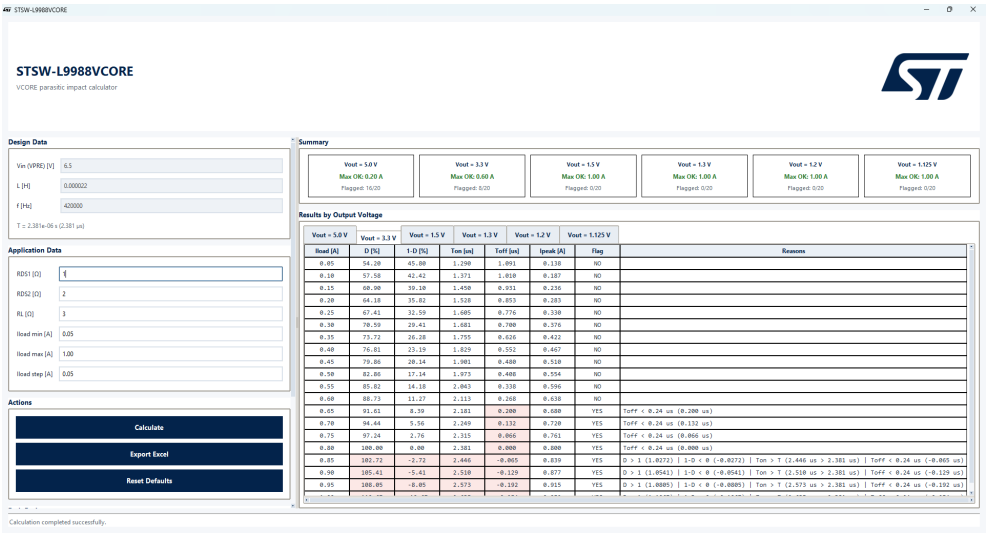
@ 5 V output, the maximum allowed current is approximately 200 mA. Red flags begin to appear at approximately 250 mA.

Figure 4. STSW-L9988VCORE @ 5 V output



@ 3.3 V output, the maximum allowed current is approximately 600 mA. Red flags begin to appear at approximately 650 mA.

Figure 5. STSW-L9988VCORE @ 3.3 V



@ 1.5 V, 1.3 V, 1.2 V and 1.125 V outputs, no red flags appear up to 1 A

This demonstrates that the same parasitic resistance set can have a different impact depending on the selected output voltage.

Revision history

Table 1. **Document revision history**

Date	Version	Changes
15-Oct-2026	1	Initial release.

Contents

1 L9988 - VCORE parasitic impact tool 2
1.1 Design data section 2
1.2 Application data section 2
1.3 Action section 3
1.4 Summary section 3
1.5 Results by output voltage section 4
1.6 Path resistances section 4
2 Input parameters 5
3 Calculation outputs 6
4 Result interpretation 7
5 Path resistances 8
6 PCB layout recommendations 9
7 Example 10
Revision history 11
List of tables 13
List of figures 14

List of tables

Table 1. Document revision history 11

List of figures

Figure 1. L9988 - VCORE parasitic impact tool user interface. 2
Figure 2. Path resistance. 8
Figure 3. Figure buck layout suggestions. 9
Figure 4. STSW-L9988VCORE @ 5 V output. 10
Figure 5. STSW-L9988VCORE @ 3.3 V 10

IMPORTANT NOTICE – READ CAREFULLY

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice.

In the event of any conflict between the provisions of this document and the provisions of any contractual arrangement in force between the purchasers and ST, the provisions of such contractual arrangement shall prevail.

The purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgment.

The purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of the purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

If the purchasers identify an ST product that meets their functional and performance requirements but that is not designated for the purchasers' market segment, the purchasers shall contact ST for more information.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, refer to www.st.com/trademarks. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2026 STMicroelectronics – All rights reserved