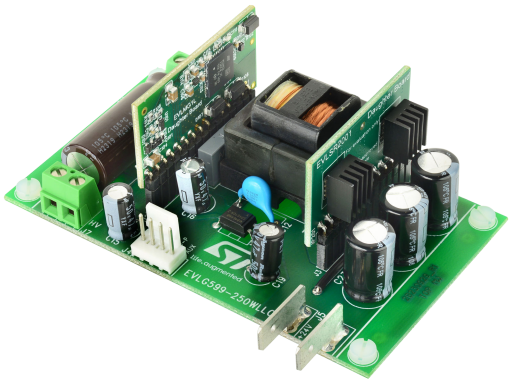
DC/DC resonant converter for industrial applications using STNRG599A, MASTERGAN1L and SRK2001A

Introduction

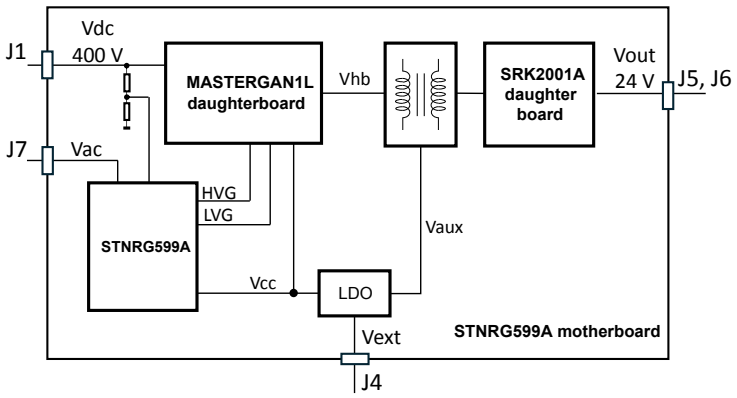
The EVLG599-250WLLC demonstration board is a resonant LLC converter dedicated to any kind of industrial application where minimum size and high efficiency are required (industrial DC-DC applications, adapters, consumer SMPS). It can be used as a DC-DC converter with an output power up to 250 W and a nominal output voltage of 24 V, from an input voltage of 400 V provided by a PFC. The converter consists of a motherboard with the LLC resonant tank and the STNRG599A, and two daughterboards: one, on the primary side, with the MASTERGAN1L, and another one, on the secondary side, with the SRK2001A and the synchronous rectification MOSFETs. The converter is based on STNRG599A, a novel phase shift resonant controller, and on the MASTERGAN1L, embedding a GaN transistor-based half-bridge leg and corresponding drivers in the same package. This allows direct interfacing with any kind of SMPS controller. Thanks to the GaN technology and embedded drivers, the converter has been designed with a higher operating frequency than using conventional MOSFETs, with a reduction in dimensions of the resonant transformer and an increase in compactness of the board. The STNRG599A integrated HV startup allows the IC to be powered from AC mains for proper power-up, with no need for auxiliary standby supplies. It can also provide current to another control IC such as, for example, the PFC control IC. The board has no heat sink on the primary side and has very reduced dimensions. The high efficiency and small size (the power density is 41 W/inch^3) make the board very suitable when available space is limited. It comes with overcurrent and short-circuit protections and an integrated input voltage monitor, allowing LLC converter startup with correct sequencing, preventing operation with too low input voltage. Furthermore, the LINE pin is internally clamped to 3.4 V, typ, to manage feedback failure disconnection of the low-side resistor of the external divider on the input voltage. Note that STNRG599A is the IC version with X-capacitor discharge enabled at the HV pin, while STNRG599B is the IC version with X-capacitor discharge disabled at the HV pin, suitable for lighting applications. The following Figure 1 shows the evaluation board. On the left, the AC input to the HV pin of the STNRG599 is in the visible bottom corner, while the DC input to the half-bridge leg of MASTERGAN1L is in the hidden top corner. The daughterboard on the left is the MASTERGAN1L one, while the daughterboard on the right is the SRK2001A one. In the former, the MASTERGAN1L is well visible, while in the latter the SR MOSFET pair with heat sinks is visible. The STNRG599A is not visible since it is mounted on the bottom of the motherboard. The output connector is in the right bottom corner. The picture of the board is in the following Figure 1.

Figure 1. EVLG599-250WLLC evaluation board



The following Figure 2 shows the block diagram of the board.

Figure 2. EVLG599-250WLLC functional block diagram



The following Table 1 describes the connectivity of the board.

Table 1. EVLG599-250WLLC connectors

Reference	Type	Description
J1	Screw connector terminal	DC input voltage (400 V ±10%, ≥ 250 W)
J2	Female strip connector 15 pins	To insert the EVLMG1L daughterboard
J3	Female strip connector 13 pins	To insert the EVLSR2001 daughterboard
J4	Vertical connector header vertical	Ext. VCC, GND, N.C., Ext. LINE
J5	Male "faston" connector	Output voltage, positive terminal
J6	Male "faston" connector	Output voltage, negative terminal
J7	Screw connector terminal	AC input voltage (for HV startup)

The following Table 2 summarizes the main characteristics and performances.

Table 2. EVLG599-250WLLC characteristics

Parameter	Value
DC input voltage	400 V ±10%
DC output voltage	24 V
Output current	Up to 10.4 A
Output power	Up to 250 W
Efficiency	> 96% at full load (and above half load)
Open load consumption	≤ 210 mW
Operating frequency	260 ±10 kHz (400 Vdc, 10.4 A)
Board size	W x H: 80 x 55 mm x mm. Max. height: 23 mm
Power density	41 W/inch^3

1 Evaluation board schematic

Figure 3. **EVLG599-250WLLC motherboard schematic**

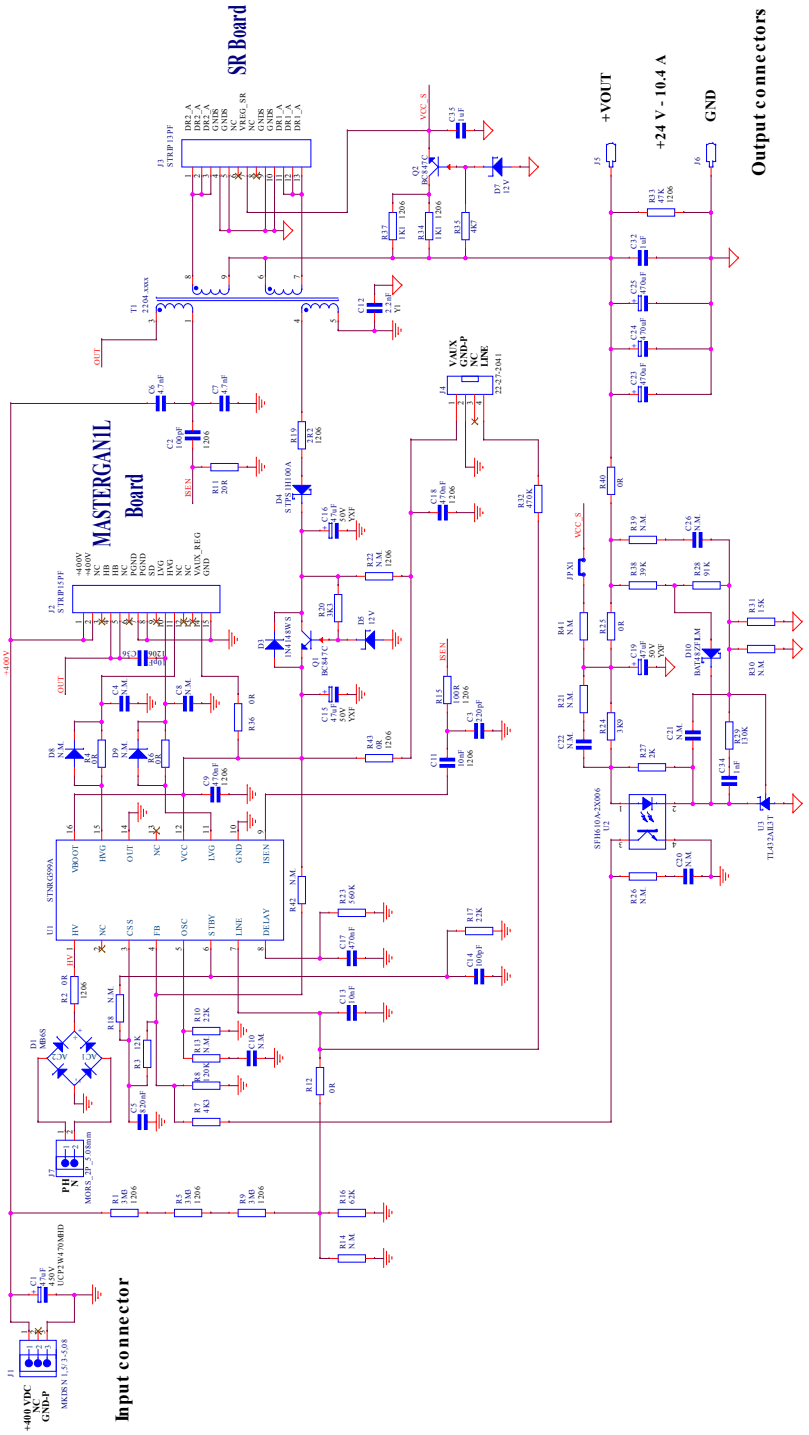


Figure 4. **EVLG599-250WLLC MasterGaN1L daughterboard schematic**

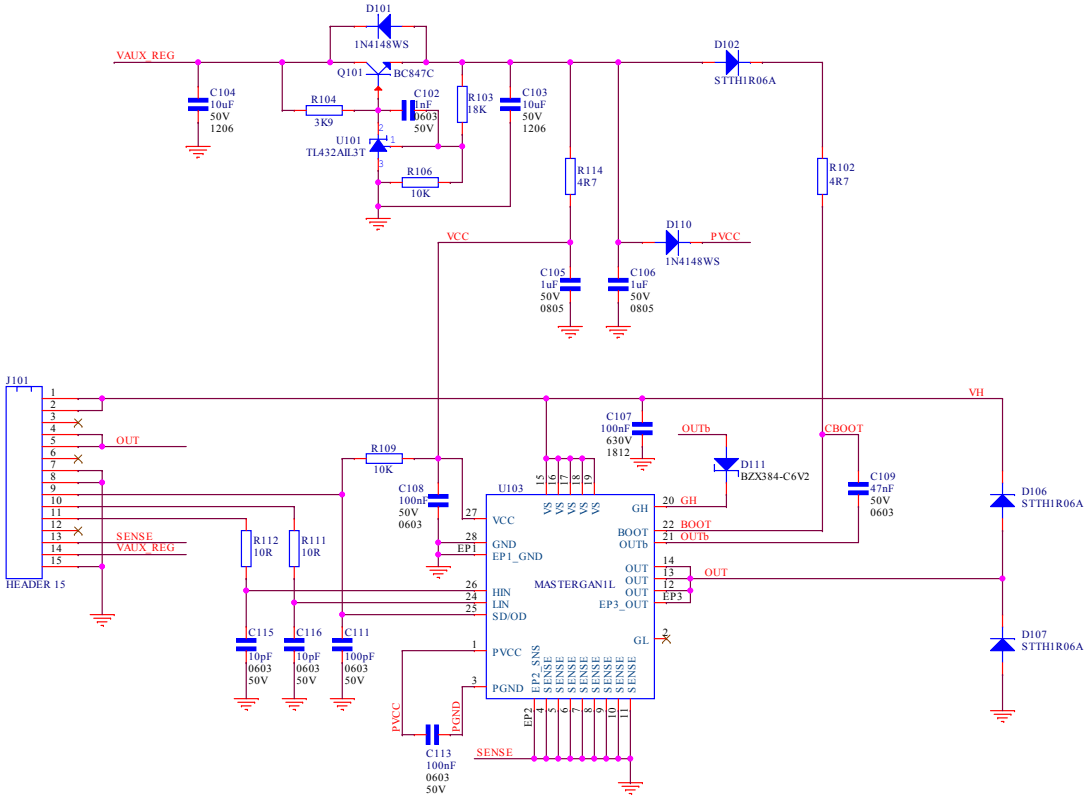
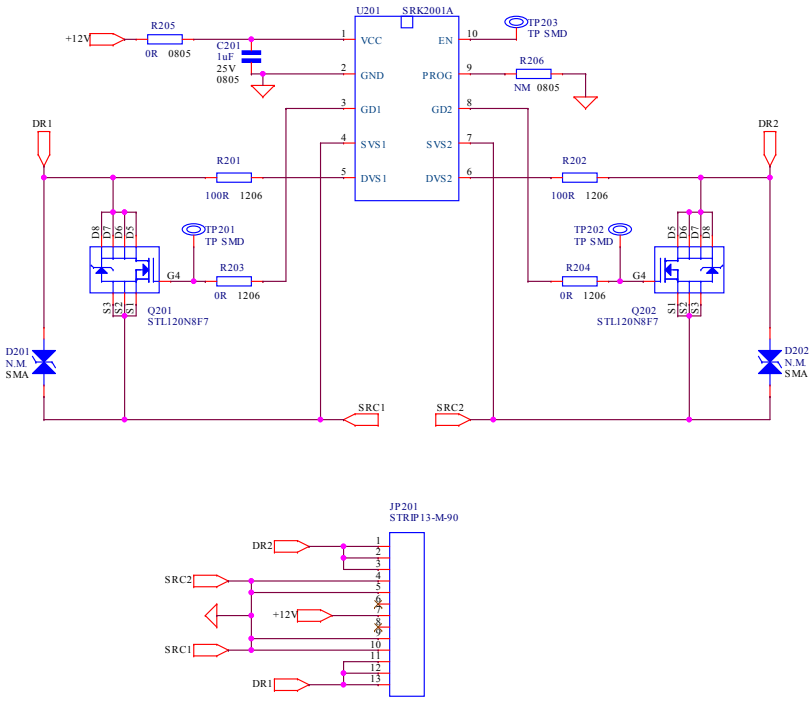


Figure 5. **EVLG599-250WLLC MasterGaN1L daughterboard schematic**



2 Evaluation board layout

In the following figures, the layout of the motherboard and of the two daughterboards are shown. Top and bottom are both observed from the top.

Figure 6. **EVLG599-250WLLC motherboard layout – top side**

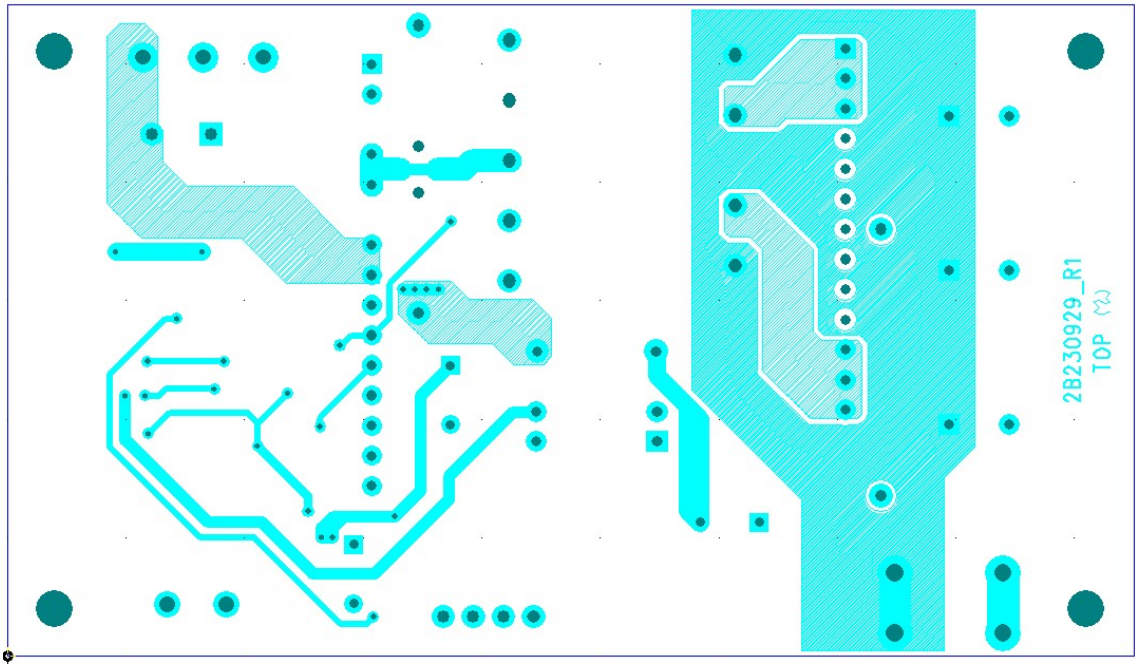


Figure 7. **EVLG599-250WLLC motherboard layout – bottom side**

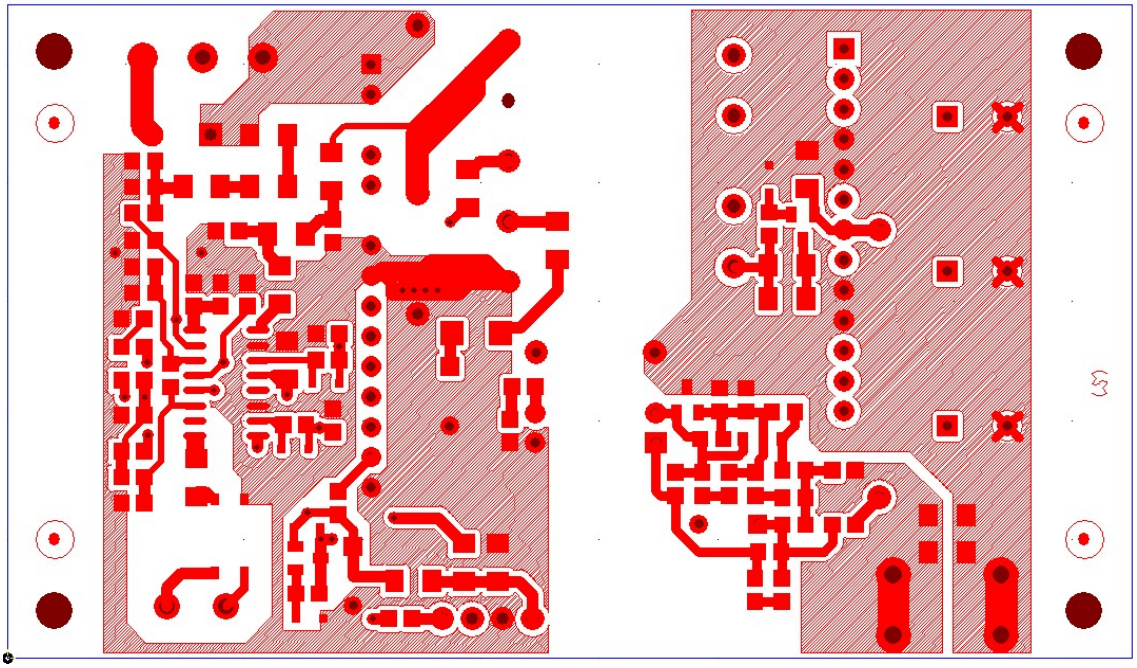


Figure 8. **MASTERGAN1L daughterboard layout – top side**

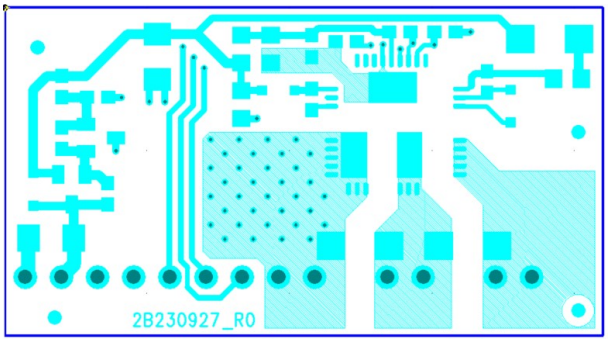


Figure 9. **MASTERGAN1L daughterboard layout – bottom side**

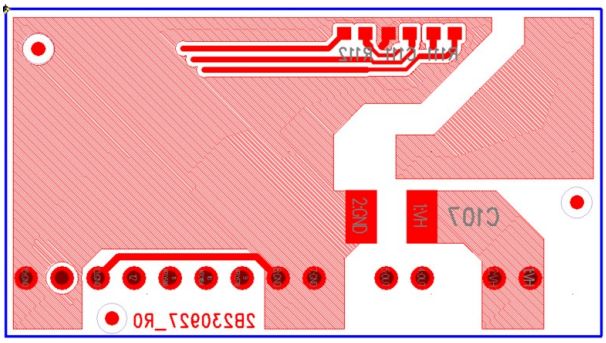


Figure 10. **SRK2001A daughterboard layout – top side**

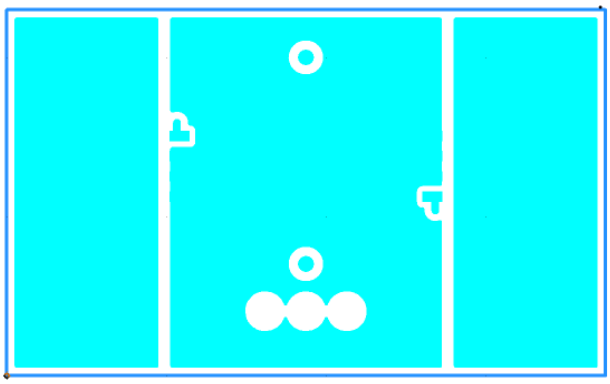
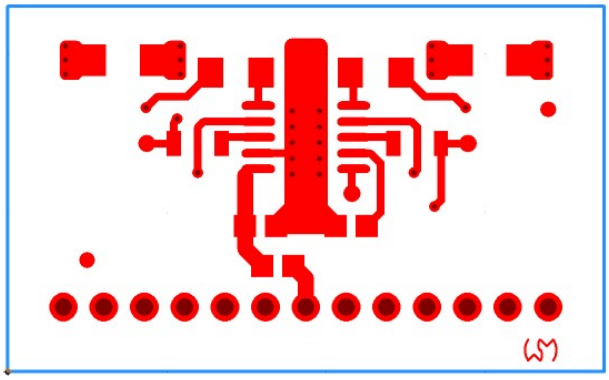


Figure 11. **SRK2001A daughterboard layout – bottom side**



3 Evaluation board assy/silk

In the following figures, the assy and the silk of the motherboard and of the two daughterboards are shown. Top side is observed from the top, while bottom side is observed from the bottom.

Figure 12. EVLG599-250WLLC motherboard assy/silk – top side

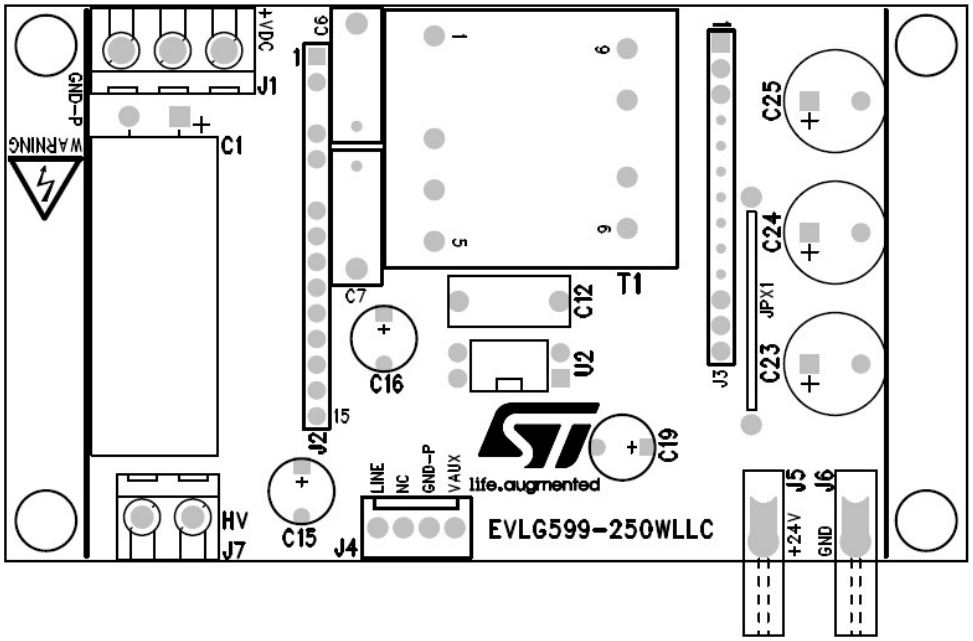


Figure 13. EVLG599-250WLLC motherboard assy/silk – bottom side

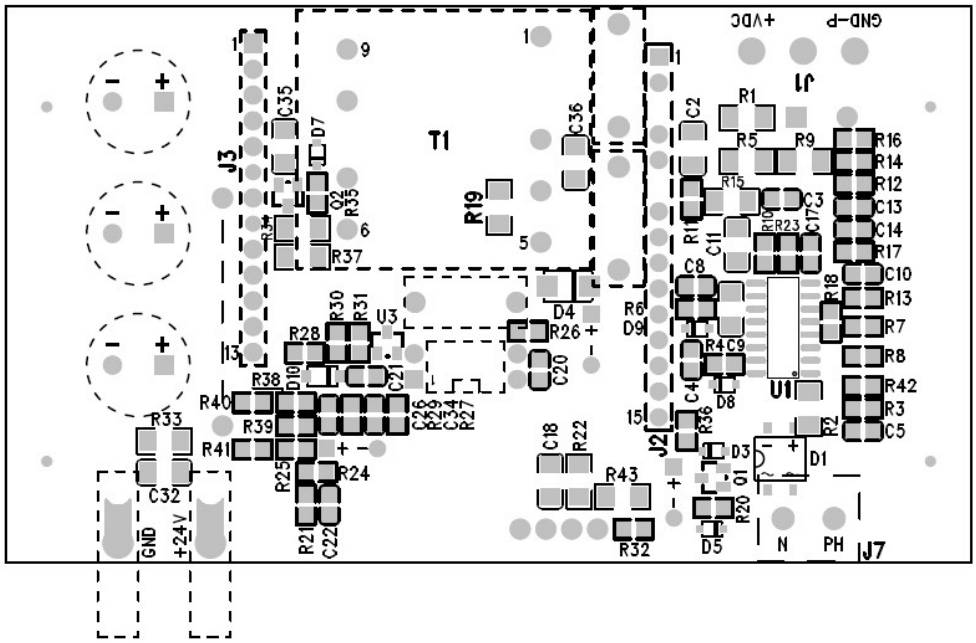


Figure 14. **MASTERGAN1L daughterboard assy/silk top side**

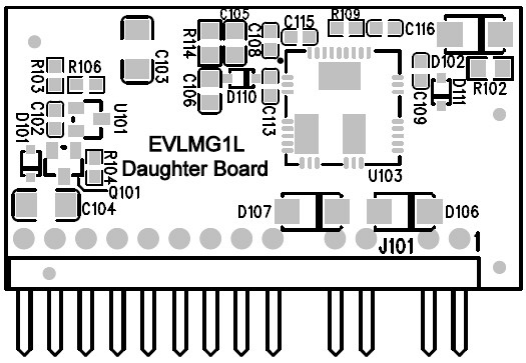


Figure 15. **MASTERGAN1L daughterboard assy/silk bottom side**

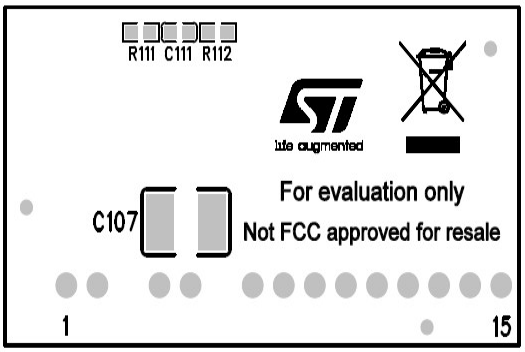


Figure 16. **SRK2001A daughterboard assy/silk top side**

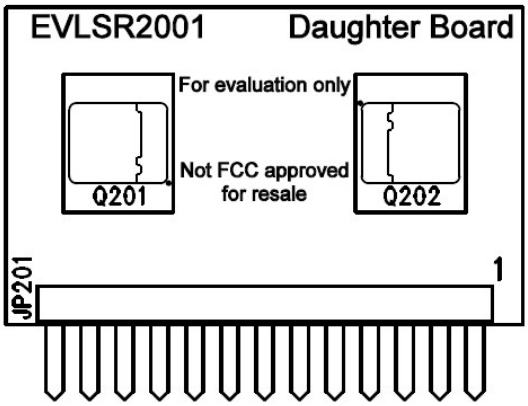
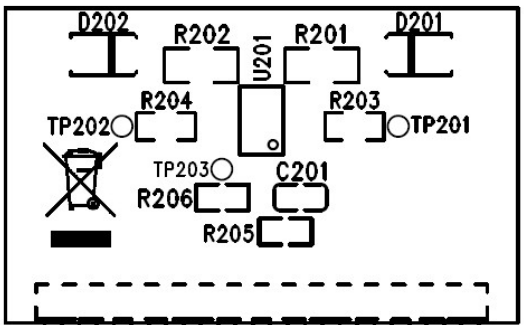


Figure 17. **SRK2001A daughterboard assy/silk bottom side**



4 Evaluation board description

The evaluation board EVLG599-250WLLC consists of one motherboard (with the STRNG599A and the LLC tank) and two daughterboards (one for the MASTERGAN1L and one for the SRK2001A) that are plugged on it.

At J1, a high-voltage DC source (> 250 W capable) must be connected, with correct polarity, to supply the half-bridge leg integrated in the MASTERGAN1L. The turn-on input voltage of the converter, which is the DC brown-in, is about 385 V and the turn-off input voltage of the converter, which is the DC brown-out, is about 280 V. The maximum voltage at J1 is 440 V.

The converter can be turned on in two ways: 1) by connecting a low-voltage DC source to J4 (between pins 1 and 2, which are VAUX and GNDP, respectively) to bring the VCC pin of the STNRG599 above V_{VCCON} = 16.5 V, typ (but below the AMR of the pin), 2) by connecting an AC source, programmed at low mains or high mains, to J7 to use the high-voltage startup integrated in the STNRG599A. In both cases, once the converter operation starts, the power supply of the STRNG599A and of the MASTERGAN1L is guaranteed by the auxiliary winding of the transformer that is regulated, on the motherboard, at about 11.5 V, by a simple LDO based on a 12 V Zener diode and an NPN transistor. This means that, in case 1), the external low-voltage DC source can be turned off after the converter operation has started. In case 2), the high-voltage startup integrated in the STNRG599A is automatically turned off after about 80 ms from $V_{VCC} = V_{VCCON}$. The power supply of the MASTERGAN1L is derived from the regulated 11.5 V, by another LDO, based on the TL432 and an NPN transistor, implemented on its daughterboard. On the secondary side, to limit the power dissipation by the SRK2001A, its power supply is derived by the output voltage, 24 V typ, through a third LDO that is like the one on the primary side (12 V Zener diode and NPN transistor). Note that pin 4 of J4 allows the voltage of the LINE pin of the STNRG599A to be set.

The converter is based on an LLC resonant tank operating at about 260 kHz at Vin = 400 V and Iout = 10.4 A. The output voltage regulation at full load is maintained over a wide input voltage range from 290 V to 440 V.

The LLC resonant tank is driven by the MASTERGAN1L, an advanced system-in-package power device integrating a GaN transistor-based half-bridge leg, and corresponding drivers.

The half-bridge leg embedded in the MASTERGAN1L is driven by the STNRG599A, which is a double-ended controller specific for series-resonant topologies, supporting both LLC and LCC configurations. It provides two complementary outputs (HVG and LVG) 180º out-of-phase with 50% duty cycle and a dead-time, inserted between the turn-off of either switch and the turn-on of the other, automatically adjusted to fit the transition times of the half-bridge midpoint to ensure zero voltage switching over the whole operating range. The complementary outputs usually drive the high-side MOSFET and the low-side MOSFET of the half-bridge leg, the OUT pin being connected to the half-bridge node. However, in this case, to drive the MASTERGAN1L, the complementary outputs must both be referred to ground, so the OUT pin is connected to GND. Proper operation of the adaptive dead time function requires a 10 pF high-voltage capacitor between the half-bridge node and the LVG pin. It is C36 on the motherboard.

The output voltage regulation is obtained by directly controlling the phase shift between the half-bridge voltage and the resonant tank current. This novel proprietary control method called Phase Shift Control (PSC) method is characterized by a good relationship between the controlled variable (i.e. the phase shift) and the power transferred by the converter. This aspect of the novel method results in advantageous properties, including good input voltage ripple rejection and low sensitivity to the tolerance of the components.

The STNRG599A is equipped with a full set of protection features such as hard-switch prevention or anti-capacitive protection, 1st and 2nd level overcurrent protection, the delayed shutdown and restart function based on pin DELAY.

At light load, the STNRG599A enters a controlled burst mode operation that makes the converter work intermittently. This helps to reduce the average switching frequency and minimize the open-load input power of the converter. To further reduce the average switching frequency, the STNRG599A is equipped with an enhanced burst mode function: in the final part of the switching activity of the single burst packet, before it is stopped by the burst mode comparator, the controller forces a phase shift reduction to increase the energy transferred by each switching cycle. This results in an extension of the idle time between two consecutive burst packets and in a reduction of the input power.

The PSC method allows burst mode entry level to be set in terms of the phase (between the input voltage and the input current of the resonant tank) at which the burst mode operation must start. The phase is proportional to the transferred power, so the burst mode entry level is well linked to the output load.

The STNRG599A checks the input voltage Vin, to supply the resonant transformer, to perform the brown-in\out function by the LINE pin with the voltage divider consisting of resistors R1, R5, R9 and R16. The LINE pin also implements the OVP protection. In fact, if the pin is pulled to 3.1 V (typ, 200 mV hysteresis), the turn-off procedure based on the DELAY pin is activated: the switching activity is immediately stopped, the soft-start capacitor (CSS) is completely discharged and the internal 250 µA current source is kept on till VDELAY = 1.75 V. As the voltage on the pin exceeds 1.75 V, the internal 250 µA current source is turned off, the voltage on the pin decays because of RDELAY and, also in this case, the IC is restarted, following the complete soft-start process, when VDELAY falls below 0.2 V.

To achieve high efficiency, synchronous rectification is implemented on the secondary side by SRK2001A driving the MOSFETs Q201 and Q202. This function is performed on the daughterboard located on the secondary side.

Additional protections are OCP1 and OCP2, managed by the ISEN and DELAY pins, to avoid excessive current levels in the resonant tank converter.

5 Efficiency at heavy and light loads

The following figures show the efficiency of the converter at heavy loads and light loads. The board was supplied by a DC high-voltage source of 400 V (Vin). The input power and voltage were measured by a power meter, the output voltage by a multimeter and the output current by the active load. The output power and the efficiency were calculated from measured data.

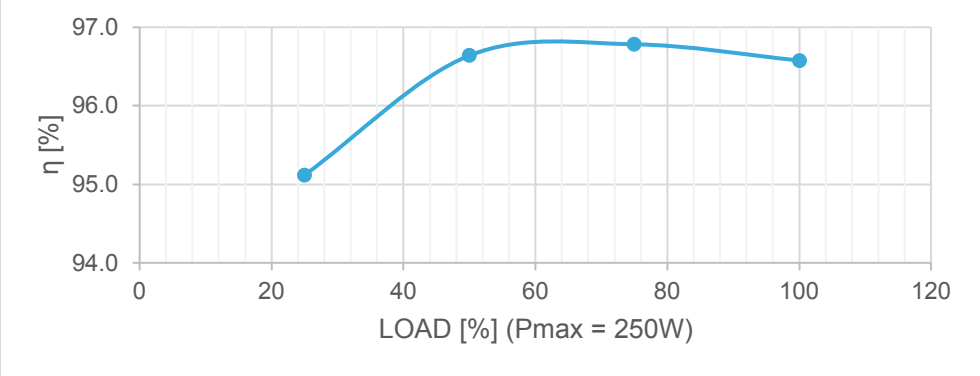
At heavy loads, the board was loaded by an active load set in CC mode. During the measurements, the board was cooled by a fan placed parallel to the long edge of the board, near the input voltage connector, at 1 cm. The measured air flow rate is 2 m/s and the air temperature was 26.5°C. Ten minutes warm-up time was kept between each measurement point, starting from the lowest load.

Figure 18 graphically shows the data collected in the Table 3: the efficiency measured from 25% to 100% load, at nominal input voltage, is reported. It is greater than 95% above 25% and greater than 96.5% above 50%.

Table 3. EVLG599-250WLLC efficiency @ heavy loads

Load [%]	Pin [W]	Vout [V]	Iout [A]	Pout [W]	η [%]
25	65.66	24.0769	2.594	62.46	95.1
50	129.32	24.0673	5.193	124.98	96.6
75	193.69	24.055	7.793	187.46	96.8
100	258.91	24.041	10.401	250.05	96.6

Figure 18. EVLG599-250WLLC efficiency @ heavy loads

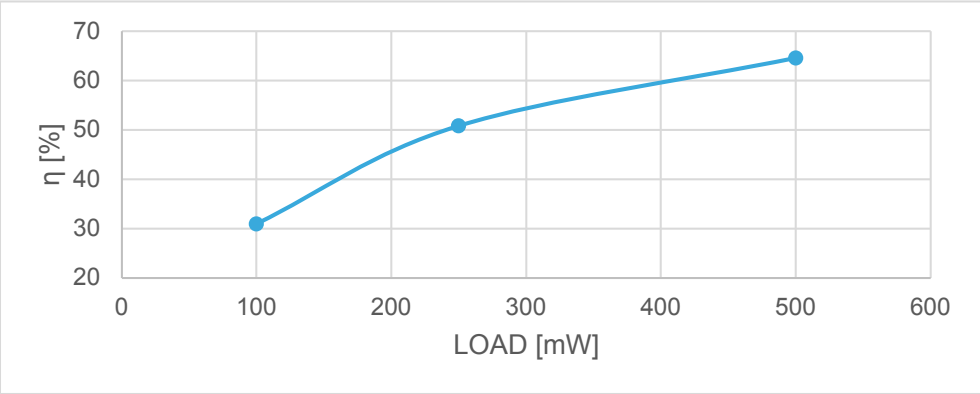


At light loads, the board was loaded by resistors to overcome the limited resolution of the active load. The input power was measured as input energy averaged in time over 36 s. Figure 19 graphically shows the data collected in the Table 4: open load input power is about 200 mW, while the efficiency goes from about 30% to about 65%, when load is increased from 100 mW to 500 mW.

Table 4. EVLG599-250WLLC efficiency @ light loads

Load [mW]	Pin [W]	Vout [V]	Iout [A]	Rload [Ω]	Pout [mW]	EFF [%]
0	198	24.331	0.000	∞	-	-
100	323	24.324	4.109	5917	99.96	30.9
250	494	24.322	10.321	2367	251.03	50.8
500	777	24.319	20.636	1183	501.84	64.6

Figure 19. **EVLG599-250WLLC efficiency @ light loads**



6 Evaluation board typical waveforms

Typical waveforms of the evaluation board are shown during startup, steady state in continuous switching and in burst mode, overload, load transient and turn-off at full load. Weak sensitivity of burst mode output current with respect to the input voltage of the half-bridge and the 100 Hz ripple rejection between the output voltage and the input voltage is shown as well.

Figure 20 and Figure 21 show the startup operation at full load and open load, respectively. The test was done by applying 400 Vdc to the connector J1 and then bringing the VCC pin of the STNRG599 to V_{VCCON} by means of an external power supply (HV startup of STNRG599A not used). In open load, the switching activity starts at power-up and stops only when CSS > 1 V (STBY is disabled if CSS < 1 V) and restarts after about 37 ms in burst mode, when STBY < 2 V.

Figure 20. EVLG599-250WLLC turn-on at full load

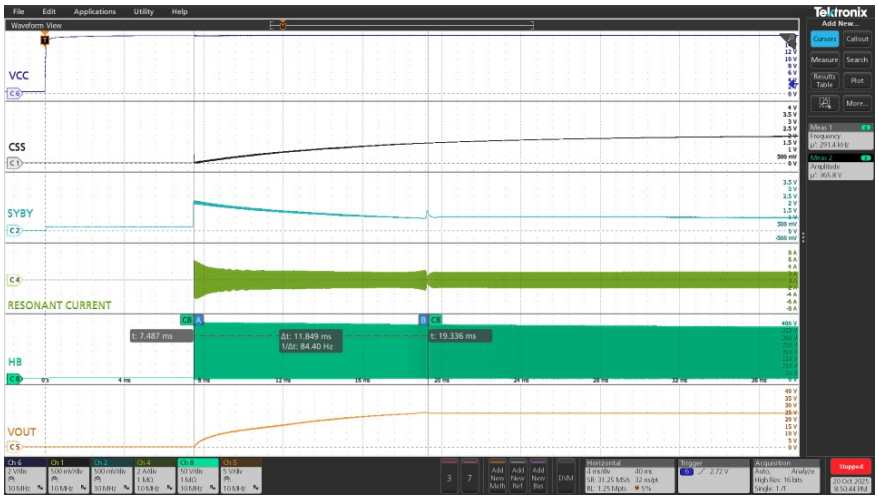


Figure 21. EVLG599-250WLLC turn-on at open load

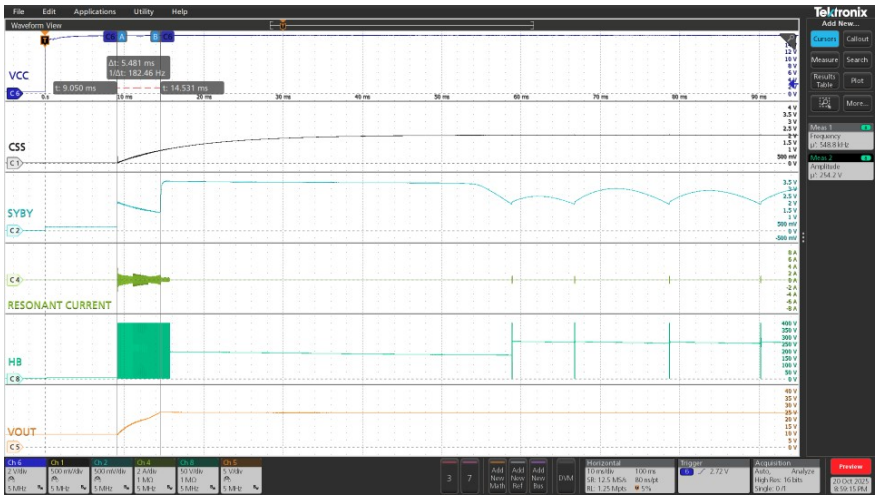


Figure 22 is a detail of the turn-on at full load showing the safe start procedure of STNRG599A in action, preventing hard switching events during the first cycles.

Figure 22. Safe start procedure, turn-on in full load

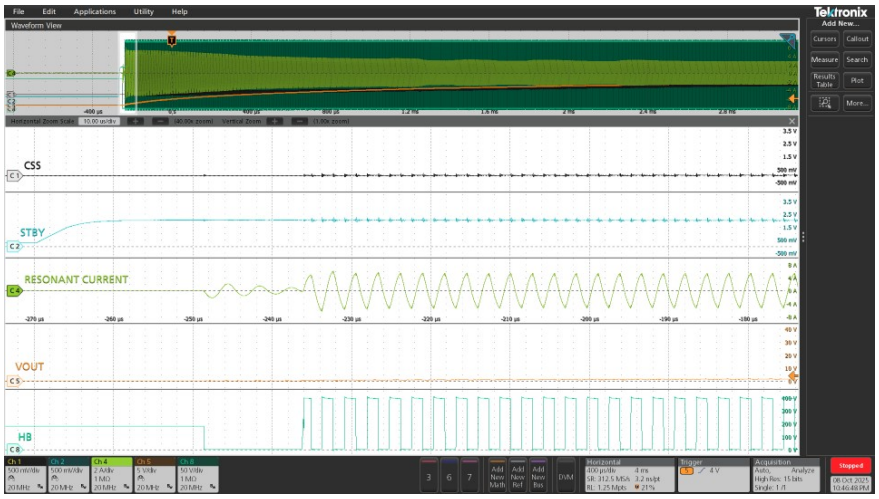


Figure 23 shows the turn-on of the converter by the embedded HV startup generator. The DC source connected at J1 is the input voltage of the half-bridge leg embedded in the MASTERGAN1L: when its voltage reaches the DC brown-in threshold (385 V, typ), the switching activity can take place. The embedded HV startup generator charges the capacitor C9 connected at the VCC pin of the STNRG599A from the AC source connected at J7, to bring it to V_{VCCON}. The capacitor C9 is typically charged by a current that is about 9 mA once the voltage at the VCC pin has reached V_{VCC_SO} (1 V, typ). When the switching activity begins, the on-board power supply, based on the auxiliary winding of the transformer, starts feeding the STNRG599A and the MASTERGAN1L daughterboard. The HV startup generator is kept on for about 80 ms, then is turned off. Note that the voltage at the VCC pin decreases after reaching V_{VCCON}, because the power consumption of the STNRG599A increases when the switching activity starts.

Figure 23. Turn-on at full load, by the embedded HV startup generator

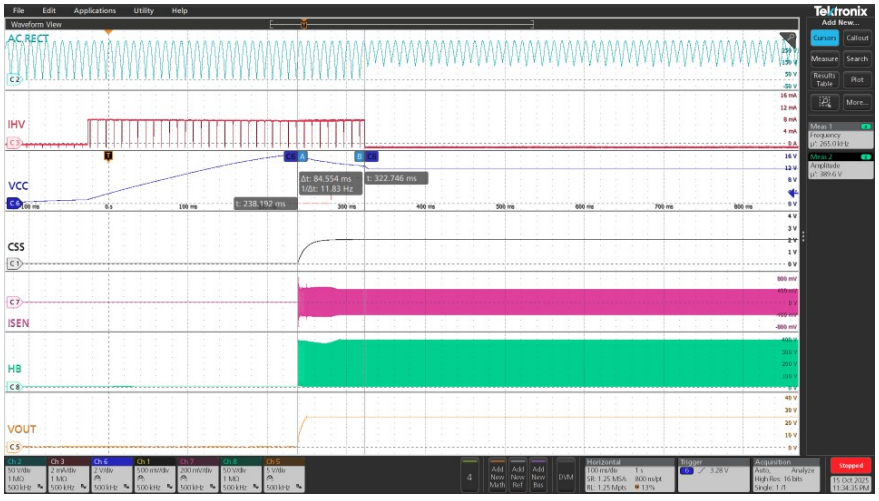


Figure 24 and Figure 25 show the steady-state operations at full load and open load, with Vin = 400 Vdc. At full load, the switching frequency is 264 kHz, the output voltage is 24.12 V and V_{STBY} ≈ 1 V. In burst mode, the output voltage is between 24.15 V and 24.09 V. V_{STBY} rising to 2 V causes the stop of the switching activity, while V_{STBY} falling to 1.875 V causes the restart of the switching activity. The burst mode period is about 18 ms with a switching packet of about 67 µs. Details of burst mode operation are given hereinafter.

Figure 24. **Operation at 400 V / 10.4 A (full load)**

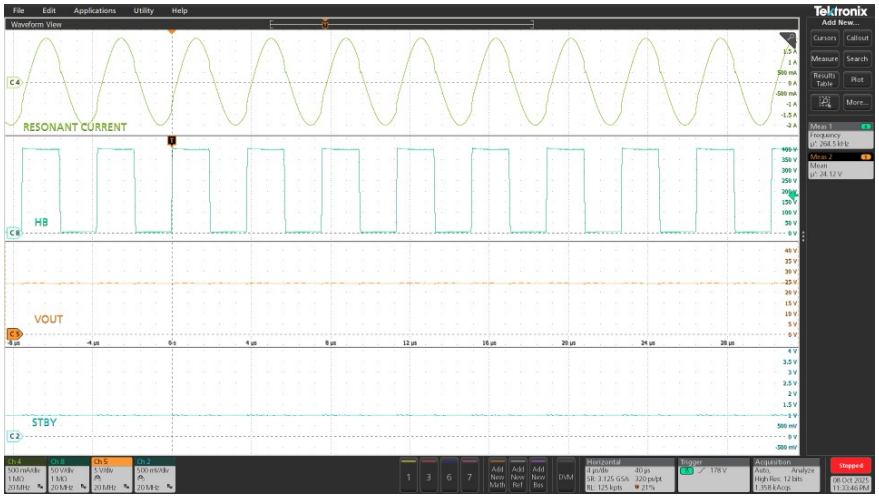


Figure 25. **Operation at 400 V / 0.0 A (open load)**

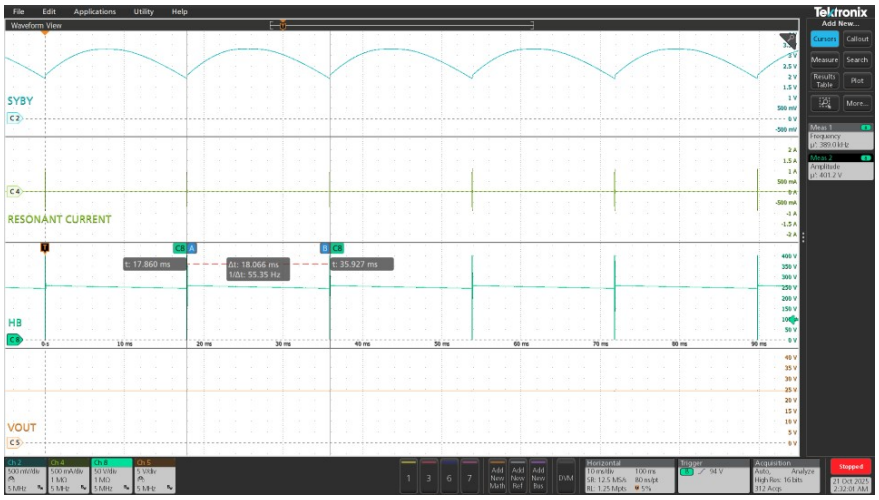


Figure 26 and Figure 27 show the output voltage ripple in full load and in open load, at Vin = 400 V: the ripple amplitude is 290 mVpp and 60 mVpp, respectively. For the full-load case, the full high-frequency ripple has been measured, while for the open-load case, the measured ripple is the low-frequency one, due to burst mode operation (high frequency component discarded).

Figure 26. **High-frequency output voltage ripple at full load, 400 V**

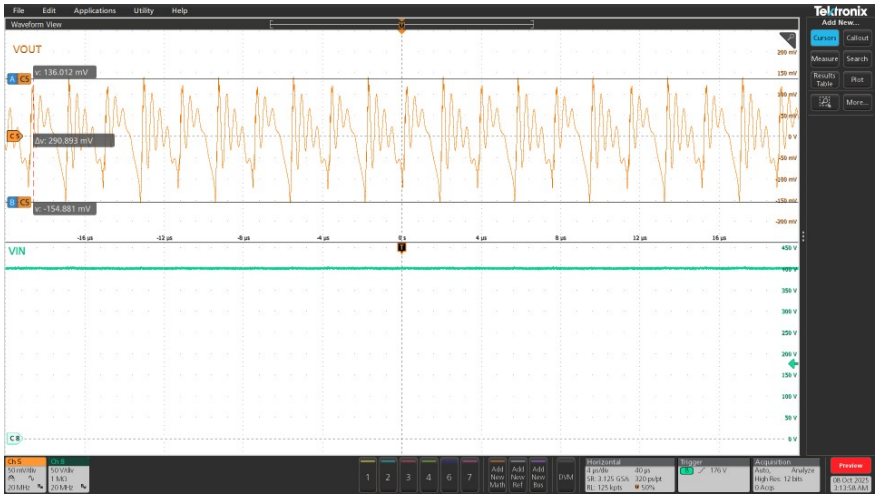
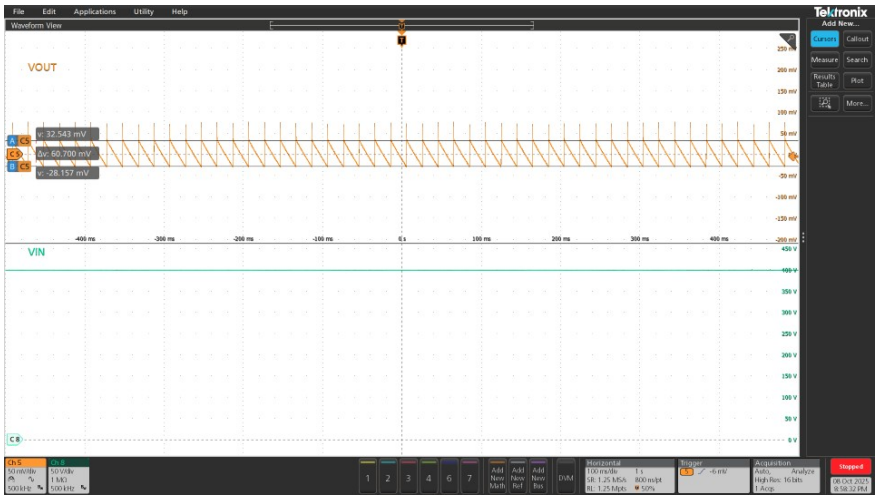


Figure 27. **Low-frequency output voltage ripple at open load, 400 V**



The burst mode operation threshold is about 1.5 A at Vin = 400 V. From this load level down to open load, regulation is obtained by switching packets separated by idle periods. When the load is reduced, mainly depending on the way the control loop is compensated, the length of the switching packet decreases while the idle period increases. At a certain point, the minimum packet length is reached and then regulation is maintained by increasing the idle period. Burst mode operation allows improving the efficiency of the converter at light loads by reducing the average number of switching cycles in the time unit. The STNRG599A is based on a phase-shift control methodology: because of that, the burst mode entry level is set in terms of the phase (between the input voltage and the input current of the resonant tank) at which the burst mode operation must start. As the phase is linked to the transferred power, the burst mode threshold is well linked to the output load. Significant signals during burst mode operation are shown in Figure 28. When the voltage at the STBY pin reaches 2 V (rising), the switching activity stops, the idle period starts and continues until the voltage at the STBY pin falls to 1.9 V – 25 mV = 1.875 V, which is the voltage at which switching activity restarts. To reduce the number of switching cycles in the burst packet, and thus the average number of switching cycles in the unit time to increase the efficiency, the STNRG599A implements an additional feature called Enhanced Burst Mode: during the last pulses of a burst packet, the phase shift is internally set to 30% less than the programmed value to enter burst mode and this increases the switching current amplitude (Figure 29). The burst mode function is disabled as far as the voltage at the CSS pin of the STNRG599A is less than 1 V. In other words, if V_{CSS}< 1 V, switching activity is not stopped by V_{STBY}> 2 V.

Figure 28. **Burst mode operation in open load, long time base**

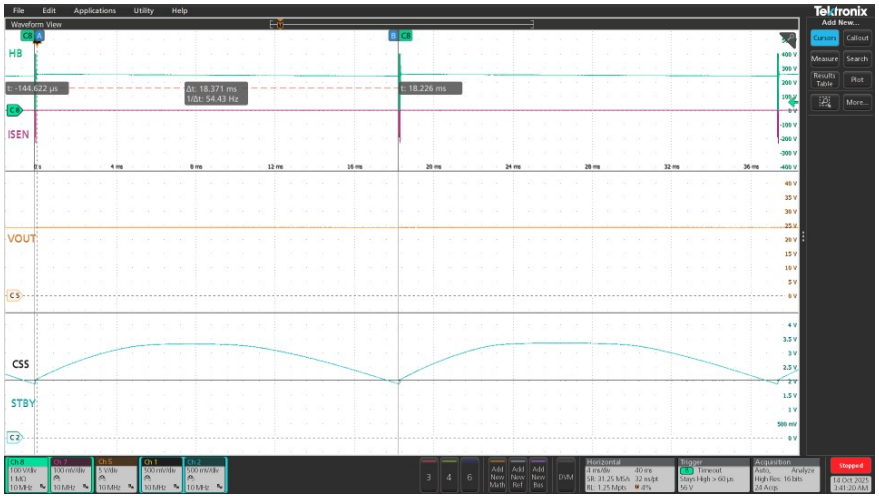
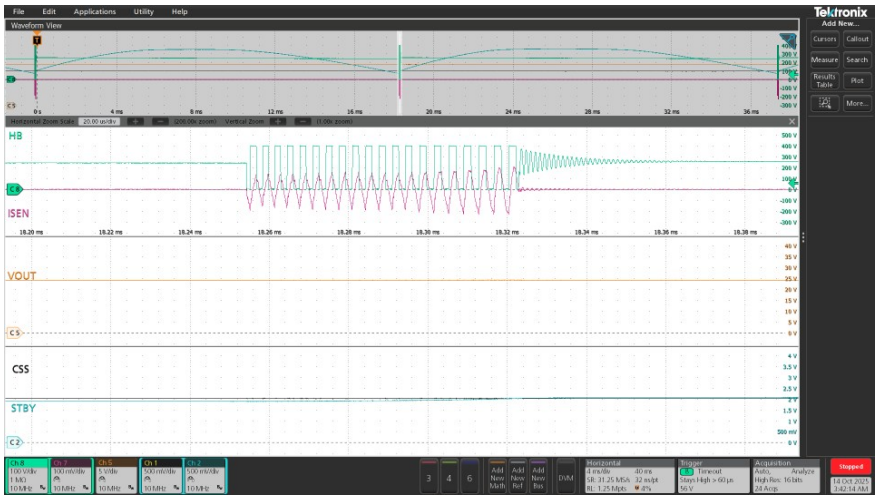


Figure 29. **Burst mode operation in open load, switching packet detail**



An important characteristic of the phase-shift control method is that the burst mode threshold (output current at which operation changes from continuous switching to burst mode) is weakly dependent on the input voltage of the half-bridge. This characteristic is shown in the following figures where the output current, at which the burst mode operation starts / stops (at load decreasing / increasing, respectively), is a function of the half-bridge input voltage. In Figure 30, the vertical scale is the whole output current range while in Figure 31 the reduced vertical scale fosters to distinguish between burst mode entry / exit levels. The burst mode output current variation with respect to the input voltage is 425 mA / 75 V ≈ 5.7 mA/V.

Figure 30. **Iout at burst mode threshold VS half-bridge Vin**

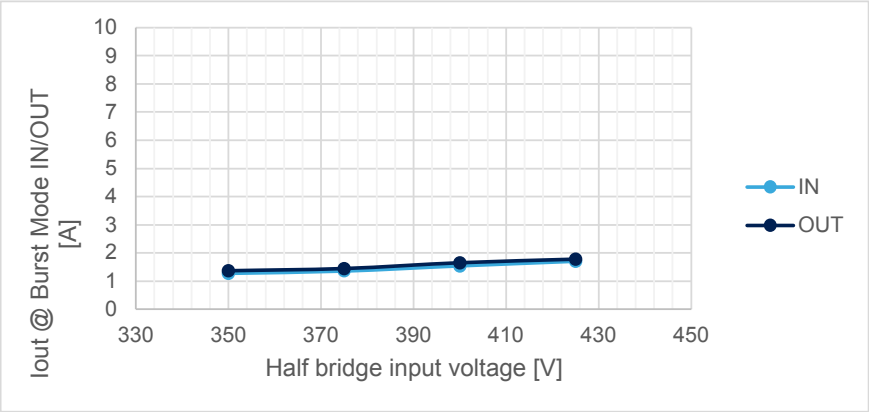
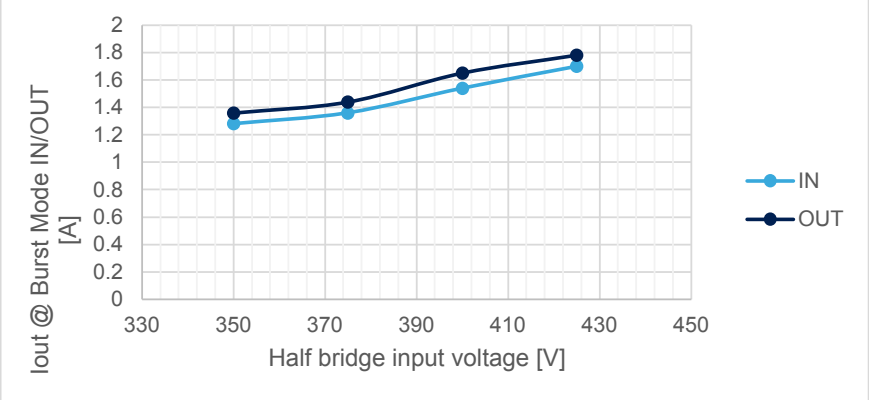
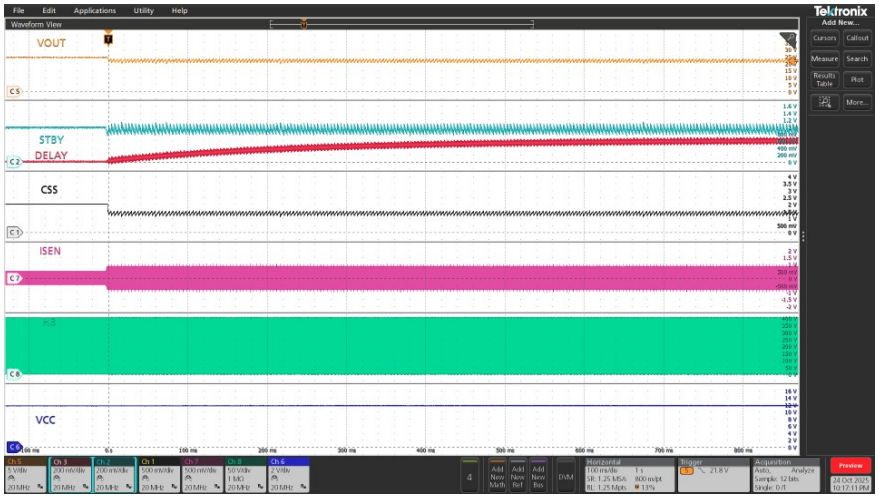


Figure 31. **Iout at burst mode threshold VS half-bridge Vin (detail)**



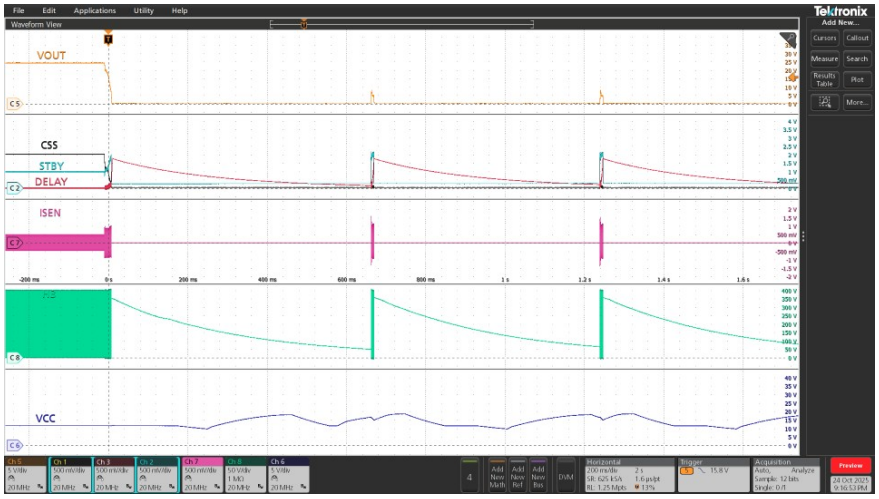
The EVLG599-250WLLC demo board is protected against output overload and short-circuit by an internal mechanism of the STNRG599A. The controller detects any overload by the voltage at the ISEN pin. Considering the voltage V_{ISEN} at the input terminal of the series capacitance to the ISEN pin, C3, if the output overload is such that 0.87 V < V_{ISEN} < 1.5 V, then the STNRG599 discharges the soft-start capacitor, C5, for 5 µs, through an internal 120 Ω resistor, and charges the delay capacitor, C17, by a constant current of 250 µA for 5 µs. The purpose of discharging the soft-start capacitor is to increase the phase shift / switching frequency and, therefore, to reduce the power transferred to the load. The purpose of charging the delay capacitor is to keep a sort of memory of the overload events. If the overload is kept, then the delay capacitor can be charged up to 1 V: at this point, the soft-start capacitor is fully discharged to limit the power transfer and the delay capacitor is charged to 1.75 V to stop the switching activity. Now, the delay capacitor is discharged by the delay resistor, R23, which is in parallel. When V_{DELAY} falls below 0.2 V, the switching activity can restart (with soft-start because the corresponding capacitor has been discharged). If the overload is still present, then the previously described mechanism is repeated, resulting in hiccup operation by the converter. Hiccup operation avoids thermal stress to the converter, in case of overload lasting for a long time, and allows the restart of the switching activity and the normal operation of the converter, when the overload is removed. Figure 32 shows a condition like “just above the full load”: at some time, the overload is applied and regulation is no longer maintained because of the repeated occurrences of the OCP1 event that keep the soft-start capacitor below the steady state value (2 V). The voltage on the delay capacitor does not reach 1 V, so the switching activity is not stopped.

Figure 32. **OCP1 protection in action**



If the overload is such that VISEN > 1.5 V (OCP2), as in the case of a short-circuit, for example, the switching activity is immediately stopped: the soft-start capacitor is fully discharged while the delay capacitor is charged to 1.75 V. At this point, the discharge of the delay capacitor into the delay resistor takes place: the switching activity is resumed by a soft-start procedure when the voltage at the DELAY pin falls below 0.2 V. If the short-circuit persists, then hiccup operation is observed. Figure 33 shows hiccup operation in case of output short-circuits. Note that, for hiccup operation, the embedded HV startup generator must be supplied by a rectified mains voltage.

Figure 33. **Hiccup operation after OCP2 protection**



The response of the converter to the load transient is shown in the following figures. The open load time interval is set to maximize the output voltage drop, that is in such a way that there is not a switching packet by burst mode during the open load time interval. The loaded time interval (full or half) is 100 ms.

Figure 34 is for full / open load transition: in this case, the peak-to-peak output voltage variation is 1.2 V, which is 5% of the regulated voltage (overshoot is 300 mV, undershoot is 900 mV).

Figure 34. Full / open load transient, Vin = 400 V

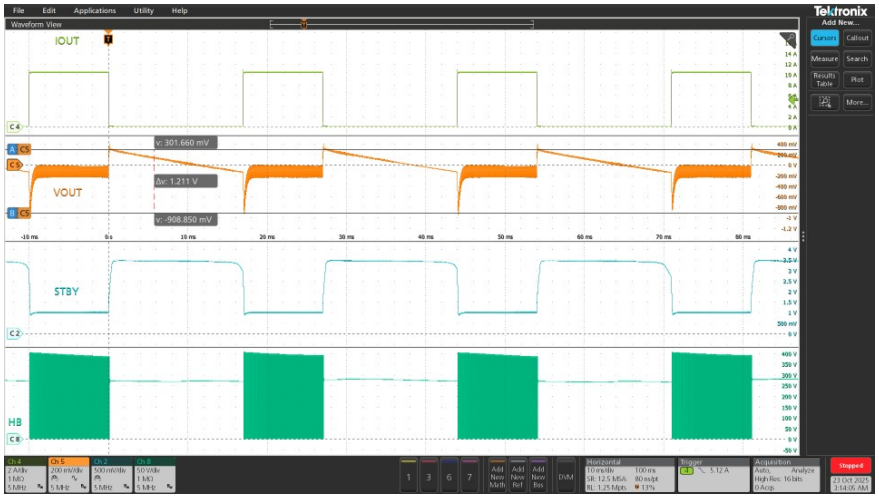


Figure 35 is for half / open load transition: in this case, the peak-to-peak output voltage variation is 0.73 V, which is 3% of the regulated voltage (overshoot is 210 mV, undershoot is 520 mV).

Figure 35. Half / open load transient, Vin = 400 V

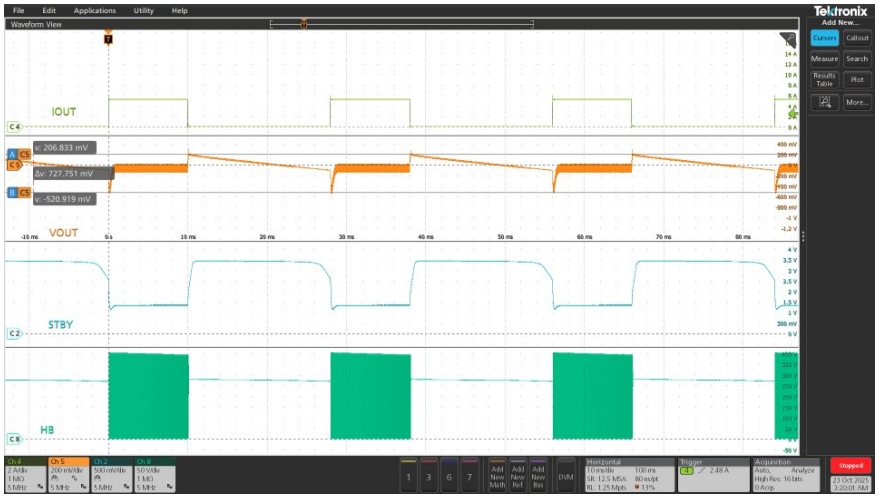
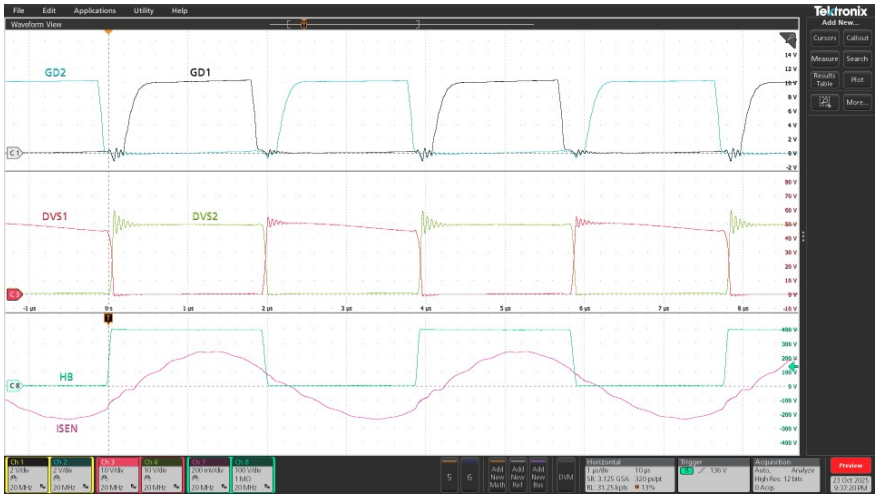


Figure 36 depicts the converter turn-off when the switch connecting the external DC source to the half-bridge leg is opened while the converter is operating at 400 V / 10.4 A. When the external DC source is disconnected, the converter takes the energy from the bulk capacitor, C1, whose voltage starts decreasing. To maintain regulation, the resonant current increases because the phase shift control loop reduces the phase between the half-bridge voltage and the resonant tank current. The regular envelope of the resonant current, showing an amplitude that is increasing without oscillation, is evidence of the good stability of the control loop. Eventually, just before the DC brown-out, the resonant current amplitude triggers OCP1: the soft-start capacitor is partially discharged and output voltage regulation ceases. The switching activity stops at the DC brown-out.

Figure 36. **External DC source disconnection at 400 V / 10.4 A**

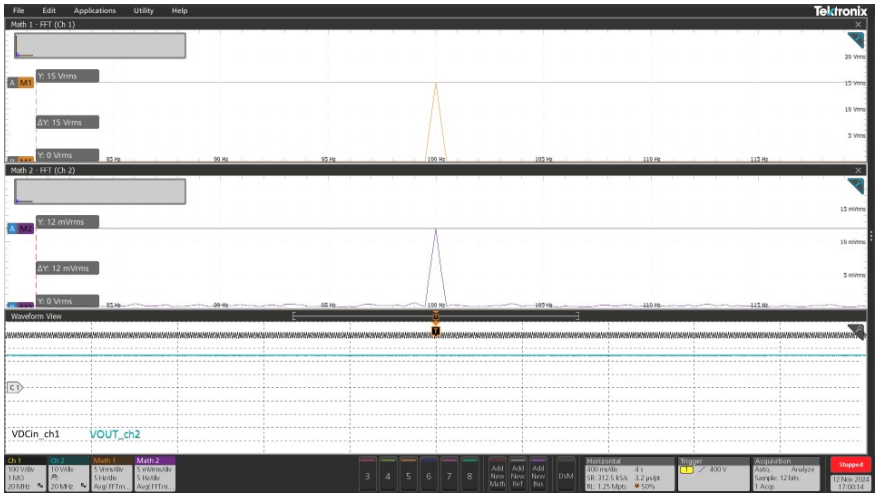
On the secondary side, synchronous rectification based on SRK2001A is used. Relevant waveforms at 400 V / 10.4 A are shown in Figure 37.

Figure 37. **Secondary side main waveforms at 400 V / 10.4 A**



The ripple rejection at full load (10.4 A) from the input voltage to the output voltage of the 100 Hz ripple, typical of a PFC front end, is measured. The input voltage is the usual 400 V over which a sinusoidal voltage at 100 Hz / 15 Vrms is superimposed. The oscilloscope has been used to calculate the FFTs of the input and output voltages: Figure 38 shows the measurement result. The output voltage ripple is 12 mVrms. Considering 15 Vrms of the input voltage, the attenuation is about -62 dB.

Figure 38. **100 Hz ripple rejection at 400 V / 10.4 A**



7 Thermal map

Figure 39 shows the thermal map of the resonant transformer side of the EVLG599-250WLLC after about 20 minutes 400 V / 10.4 A, while Table 5 highlights the temperatures of the transformer winding and of the magnetic core that are the hottest spots. Figure 40 and Table 6 show the thermal behaviour of the board when cooled by a fan whose measured air flow is 1.2 m/s (air temperature 25.0 °C).

Figure 39. EVLG599-250WLLC thermal map @ 400 V / 10.4 A, uncooled

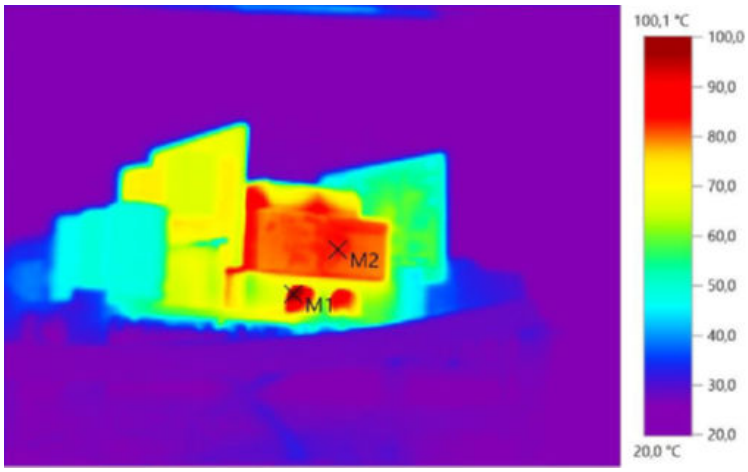


Table 5. Hottest spots, uncooled board

M1	Transformer winding	102.0 °C
M2	Magnetic core	83.7 °C

Figure 40. EVLG599-250WLLC thermal map @ 400 V / 10.4 A, cooled

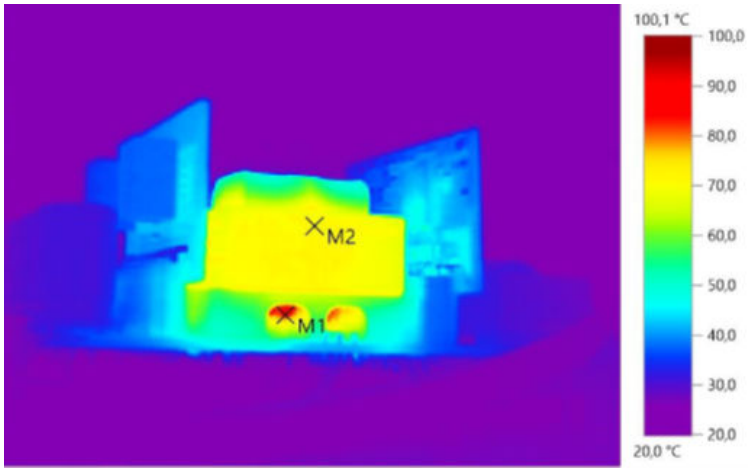


Table 6. Hottest spots, cooled board

M1	Transformer winding	84.7 °C
M2	Magnetic core	71.8 °C

8 Bill of materials

8.1 STNRG599A motherboard

Table 7. **Bill of materials, STNRG599A motherboard**

Ref.	Value	Package	Description	Manufacturer
C1	47uF	Radial	Radial electrolytic cap. - 450V, ±20%	Nichicon
C2	100pF	1206	SMD multilayer ceramic cap. - 1kV, ±10%	Johanson Technology
C3	220pF	0805	SMD multilayer ceramic cap. - 50V, ±5%	KEMET
C4	N.M.			
C5	820nF	0805	SMD multilayer ceramic cap. - 25V, ±10%	Murata
C6	4.7nF	Plastic radial	Radial polypropylene metall. cap. - 1kV, ±5%	KEMET
C7	4.7nF	Plastic radial	Radial polypropylene metall. cap. - 1kV, ±5%	KEMET
C8	N.M.			
C9	470nF	1206	SMD multilayer ceramic cap. - 50V, ±10%	Walsin
C10	N.M.			
C11	10nF	1206	SMD multilayer ceramic cap. - 50V, ±10%	Walsin
C12	2.2nF	Radial	Radial Y1 Safety ceramic cap. - 300V, ±20%	Murata
C13	10nF	0805	SMD multilayer ceramic cap. - 50V, ±10%	Murata
C14	100pF	0805	SMD multilayer ceramic cap. - 50V, ±5%	Walsin
C15	47uF	Radial	Radial electrolytic cap. - 50V, ±20%	Rubycon
C16	47uF	Radial	Radial electrolytic cap. - 50V, ±20%	Rubycon
C17	470nF	0805	SMD multilayer ceramic cap. - 50V, ±10%	KEMET
C18	470nF	1206	SMD multilayer ceramic cap. - 50V, ±10%	Walsin
C19	47uF	Radial	Radial electrolytic cap. - 50V, ±20%	Rubycon
C20	N.M.			
C21	N.M.			
C22	N.M.			
C23	470uF	Radial	Radial electrolytic cap. - 35V, ±20%	Panasonic
C24	470uF	Radial	Radial electrolytic cap. - 35V, ±20%	Panasonic
C25	470uF	Radial	Radial electrolytic cap. - 35V, ±20%	Panasonic
C26	N.M.			
C32	1uF	1206	SMD multilayer ceramic cap. - 50V, ±10%	KEMET
C34	1uF	0805	SMD multilayer ceramic cap. - 50V, ±10%	KEMET
C35	1uF	1206	SMD multilayer ceramic cap. - 50V, ±10%	KEMET
C36	10pF	1206	SMD multilayer ceramic cap. - 1kV, ±5%	Yageo
D1	MB6S	TO-269AA	SMD bridge rectifier - 600V, 0.5A	VISHAY
D3	1N4148WS	SOD-323	SMD fast-switching rectifier - 100V, 0.35A	onsemi
D4	STPS1H100A	SMA	SMD Schottky rectifier - 100V, 1A	STMicroelectronics
D5	12V	SOD-323	SMD Zener diode - 12V, ±5%	Nexperia
D7	12V	SOD-323	SMD Zener diode - 12V, ±5%	Nexperia
D8	N.M			

Ref.	Value	Package	Description	Manufacturer
D9	N.M			
D10	BAT48ZFILM	SOD-123	SMD Schottky rectifier - 40V, 0.35A	STMicroelectronics
J1	MKDSN	5.08mm	Screw conn. term., single-row, 5.08 pitch, 8 depth, 10 height, 13,5A AWG 16-26, 0,14-1,5mm2 - 400V	Phoenix Contact
J2	STRIP1X15PF		Female strip 15pin PRECI-DIP poles pitch 2.54mm - 3A. Extract/remove pins 3 and 6 before mounting.	PRECI-DIP
J3	STRIP1X13PF		Female strip 13pin PRECI-DIP poles pitch 2.54mm - 3A	PRECI-DIP
J4	MOLEX4P	6410	Connector header vertical 4POS 2.54 mm	MOLEX
J5	Faston_90	6.35mm	Conn. FASTON male 6,35mm right angle (PCB hole 1.2mm)	TE Connectivity
J6	Faston_90	6.35mm	Conn. FASTON male 6,35mm right angle (PCB hole 1.2mm)	TE Connectivity
J7	MORS_2P	5.08mm	Screw conn. term., single-row, 5.08 pitch, 8 depth, 10 height, AWG 16-28, 13.5A - 300V	TE Connectivity
JPX1			Tinned copper wire d = 0,7mm, SWG22, l ≈ 35mm black PVC sheet d_int = 1mm, l ≈ 25mm.	
Q1	BC847C	SOT23	SMD NPN transistor General purpose	onsemi
Q2	BC847C	SOT23	SMD NPN transistor General purpose	onsemi
R1	3M3	1206	SMD resistor - 200V, 1/4W, 1%	Yageo
R2	0R	1206	SMD resistor - 200V, 1/4W, 5%	Yageo
R3	12K	0805	SMD resistor - 150V, 1/8W, 1%	Yageo
R4	0R	0805	SMD resistor - 150V, 1/8W, 5%	Yageo
R5	3M3	1206	SMD resistor - 200V, 1/4W, 1%	Yageo
R6	0R	0805	SMD resistor - 150V, 1/8W, 5%	Yageo
R7	4K3	0805	SMD resistor - 150V, 1/8W, 1%	VISHAY
R8	120K	0805	SMD resistor - 150V, 1/8W, 1%	Yageo
R9	3M3	1206	SMD resistor - 200V, 1/4W, 1%	Yageo
R10	22K	0805	SMD resistor - 150V, 1/8W, 1%	Yageo
R11	20R	0805	SMD resistor - 1/8W, 1%	Yageo
R12	0R	0805	SMD resistor - 150V, 1/8W, 5%	Yageo
R13	N.M.			
R14	N.M.			
R15	100R	1206	SMD resistor - 200V, 1/4W, 1%	Yageo
R16	62K	0805	SMD resistor - 150V, 1/10W, 1%	Yageo
R17	22K	0805	SMD resistor - 150V, 1/8W, 1%	Yageo
R18	N.M.			
R19	2R2	1206	SMD resistor - 1/4W, 1%	Yageo
R20	3K3	0805	SMD resistor - 150V, 1/8W, 1%	Yageo
R21	N.M.			
R22	N.M.			
R23	560K	0805	SMD resistor - 150V, 1/10W, 1%	Yageo

Ref.	Value	Package	Description	Manufacturer
R24	3K9	0805	SMD resistor - 150V, 1/8W, 1%	Yageo
R25	0R	0805	SMD resistor - 150V, 1/8W, 5%	Yageo
R26	N.M.			
R27	2K	0805	SMD resistor - 150V, 1/8W, 1%	VISHAY
R28	91K	0805	SMD resistor - 150V, 1/8W, 1%	Yageo
R29	130K	0805	SMD resistor - 150V, 1/8W, 1%	Yageo
R30	N.M.			
R31	15K	0805	SMD resistor - 150V, 1/8W, 1%	Yageo
R32	470K	0805	SMD resistor - 150V, 1/8W, 1%	Yageo
R33	47K	1206	SMD resistor - 1/4W, 1%	Yageo
R34	1K1	1206	SMD resistor - 1/2W, 1%	Stackpole Electr. Inc.
R35	4K7	0805	SMD resistor - 150V, 1/8W, 1%	Yageo
R36	0R	0805	SMD resistor - 150V, 1/8W, 5%	Yageo
R37	1K1	1206	SMD resistor - 1/2W, 1%	Stackpole Electr. Inc.
R38	39K	0805	SMD resistor - 150V, 1/8W, 1%	Yageo
R39	N.M.			
R40	0R	0805	SMD resistor - 150V, 1/8W, 5%	Yageo
R41	N.M.			
R42	N.M.			
R43	0R	1206	SMD resistor - 200V, 1/4W, 5%	Yageo
T1	2204.0060		250W resonant LLC transformer	AQ Magnetica
U1	STNRG599A	SOIC16	Enhanced resonant controller	STMicroelectronics
U2	SFH610A-2X006	DIP4	Optocoupler	VISHAY
U3	TL432AIL3T	SOT23	Volt. ref. adjustable shunt SOT23	STMicroelectronics

8.2 MASTERGAN1L daughterboard

Table 8. Bill of materials, MASTERGAN1L daughterboard

Ref.	Value	Package	Description	Manufacturer
C102	1nF	0603	SMD multilayer ceramic cap. - 50V, ±10%	KEMET
C103	10uF	1206	SMD multilayer ceramic cap. - 50V, ±10%	SAMSUNG
C104	10uF	1206	SMD multilayer ceramic cap. - 50V, ±10%	SAMSUNG
C105	1uF	0805	SMD multilayer ceramic cap. - 50V, ±10%	Taiyo Yuden
C106	1uF	0805	SMD multilayer ceramic cap. - 50V, ±10%	Taiyo Yuden
C107	100nF	1812	SMD multilayer ceramic cap. - 630V, ±10%	TDK
C108	100nF	0603	SMD multilayer ceramic cap. - 50V, ±20%	TDK
C109	47nF	0603	SMD multilayer ceramic cap. - 50V, ±10%	AVX
C111	100pF	0603	SMD multilayer ceramic cap. - 50V, ±5%	TDK
C113	100nF	0603	SMD multilayer ceramic cap. - 50V, ±20%	TDK
C115	10pF	0603	SMD multilayer ceramic cap. - 50V, ±5%	KEMET
C116	10pF	0603	SMD multilayer ceramic cap. - 50V, ±5%	KEMET

Ref.	Value	Package	Description	Manufacturer
D101	1N4148WS	SOD-323	SMD fast-switching rectifier - 100V, 0.35A	onsemi
D102	STTH1R06A	SMA	SMD rectifier - 600V, 1A	STMicroelectronics
D106	STTH1R06A	SMA	SMD rectifier - 600V, 1A	STMicroelectronics
D107	STTH1R06A	SMA	SMD rectifier - 600V, 1A	STMicroelectronics
D110	1N4148WS	SOD-323	SMD fast-switching rectifier - 100V, 0.35A	onsemi
D111	6V2	SOD-323	SMD Zener diode - 6.2V, 0.3W, ±5%	Nexperia
J101	HEADER 15		Single-row right angle PCB header 15 ways	Würth Elektronik
Q101	BC847C	SOT23	SMD NPN transistor general purpose	onsemi
R102	4R7	0805	SMD resistor - 1/10W, 1%	Yageo
R103	18K	0603	SMD resistor - 1/10W, 1%	Yageo
R104	3K9	0603	SMD resistor - 1/10W, 1%	Yageo
R106	10K	0603	SMD resistor - 1/10W, 1%	Yageo
R109	10K	0603	SMD resistor - 1/10W, 1%	Yageo
R111	10R	0603	SMD resistor - 75V, 1/10W, 1%	Yageo
R112	10R	0603	SMD resistor - 75V, 1/10W, 1%	Yageo
R114	4R7	0805	SMD resistor - 1/10W, 1%	Yageo
U101	TL432AIL3T	SOT23	Volt. ref. adjustable shunt SOT23	STMicroelectronics
U103	MASTERGAN1L	VFQFPN 9x9x1.0-48L	High-voltage enhancement mode GaN half-bridge with gate driver	STMicroelectronics

8.3 SRK2001A daughterboard

Table 9. Bill of materials, SRK2001A daughterboard

Ref.	Value	Package	Description	Manufacturer
C201	1uF	0805	SMD multilayer ceramic cap. - 25V, ±10%	
D201	N.M.			
D202	N.M.			
HS1	HEATSINK		Heatsink black anodized aluminum 71°K/W for SMD (8x10x6mm)	Fischer Elektronik
HS2	HEATSINK		Heatsink black anodized aluminum 71°K/W for SMD (8x10x6mm)	Fischer Elektronik
JP201	STRIP13-M-90		13p right angle male header	Würth Elektronik
Q201	STL120N8F7	PowerFLAT5x6	N-Channel Power MOSFET - 80V, 120A	STMicroelectronics
Q202	STL120N8F7	PowerFLAT5x6	N-Channel Power MOSFET - 80V, 120A	STMicroelectronics
R201	100R	1206	SMD resistor - 200V, 1/4W, 1%	Yageo
R202	100R	1206	SMD resistor - 200V, 1/4W, 1%	Yageo
R203	0R	1206	SMD resistor - 200V, 1/4W, 5%	Yageo
R204	0R	1206	SMD resistor - 200V, 1/4W, 5%	Yageo
R205	0R	0805	SMD resistor - 150V, 1/8W, 5%	Yageo
R206	N.M.			
U201	SRK2001A	SSOP10	SRK2001 SR controller	STMicroelectronics

9 LLC transformer specification

Table 10. LLC transformer, general description and characteristics

Application type	Consumer, home appliance
Transformer type	Open
Coil former	Horizontal type, 5+4 pins, 2 slots
Max. temp. rise	45 °C
Max. op. ambient temp	60 °C
Mains insulation	According to EN60950

Table 11. LLC transformer, electrical characteristics

Converter topology	Half-bridge resonant
Core type	DMR96
Min. operating frequency	100 kHz
Typical operating frequency	250 kHz
Primary inductance (1)	210 µH ±10% @ 1 kHz – 0.25 V
Leakage inductance(2)	45 µH ±5% @ 100 kHz – 0.25 V

1. *Measured between pins 1 / 3.*
2. *Measured between pins 1 / 3 with ONLY a secondary winding shorted. Difference between the two measured leakage inductances has to be < 5 %.*

Table 12. LLC transformer, DC output characteristics

	LLC	Aux
DC output voltage	24 V	16 V
DC load	10 A	0.05 A

Figure 41. LLC transformer, electrical diagram and pin numbering

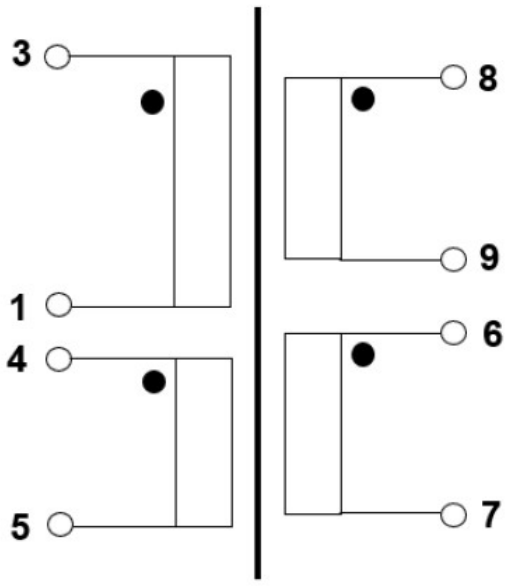


Table 13. LLC transformer, winding specifications

Pins	Winding	I_{RMS} [A]	# Turns	Wire type
1 - 3	Primary	1.68	27	40 x 0.1 Litz
-	-	-	-	-
6 - 7	Sec. A(1)	6.9	3	2 x 60 x 0.10 Litz
8 - 9	Sec. B(1)	6.9	3	2 x 60 x 0.10 Litz
-	-	-	-	-
4 - 5	Aux(2)	0.05	2	0.224 G2

1. *Secondary windings A and B must be wound in parallel.*
2. *Aux winding wound on top of primary winding, turns spread on whole winding.*

Figure 42. LLC transformer, mechanical aspect

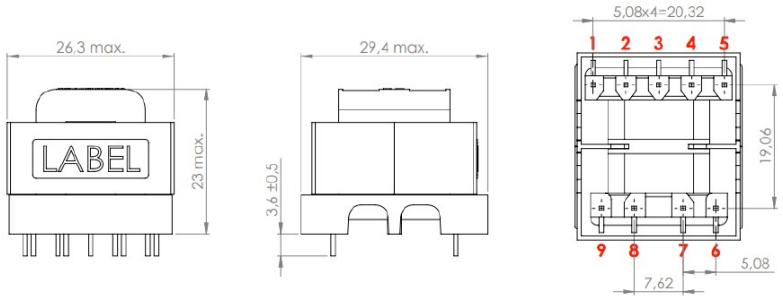


Table 14. LLC transformer, mechanical description and dimension

Coil former type	Horizontal, 5+4 PINS
Maximum height from PCB	23 mm
Pin distance	5.8 mm (all but 7 / 8) / 7.62 mm (7 / 8)
Row distance	19 mm
Pin dimension	0.7 mm x 0.7 mm

10 References

[1] MASTERGAN1L: “DS14355” datasheet on www.st.com
[2] STNRG599A: “DS15052” datasheet on www.st.com
[3] SRK2001A: “DS11726” datasheet on www.st.com

Revision history

Table 15. **Document revision history**

Date	Version	Changes
11-Mar-2026	1	Initial release.

Contents

List of tables

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