Robustness of p-GaN transistors under drain overvoltage stress

Introduction

Power gallium nitride (GaN) transistors, particularly p-GaN devices, are a cornerstone of modern power electronics due to their superior switching speed, high efficiency, and compact form factor compared to traditional silicon-based transistors. These advantages make p-GaN transistors ideal for applications such as power supplies, motor drives, automotive systems, and renewable energy systems.

In real-world operating environments, power devices are frequently subjected to transient electrical stresses, including DC and transient overvoltage. These stresses can result from switching transitions, load variations, parasitic inductances, or external disturbances, potentially affecting device reliability and system performance.

This application note provides a comprehensive understanding of p-GaN transistor behavior under overvoltage and voltage overshoot conditions. It explores the underlying causes and characterizes the device's performance. By mastering these aspects, engineers can optimize power systems to leverage the benefits of p-GaN technology while mitigating risks associated with transient voltage stresses.

1 Overview of p-GaN transistor technology and applications

1.1 Technology

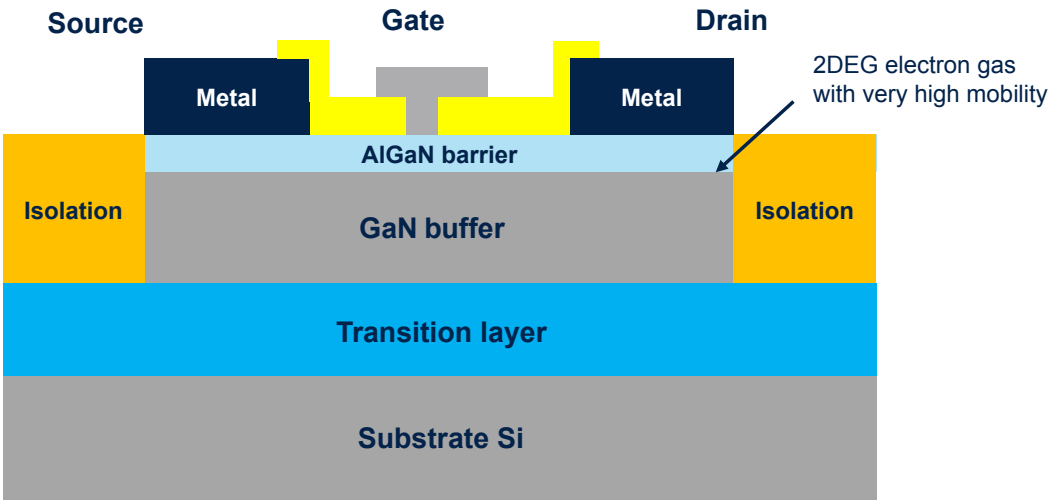
P-GaN transistors are enhancement-mode (e-mode) normally-off devices that leverage the unique material properties of GaN to achieve superior performance compared to traditional silicon MOSFETs. GaN is a wide band-gap semiconductor with a band-gap of approximately 3.4 eV, enabling higher breakdown voltages, faster switching speeds, and lower conduction losses.

The fabrication of p-GaN transistors involves the epitaxial growth of GaN layers on a silicon substrate.

The device structure includes:

- **GaN buffer layer**: Grown on silicon to accommodate lattice mismatch and reduce defects. This layer provides electrical isolation and supports the active layers above.
- **AlGaN barrier layer**: A thin layer of aluminum gallium nitride (AlGaN) is grown on top of the GaN channel. The difference in polarization between AlGaN and GaN creates a high-density two-dimensional electron gas (2DEG) at the interface, forming the conductive channel.
- **P-GaN gate layer**: A p-type GaN layer is selectively grown or implanted on the AlGaN barrier under the gate region. This p-type layer depletes the 2DEG channel beneath the gate at zero bias, enabling normally-off operation.
- **Source and drain contacts**: Ohmic contacts are formed on the GaN channel to allow current flow when the device is turned on.

Figure 1. Cross section of typical p-GaN structure

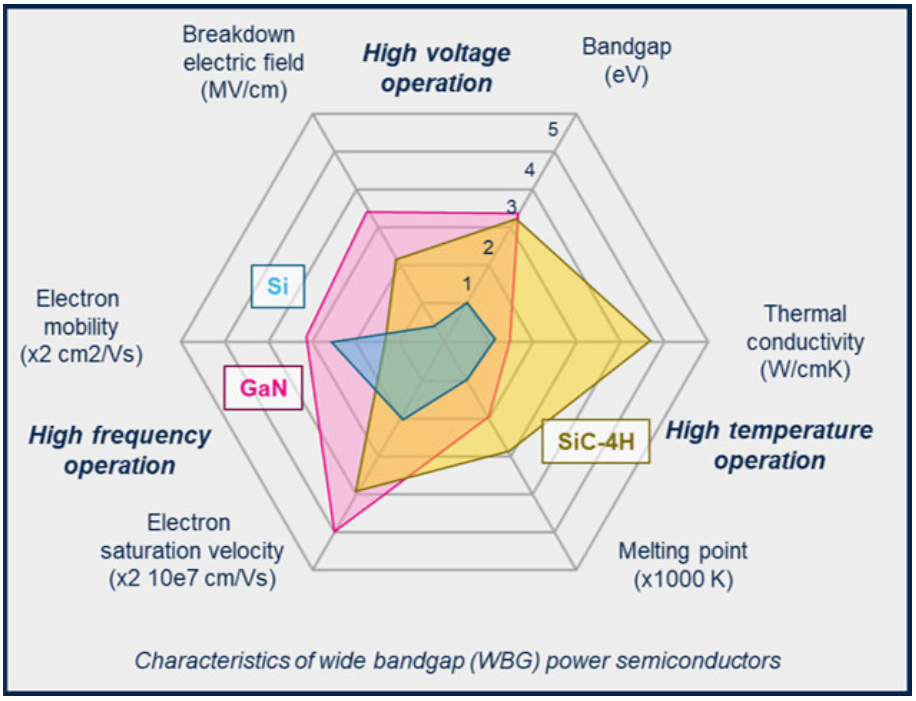


The key innovation in p-GaN transistors is the integration of the p-type GaN layer in the gate region, which contrasts with traditional AlGaN/GaN high electron mobility transistors (HEMTs) that are normally-on devices. The p-GaN gate depletes the channel at zero gate voltage, ensuring the transistor is **off** by default, which is critical for safe power system design [1].

When a positive gate voltage is applied, it neutralizes the p-GaN depletion effect, allowing the 2DEG channel to conduct. This results in low on-resistance and fast switching capabilities.

- **Normally-off operation**: Simplifies gate drive circuitry and enhances system safety
- **Low on-resistance $R_{DS(ON)}$**: Reduces conduction losses and improves efficiency
- **High switching speed**: Enables high-frequency operation, reducing passive component size
- **High breakdown voltage**: Supports robust operation in high-voltage applications
- **Compact device footprint**: Facilitates miniaturization of power converters.

Figure 2. Radar chart of the relevant material properties for Si, SiC, and GaN

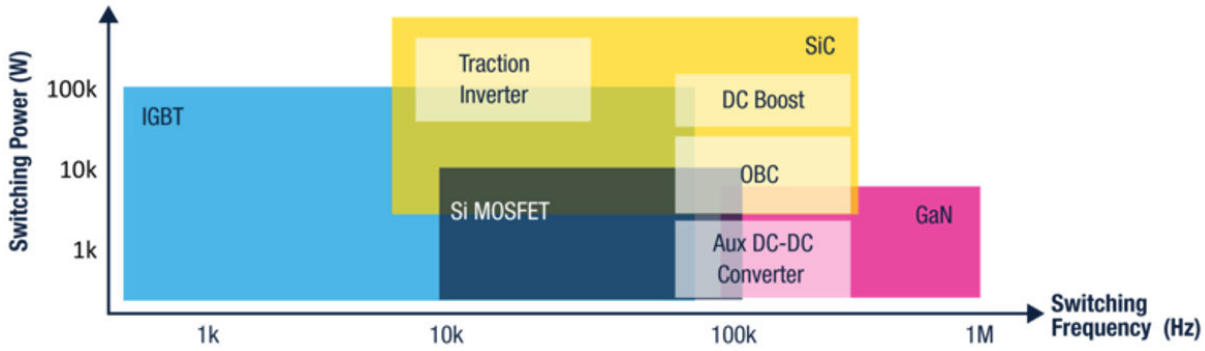


This combination of material properties, device structure, and fabrication techniques makes p-GaN transistors highly suitable for demanding power electronics applications, where efficiency, size, and reliability are critical.

Typical applications include:

- DC-DC converters for computing and telecom power supplies
- Motor drives and industrial automation
- Automotive electronics, including onboard chargers (OBC) and DC-DC converters
- Renewable energy systems, such as solar inverters and energy storage.

Figure 3. Comparison power transistor switching power vs switching frequency



1.2 No avalanche mechanism in the GaN HEMT transistor

In traditional silicon MOSFETs, the body diode is part of the device structure. It forms naturally due to the parasitic NPN transistor between the source and drain regions. This diode provides a conduction path for current when the MOSFET is reverse-biased, allowing current to flow in the reverse direction during switching events, such as in synchronous rectification.

When the drain-source voltage of a MOSFET exceeds its rated V_{DS} and avalanche breakdown occurs, avalanche current (I_{AS}) flows into the internal resistance R_{BE}. This causes a voltage to develop across the base-emitter junction of the parasitic bipolar transistor.

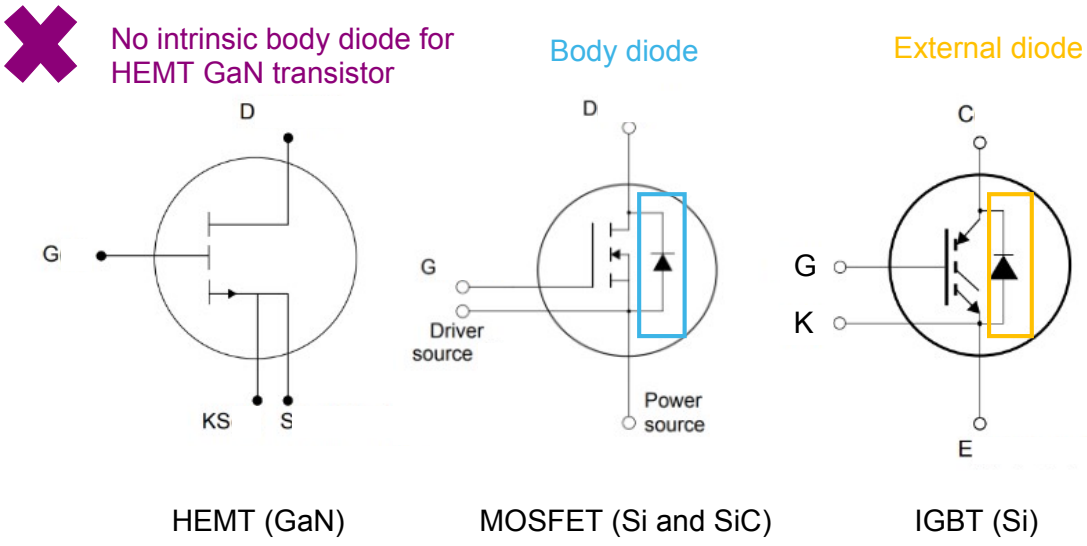
The parasitic bipolar transistor may activate during avalanche conditions, potentially leading to device failure if the design does not ensure adequate robustness.

In contrast, GaN transistors, particularly GaN high-electron-mobility transistors (HEMTs), including p-GaN devices, are based on a heterostructure rather than a bulk semiconductor junction. The conduction channel in GaN HEMTs is formed by a two-dimensional electron gas (2DEG) at the interface between the AlGaN barrier and GaN channel layers. This 2DEG channel is unipolar and does not involve a p-n junction between source and drain.

A significant challenge when using GaN HEMTs in various applications is their lack of intrinsic avalanche capability. Unlike Si or SiC MOSFETs and Si IGBTs, GaN HEMTs do not have a p-n junction between the source and drain terminals. Recent studies have shown that while Si and SiC MOSFETs dissipate surge energy through internal avalanche mechanisms, GaN HEMTs manage surge energy via an LC resonance formed between their output capacitance (C_{oss}) and the circuit's inductive loop. Device failure in GaN HEMTs typically occurs when the peak drain-to-source voltage exceeds the transistor's transient breakdown voltage (BV)[2].

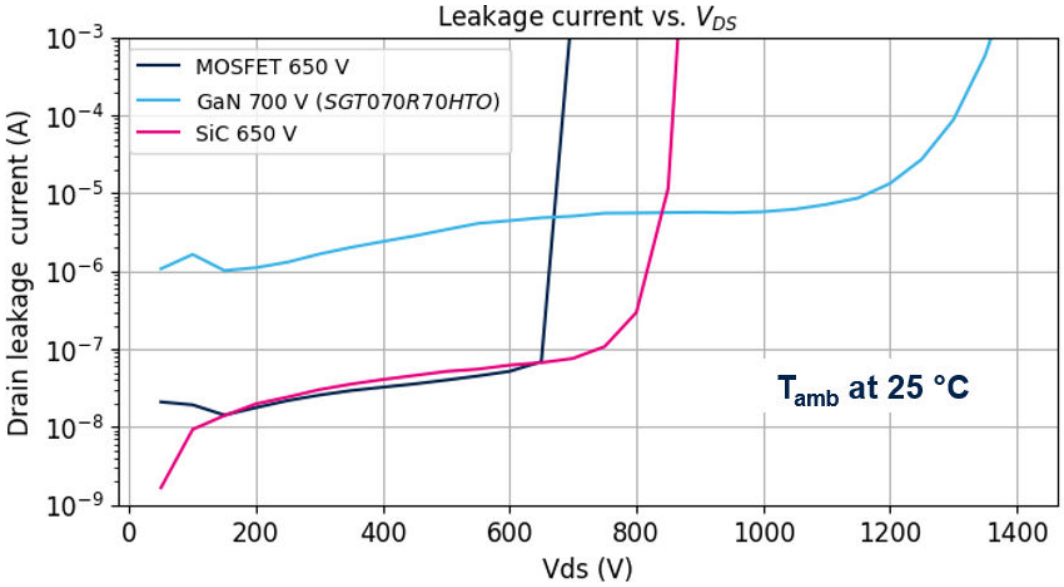
Avalanche breakdown in silicon MOSFETs occurs when the device is subjected to voltages exceeding its breakdown voltage, causing a controlled multiplication of carriers (electrons and holes) through impact ionization. The body diode and the bulk silicon structure allow the device to sustain avalanche current for short durations without immediate failure, which is a key ruggedness feature.

Figure 4. Overview of power transistor symbols



GaN devices have a much higher critical electric field (typically 3 MV/cm compared to 0.3 MV/cm for silicon), allowing higher breakdown voltages but with different failure modes (see Figure 5).

Figure 5. Drain leakage current for various technologies



When subjected to overvoltage, GaN transistors do not exhibit traditional avalanche behavior. Instead, the device can experience localized hot spots, and trapping effects leading to permanent damage if the voltage exceeds safe limits [3], [4].

The absence of a body diode (see Figure 4) means that there is no intrinsic path to safely conduct avalanche current, so the device is generally less tolerant to avalanche energy than silicon MOSFETs.

GaN HEMTs have been found to withstand the energy surge through capacitive charging, which often causes significant voltage overshoot near their catastrophic limit [5].

Designers must carefully manage voltage transients and overshoot to avoid damaging the GaN transistor, often using snubbers, clamps, or other protective elements.

GaN devices must be operated within their specified voltage and energy limits, as they do not inherently tolerate avalanche conditions like silicon MOSFETs.

1.3 Standardization efforts by JEDEC for GaN power devices

JEDEC is a global industry group that develops open standards for the microelectronics industry, focusing on reliability and quality of semiconductor devices. Within JEDEC, the JC-70 committee is dedicated to wide band-gap power semiconductor devices, including emerging technologies such as GaN transistors, where STMicroelectronics actively participates in writing guideline documents.

The *JC-70* committee has recently initiated a task group focused on establishing guidelines and standards for transient voltage characterization and the reliability of GaN power devices.

While JEDEC policy restricts the publication of work still under development, this task group's efforts build upon extensive background knowledge and ongoing research in the field. These contributions inform the creation of new standards on transient overvoltage ratings and reliability. These forthcoming guidelines aim to support the robust and reliable deployment of GaN transistors in power electronics applications [1].

Nevertheless, the standard unclamped inductive switching (UIS) test, as defined in the JEDEC document *JESD24-5* [6], provides a widely accepted methodology for evaluating the avalanche ruggedness and transient energy capability of power semiconductor devices.

2 Test methods

2.1 Drain step stress

This pseudo-static test is designed to evaluate the reliability of the DUT under progressively increasing stress conditions of rising voltage levels when it is in its **off** (non-conductive) state [4]. During the test, the voltage applied between the drain and the source (V_{DS}) is raised in discrete steps at specific intervals while the applied voltage and the leakage currents are monitored.

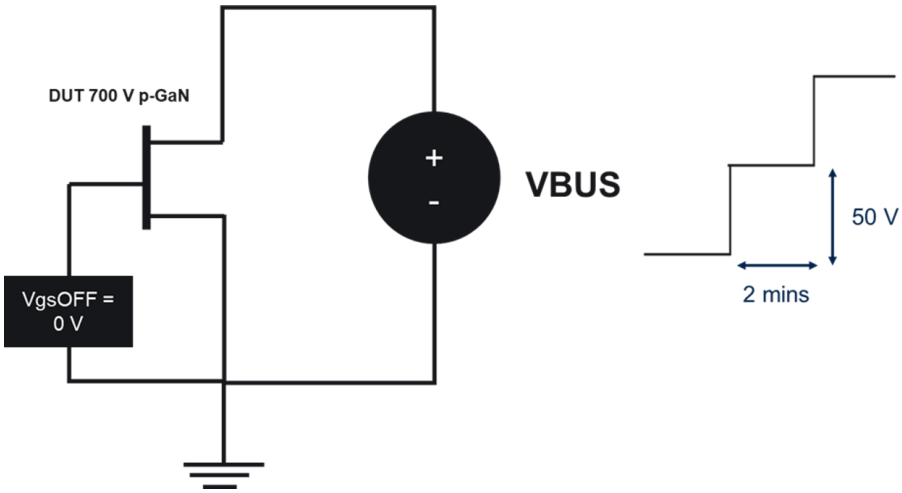
Throughout the test, the DUT's response to each stress level is continuously monitored to detect any signs of degradation or failure.

The voltage is increased every two minutes by 50 V steps at ambient temperature (~ 25 °C): The two-minutes intervals provide sufficient time for the DUT to stabilize electrically and thermally at each voltage level. This duration allows transient effects to settle and any early signs of degradation, such as increased leakage currents, to manifest clearly. The 50 V increases help identify the voltage threshold at which degradations begin in a controlled, measurable way.

Key signals to observe during the test include:

- **Drain-source current (I_{DS})**: As the off-state voltage increases, any rise in leakage current path between the drain and source, can be an early indicator of degradation mechanisms such as percolation paths creation [4], [7], [8]. Tracking leakage current helps detect subtle damage before catastrophic failure occurs, providing insight into the transistor's health and reliability
- **Gate-source current (I_{GS})**: Similar to I_{DS}, monitoring the leakage path between the drain and source is essential to differentiate damage in the drain-to-source path from the drain-to-gate path.
- **Drain-source voltage (V_{DS})**: Monitoring the applied voltage ensures that the stress levels are accurately controlled and increased as planned. It also helps detect any sudden voltage drops or irregularities that might indicate device failure. It also helps identify the exact voltage at which degradation or failure initiates.

Figure 6. The step stress setup schematic



The test is stopped when catalytic breakdown is reached or when the power supply compliance is reached (in this case, limited at 8 mA).

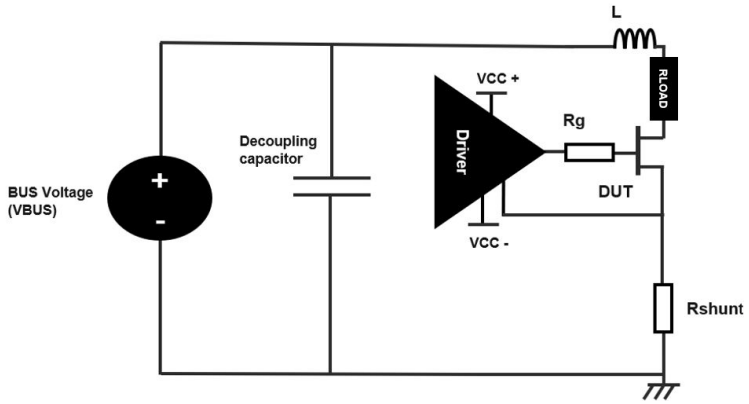
2.2 Unclamped inductive switching (UIS)

The unclamped inductive switching (UIS) rating has been a valuable parameter since it became common in MOSFET datasheets in the mid-1980s [9].

Also referred to as the avalanche energy rating, UIS ratings are standard specifications on silicon power MOSFET datasheets. Although UIS is not typically an application-driven attribute, devices are generally operated below their avalanche breakdown voltage. However, it remains critical for assessing device ruggedness [1].

The introduction of UIS and E_{AS} testing arose from early silicon power MOSFET generations to the destructive turn-on of a parasitic bipolar transistor embedded within the device structure. The UIS test setup, illustrated in Figure 7, involves triggering the device under test (DUT) with a gate pulse of defined duration while an inductor L is charged at a current ramp determined by VBUS/L, where VBUS is the BUS voltage. When the DUT switches-off, the energy stored in the inductor discharges through the device as avalanche current. During this process, the drain-source voltage rises to the device's breakdown voltage, dissipating significant energy [10].

Figure 7. The unclamped inductive switching schematic



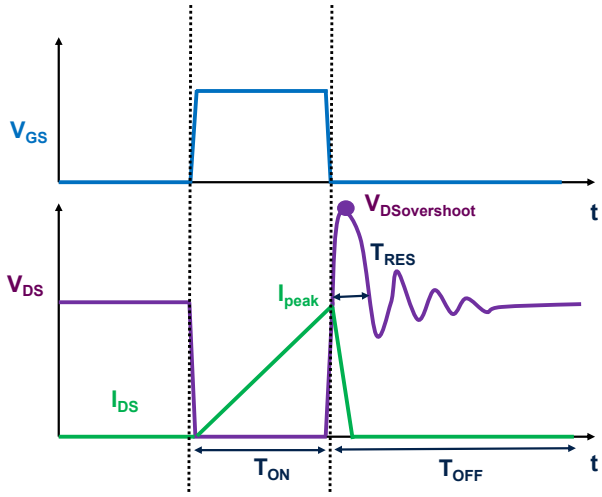
The avalanche energy E dissipated by the transistor is calculated by the formula:

$$E = \frac{1}{2}LI^2 \quad (1)$$

Where I is the peak current through the device.

A key aspect of UIS testing is that varying the inductance value allows control over the stress imposed on the DUT. Increasing the inductance reduces the peak current required to damage the transistor; however, this reduction in current does not offset the increase in inductance in the energy equation. Consequently, the avalanche energy increases even as the current decreases [10].

Figure 8. UIS measurement, voltage, and current waveforms



During the UIS test, the transistor is switched on to energize the inductor, then turned-off, causing the inductor current to continue flowing through the device as the voltage across the drain-source rises, potentially exceeding the breakdown voltage. The maximum surge voltage depends on the VBUS, the maximum peak current reached at the end of the T_{ON}, and the parasitic inductance of the power loop.

The duration of the surge during the resonance of the transistor is calculated using the following formula:

$$T_{RES} = \pi\sqrt{(L_{loop} \times C_{loop})} \quad (2)$$

Where T_{RES} is the duration of the resonance time, L_{loop} includes L_{stray} + L (inductance), and C_{Loop} corresponds to the C_{OSS} (DUT) + C_{PCB}.

The maximum voltage overshoot can be approximated by the energy balance between the inductive energy and the device capacitances.

A common simplified formula to estimate the maximum voltage overshoot is:

$$V_{DSovershoot} = VBUS + \sqrt{\left(\frac{2E}{C_{loop}}\right)} \quad (3)$$

Where E is the energy stored in the inductance before switching-off.

Key signals to observe during the test include:

- **Drain-source voltage (V_{DS})**: Monitored to capture the voltage overshoot and transient stress during the switching-off of the inductive load. It indicates the maximum voltage that the device can sustain.
- **Drain-source current (I_{DS})**: Measured to observe the inductive current flowing through the device at turn-off, which defines the energy the device must withstand.
- **Gate-source voltage (V_{GS})**: Controlled and monitored to ensure proper switching of the transistor and to observe any gate voltage transients that may affect device behavior.

For more information regarding the probing considerations for power GaN transistors you can refer to the application note AN5770 [11].

2.3 V_{DS} transient test

This test was designed to simulate real-world switching conditions where voltage surge occur, assessing the transistor's ability to withstand these stresses without failure. The test method evaluates the transient voltage robustness of the power transistor, often referred to as the V_{DS} transient test.

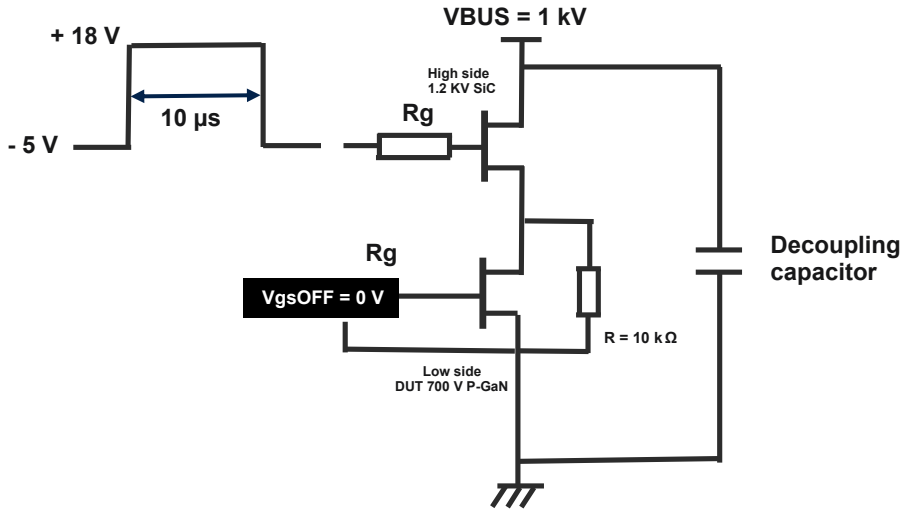
The DUT is indeed kept in the off state (gate voltage at 0 V), meaning it does not conduct current through its channel during the test pulse. The focus is on applying a controlled high-voltage transient across the drain-source terminals to evaluate the device's ability to withstand transient voltage stress without turning on or failing.

A separated high-side power transistor with a higher voltage rating than the DUT placed in low side is used to generate and apply the voltage pulse (typically with a pulse duration T_{pulse} > 1 µs) to the DUT's drain-source terminals. This transistor acts as a controlled voltage source, enabling precise application of the transient voltage waveform.

A resistor is placed in parallel with the DUT to provide a controlled discharge path for the device's output capacitance (C_{Loop}) during the voltage transient. This resistor helps to limit the voltage slew rate (dv/dt) during the capacitor discharge, preventing excessively fast voltage changes that could induce damaging voltage spikes or oscillations.

This methodology allows the characterization of the maximum transient voltage withstand capability and helps identify safe operating margins for surges in real applications.

Figure 9. The V_{DS} transient schematic



The V_{DS} transient test applies a high-voltage pulse to the device in the off state, subjecting it to rapid voltage stress across the drain-source terminals. This test stresses the device's intrinsic structures and interfaces in a way that shares similarities with ESD events, enabling detection of ESD-related weaknesses.

By applying a transient pulse with fast rise time to the device in the off-state, the V_{DS} transient test replicates critical aspects of ESD stress.

Fast voltage rise (dv/dt) mimics the fast transient voltage conditions of an ESD event, which can cause the failure of the device.

3 Performance of p-GaN transistors under overvoltage conditions

The following section presents the detailed test results obtained for the p-GaN transistor under overvoltage conditions, highlighting its transient and pseudostatic voltage robustness. All the test methods are specifically designed to evaluate the device until failure. The device under test is a commercially available 700 V p-GaN transistor with a typical on-resistance of 53 mΩ (Ref: SGT070R70HTO) [12].

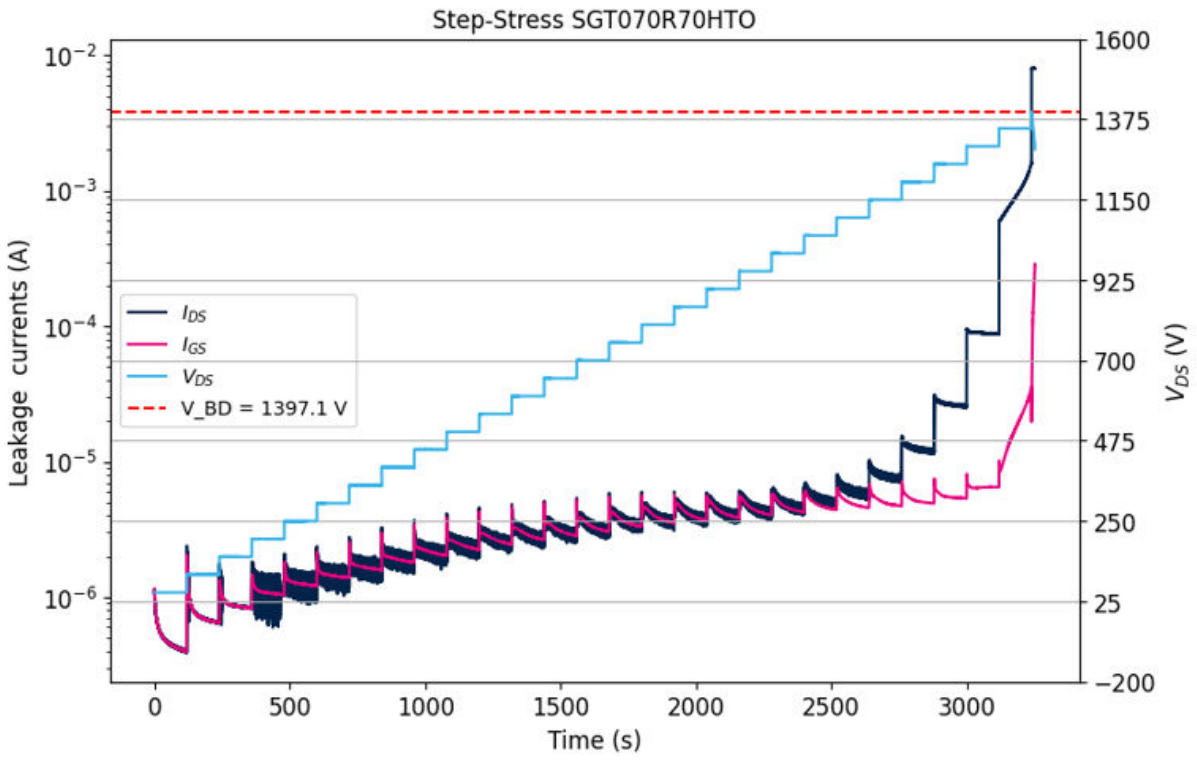
3.1 Drain step stress results

The drain step stress test was performed under the previously described conditions (see Section 2.3: V_{DS} transient test).

Under these conditions, the p-GaN transistor withstood a 1300 V two-minute step applied between its drain and source terminals (see Figure 10), almost twice its nominal rating of 700 V, without significant leakage. The test was stopped before the catalytic breakdown of the DUT at the power supply compliance. Posttest characterization confirmed that the DUT remained fully functional, demonstrating excellent static voltage robustness.

We can observe from the 1350 V step, an increase in leakage current due to the accumulation of charges creating current filaments. The test allows us to pinpoint the breakdown voltage in static conditions to over 1400 V.

Figure 10. Measured drain step stress waveforms



This drain step stress test is easy to implement, only requiring a single high-voltage DC power supply with the voltage applied across DUT's drain-source terminals. In contrast, traditional silicon MOSFET devices are unable to reach voltages greater than their ratings due to the phenomenon of avalanche occurring.

These results highlight again the better ruggedness to drain voltage of p-GaN transistors, making them well suited for applications involving high-voltages stress.

3.2 UIS (single pulse) results

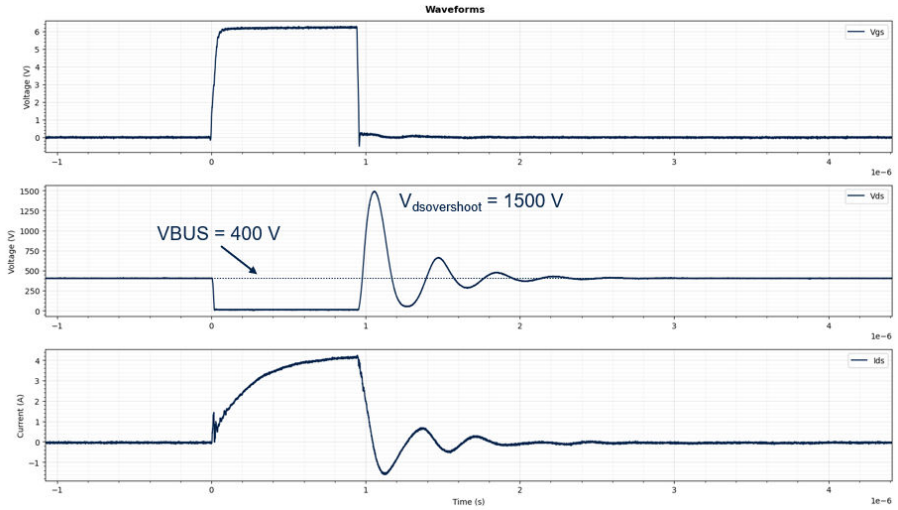
Two distinct test configurations were employed to comprehensively evaluate the transient behavior of the p-GaN transistor at room temperature under different inductive switching conditions.

The first configuration featured a higher inductance of L = 22 µH combined with a load resistor in series of 100 Ω to simulate more realistic operating conditions. The pulse on duration was reduced to 1 µs, and the bus voltage was increased progressively up to 450 V in this case.

The second configuration utilized a low inductance of L = 1 µH with no load resistor (R_{load}), enabling fast switching events. During this test, the drain-source voltage, gate-source voltage, and drain current signals were continuously monitored. The pulse on duration was set to 2.5 µs, while the bus voltage was varied from 5 V up to 17.5 V, limited by the low inductance value to avoid excessive current.

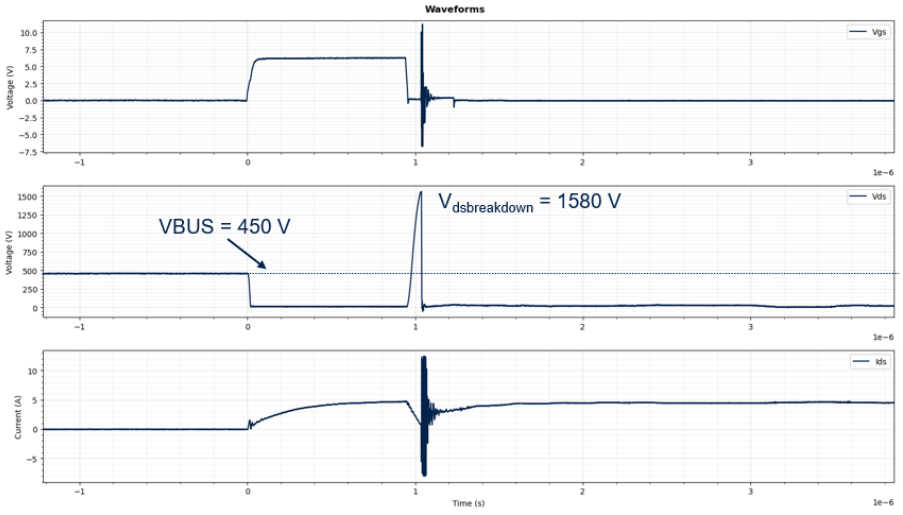
Figure 11 shows the waveforms recorded during the UIS characterization of a p-GaN transistor. During the switching transition from the on to off-state, a voltage overshoot can occur between the drain and source terminals due to the parasitic inductances present in the circuit. This inductive effect generates a transient voltage spike, causing the drain-source voltage to exceed the device's maximum rated V_{DS} specified in the datasheet under the given test conditions.

Figure 11. Measured UIS waveforms in normal operation - single pulse in config 1



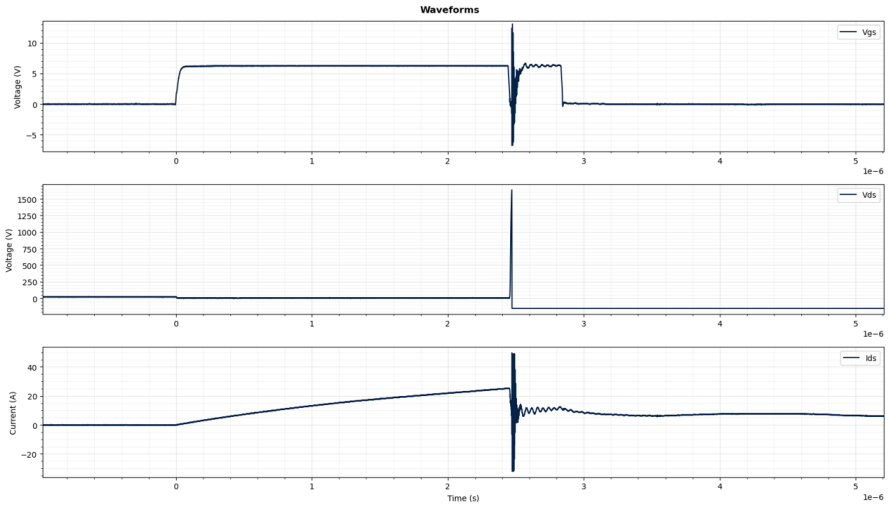
The UIS characterization (config 1) of the p-GaN transistor demonstrated impressive robustness, with device failure occurring only when the V_{DS} reached 1580 V, more than twice its nominal 700 V rating (see Figure 12).

Figure 12. Measured UIS waveforms in failure operation - single pulse in config 1



For config 2, the maximum voltage withstand was very close to approximately 1620 V (see Figure 13), confirming consistent transient voltage capability across different test conditions.

Figure 13. Measured UIS waveforms in failure operation - single pulse in config 2



These results underscore the remarkable transient voltage of p-GaN transistors and provide valuable insights for designers considering these technologies for high-performance power applications [12]. More than, it can be observed that V_{BUS} does not significantly impact the results, rather the voltage overshoot is the critical factor.

MOSFET and SiC transistors rely on a p-n junction that can fail under high electric fields. In such conditions, electrons impact the material structure, causing the temperature to increase, which can lead to the destruction of the device. This is why datasheets specify maximum values for avalanche energy (E_{AS}) and avalanche current (I_{AS}). In contrast, GaN devices behave differently. Their failure mechanism is more related to the limitation of the material's critical electric field [2].

Regarding the other technologies, silicon carbide (SiC) transistors typically clamp at higher voltages (~1000 V for a 650 V product) during UIS tests compared to silicon MOSFETs (~700 V for a 650 V product) due to several intrinsic material and device structure properties. SiC has a wider bandgap (~3.3 eV) and a much higher critical electric field (~2-3 MV/cm) than silicon (~0.3 MV/cm). This allows SiC devices to sustain higher voltages before an avalanche or breakdown occurs [10].

SiC MOSFETs, like their silicon counterparts, have an intrinsic body diode formed by the parasitic p-n junction between the body (p-type region) and the drift region (n-type).

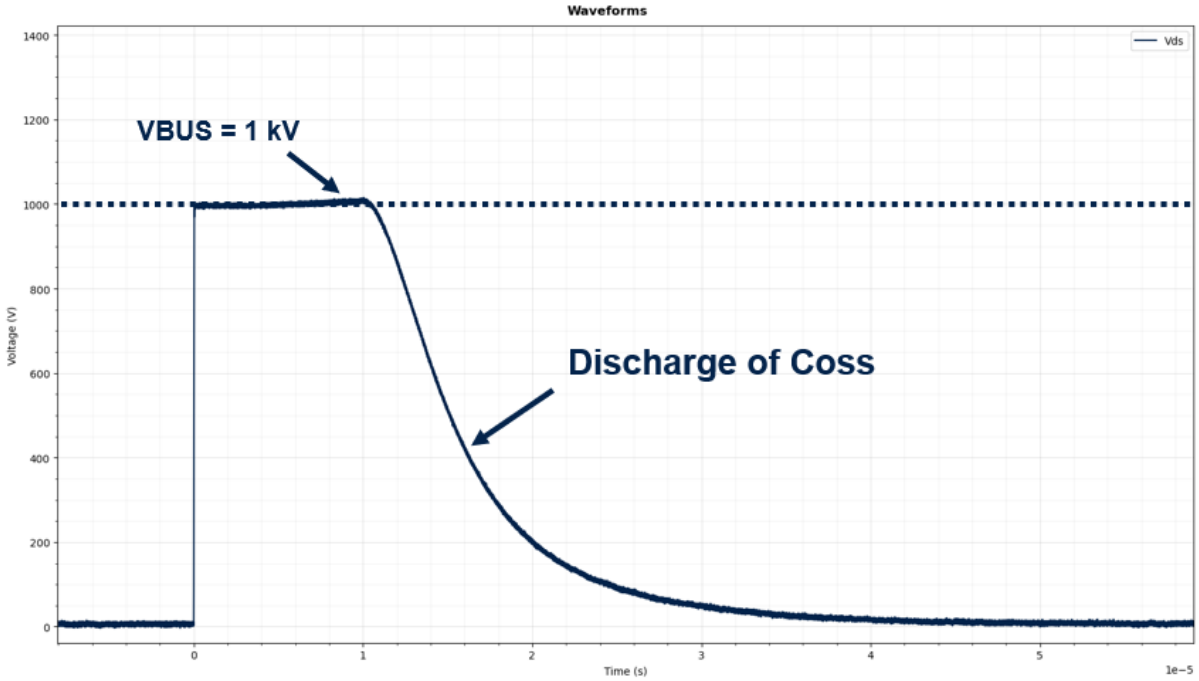
In essence, the SiC transistor's higher clamping voltage during UIS is a consequence of its intrinsic body diode and avalanche capability, combined with the superior material properties of SiC. This contrasts with p-GaN transistors, which lack a body diode and avalanche region, resulting in different transient voltage behavior.

3.3 V_{DS} transient (single pulse) results

The V_{DS} transient test was conducted under the following conditions: a T_{pulse} of 10 µs, a bus voltage of 1 kV, and a high-side transistor capable of sustaining the surge a 1200 V SiC device. The gate voltage during the test was held at 0 V, ensuring the device under test (DUT) remained in the off-state.

Under these conditions, the p-GaN transistor successfully withstood the 1 kV transient surge applied between its drain and source terminals without any damage (see Figure 14). Post-test characterization confirmed that the DUT remained fully functional, demonstrating excellent transient voltage robustness.

Figure 14. Measured VDS transient waveforms in normal operation - single pulse



This V_{DS} transient test is straightforward and efficient to implement, requiring only a single high-voltage pulse applied across the DUT's drain-source terminals. In contrast, traditional silicon MOSFET devices would be unable to survive such a surge without failure, as the applied voltage significantly exceeds their maximum rated limits. The resulting localized high electric fields in MOSFETs can cause premature breakdown and irreversible damage.

These results highlight the superior transient voltage endurance of p-GaN transistors, making them well suited for applications involving high-voltage switching stress.

4 Conclusion

This application note examines the voltage behavior and robustness of p-GaN transistors under overvoltage and transient voltage conditions commonly encountered in power electronics applications. By leveraging the advantages of GaN technology such as high critical electric field, fast switching capability, and normally-off operation enabled by the p-GaN gate structure, these devices demonstrate interesting performance.

Table 1. Static and dynamic results overview - SGT070R70HTO

Breakdown voltage	$V_{withstanding}$	Datasheet reference	dV/dt	Stress time	Test
1620 V	< 1620 V	$V_{DS(TR)}$	~ 130 V/ns	40 ns → T_{RES}	**UIS configuration 2**
1580 V	<1580 V		~ 20 V/ns	180 ns → T_{RES}	**UIS configuration 1**
Not available	= 1000 V		~ 40 V/ns	10 µs → T_{PULSE}	**V_{DS} transient**
1400 V	= 1300 V	V_{DS} max. rating	~ 50 V/s	2 min → T_{STATIC}	**Drain step stress**

The document describes key test methodologies, including unclamped inductive switching (UIS), drain step stress, and V_{DS} transient testing, designed to evaluate device endurance under drain high-voltage transient stress. It highlights the importance of proper test configurations and the measurement of critical signals to accurately characterize device behavior.

A comparison with silicon MOSFET and SiC technologies emphasizes the fundamental differences in device structure and avalanche capability, explaining the unique transient response of p-GaN transistors. The absence of an intrinsic body diode and avalanche behavior in p-GaN devices necessitates careful design and protection strategies. However, it also enables exceptional transient voltage tolerance when properly managed.

5 References

Table 2. Reference name and description

Ref. name	Document name	Document links
[1]	**T. McDonald** and **S. W. Butler**, "*Progress and Current Topics of JEDEC JC-70.1 Power GaN Device Quality and Reliability Standards Activity: Or: What is the Avalanche capability of your GaN Transistor?*", 2021.	9405225
[2]	**R. Zhang**, "*Overvoltage Ruggedness and Dynamic Breakdown Voltage of P-Gate GaN HEMTs in High-Frequency Switching up to Megahertz*" presented at the *2022 IEEE Applied Power Electronics Conference and Exposition (APEC), IEEE*, 2022.	9773713
[3]	**R. Zhang** and **Y. Zhang**, "*Overvoltage Robustness of p-Gate GaN HEMTs in High Frequency Switching up to Megahertz*", *IEEE Trans. POWER Electron, vol. 38, no. 5*, 2023	
[4]	**C. Crouard**, **J. Godillon**, **J.-F. Pieprzyk**, and **P. Tounsi**, "*Study of temperature-dependent breakdown in AlGaN/GaN normally-off HEMTs under drain step-stress*", 2025.	
[5]	**J. P. Kozak**, **Q. Song**, **R. Zhang**, **J. Liu**, and **Y. Zhang**, "*Robustness of GaN Gate Injection Transistors under Repetitive Surge Energy and Overvoltage*" in 2021, *IEEE International Reliability Physics Symposium (IRPS), Mar. 2021, pp. 1–5. doi: 10.1109/IRPS46558.*	9405173
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Revision history

Table 3. **Document revision history**

Date	Revision	Changes
18-Nov-2025	1	Initial release.
28-Nov-2025	2	Updated Figure 4.

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