AN6373

Application note

Guidelines for enabling embedded SMPS on STM32WBA MCUs

Introduction

The STM32WBA series integrates a switched-mode power supply (SMPS) to optimize power consumption. This application note provides key information about the implementation of the SMPS.

A significant portion of this document adopts a general approach to step-down converters.

1 General information

This document applies to the STM32WBA Arm® Cortex®-M33-based microcontrollers.

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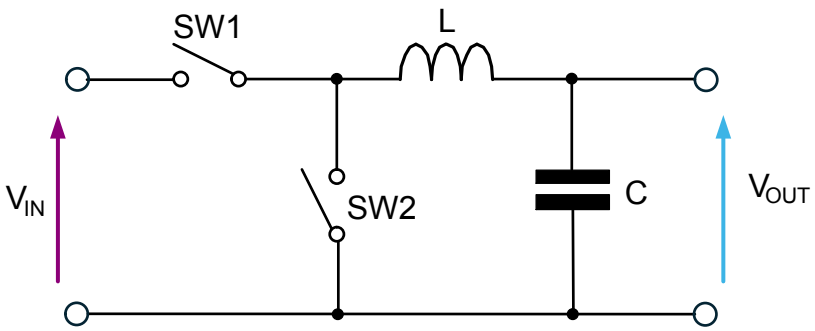
2 Step-down converter introduction

2.1 Type of converter

The SMPS embedded in STM32WB series are step-down converters (buck converters). When the power supply and input voltage exceed internal requirements, the converter reduces energy consumption. Without the SMPS, the conversion is performed by dissipating energy through the internal LDO.

This type of converter is common. The block diagram below shows a simplified view of the conversion process. The input voltage is switched through a coil, and a capacitor smooths the signal.

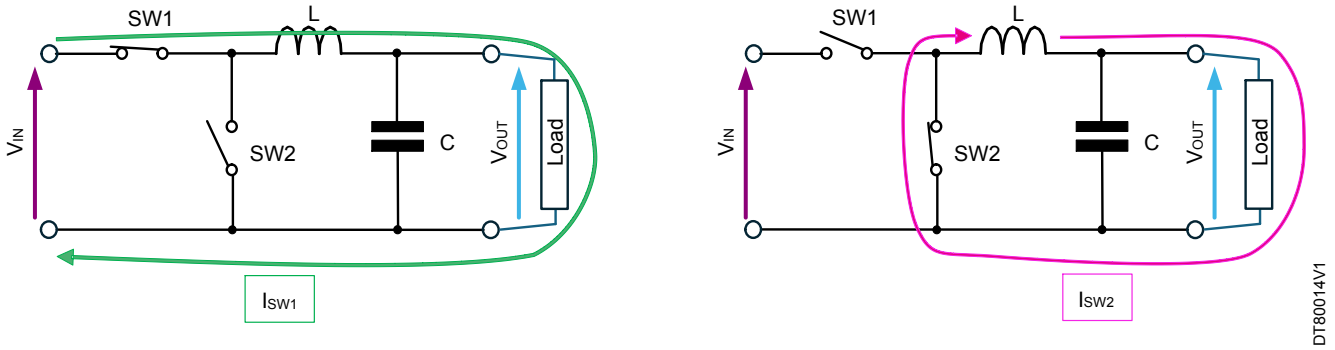
Figure 1. Block diagram of the step-down converter



2.2 Operating

The conversion is performed in two phases: SW1 = closed/SW2 = open and SW1 = open/SW2 = closed. Both switches are never closed simultaneously. The operation of the switches is controlled by a sequence that depends on the type of modulation, the output current, and the output voltage.The figures below illustrate the current paths during the sequences.

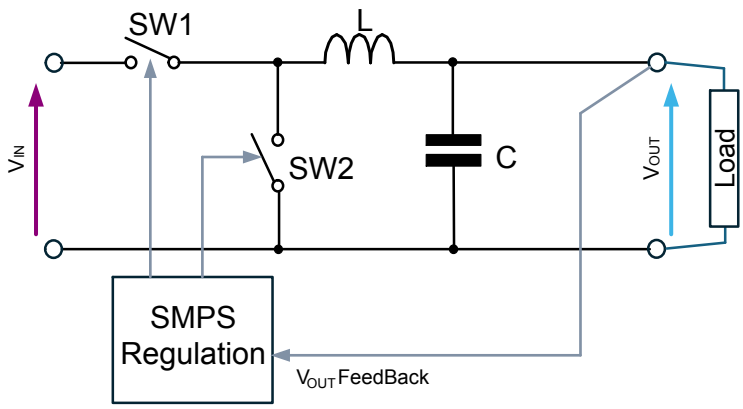
Figure 2. Current path during both switching phases



2.3 Voltage control

In the previous section, we examined the current study during operation. The goal of the conversion is to deliver a supply voltage to V_{OUT}. For a step-down converter, V_{OUT} is lower than V_{IN}. This output voltage is controlled by the regulation stage included in the DC-DC converter. To achieve this, the output voltage is sensed by the regulation stage, which adjusts the duty cycle (PWM) or the pulse frequency (PFM).

Figure 3. **Block diagram with voltage feedback**



Due to the switched system, a ripple naturally appears. The capacitor connected after the coil reduces this ripple to an acceptable value.

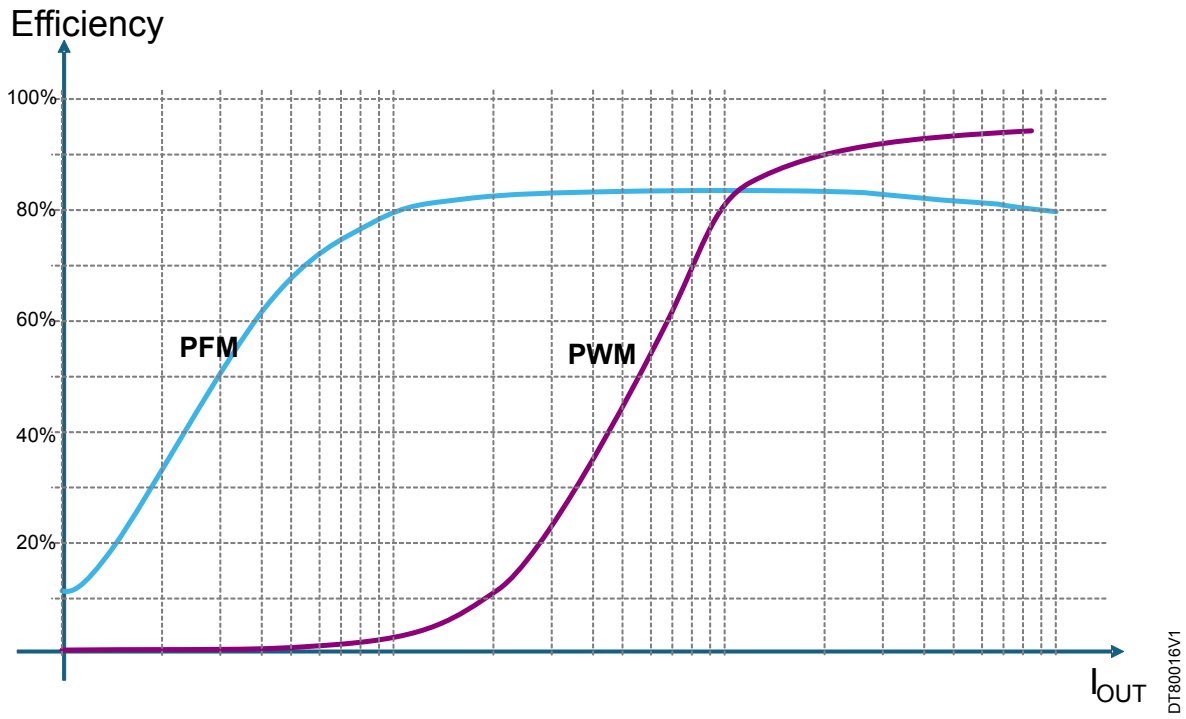
2.4 Types of modulations

There are two methods to control the switches. They can be controlled by PWM (pulse-width modulation) or PFM (pulse-frequency modulation).

PWM control uses a fixed frequency, and the duty cycle changes. PFM control always uses the same pulse size, but the time between each pulse changes.

PFM control is more efficient for low current but generates more noise than PWM control. Therefore, the selection between the two control methods is a compromise and depends on the mode selected for the load (low power or high performance).

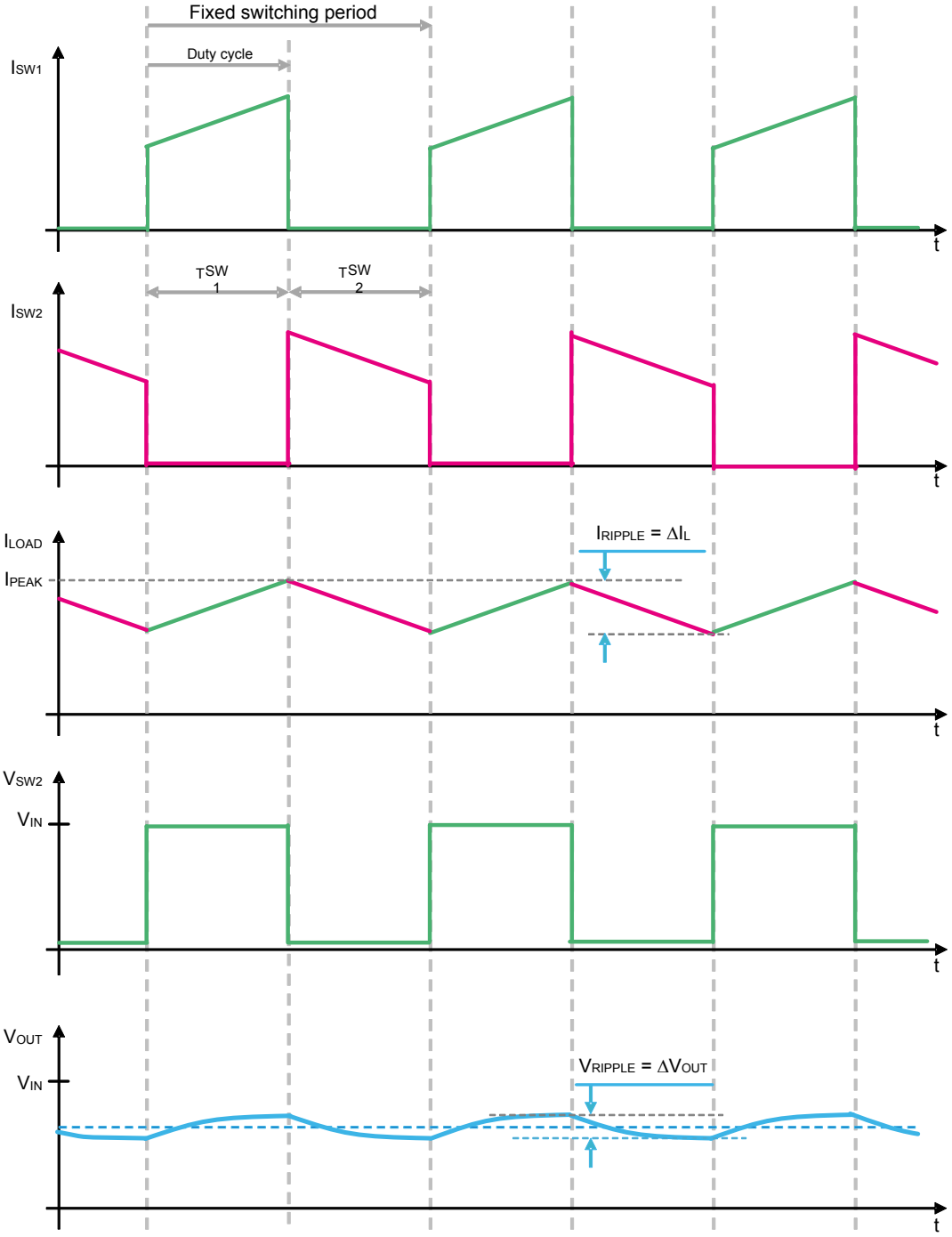
Figure 4. **Typical curve of efficiency versus I_{OUT} (PFM and PWM)**



2.4.1 PWM sequence

The PWM sequence uses a fixed frequency, and the duty cycle changes to control the required energy. The figure below illustrates both steps of the sequence and the result observed by the load. Most of the time, PWM control is used in continuous operation, where the output current does not drop to zero.

Figure 5. Timing of currents with PWM mode in continuous operation



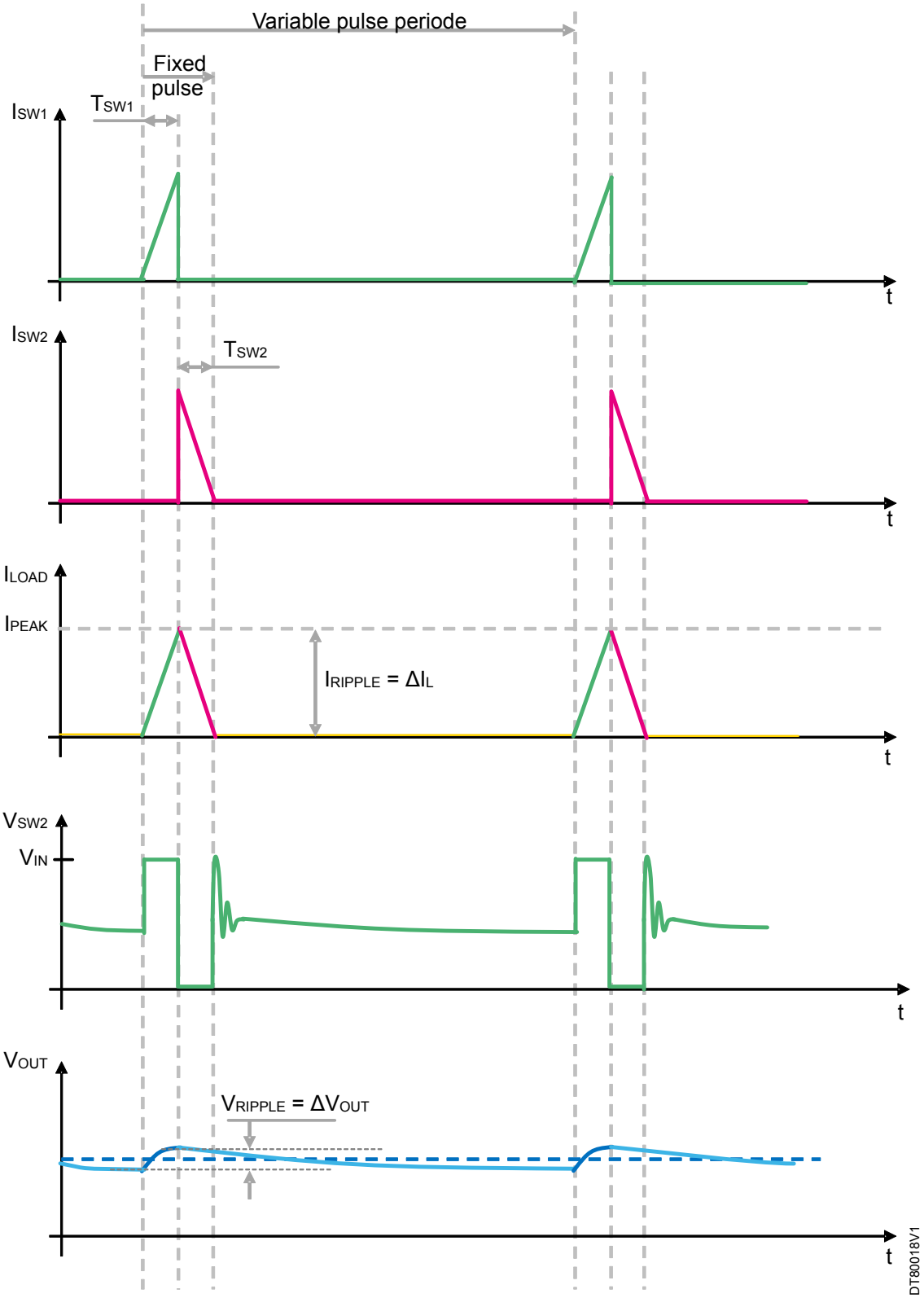
Where:

- T_{SW1} is the time during which SW1 is closed (SW2 is open).
- T_{SW2} is the time during which SW2 is closed (SW1 is open).
- $T_{SW1} + T_{SW2}$ = switching period = $1/F_{SW}$

2.4.2 PFM sequence

The PFM sequence uses a fixed pulse size and adjusts the frequency of pulses to control the required energy quantity. The current can be managed in several modes: continuous, discontinuous, or both (continuous and discontinuous). For the STM32WBA series, only the discontinuous mode is used. The figure below illustrates both steps of the sequence and the result observed by the load.

Figure 6. Timing of the currents with PFM mode (discontinuous operation mode)



Where:

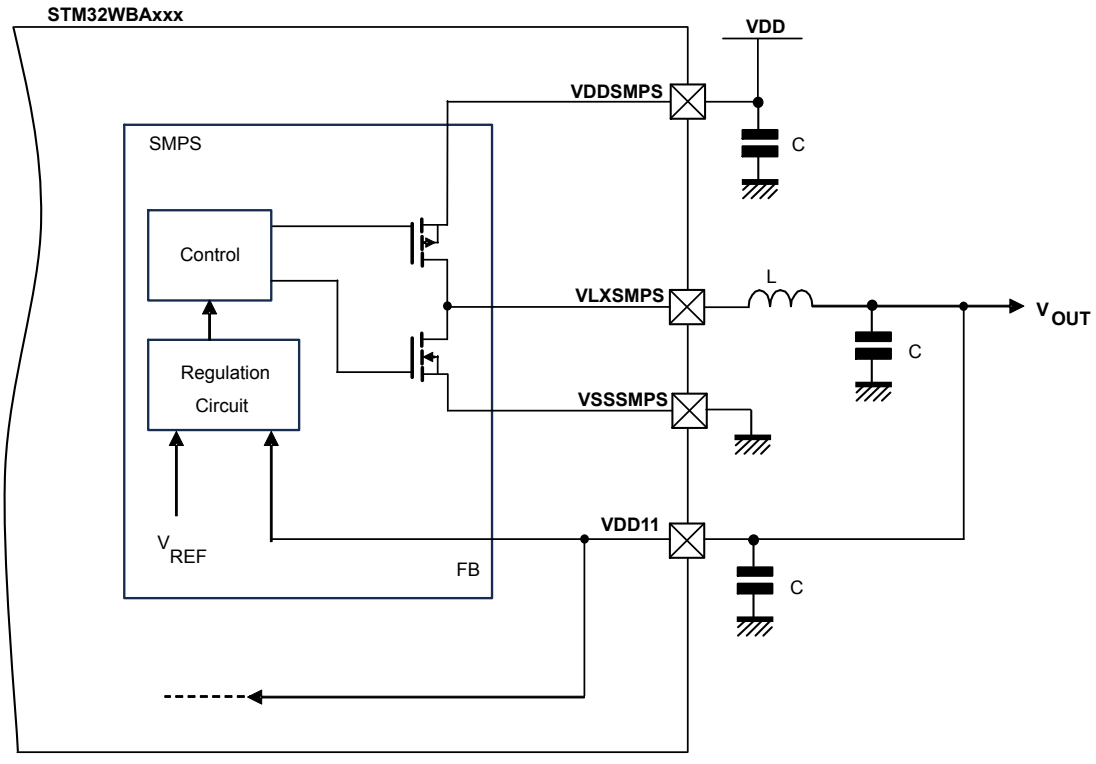
- T_{SW1} is the time during which SW1 is closed (SW2 is open).
- T_{SW2} is the time during which SW2 is closed (SW1 is open).

3 SMPS embedded on STM32WBA series

3.1 SMPS bloc diagram

As described in the general overview, this type of converter requires two switches to operate. The SMPS embedded in the STM32WBA series uses the same architecture. Both switches are replaced by two MOS transistors.

Figure 7. STM32WBA series SMPS simplified block diagram



The SMPS function included in the STM32WBA series has dedicated pins for the supply (VDDSMPS) and the ground (VSSSMPS). The primary purpose is to reduce access resistance and isolate the SMPS from the rest of the chip to address noise concerns.

The VOUT feedback is internally connected to the VDD11 pin. Within the chip, this same VDD11 pin primarily supplies a significant portion of the circuit, benefiting from the SMPS power conversion.

3.2 Specifications of STM32WBA series SMPS

The SMPS embedded in the STM32WBA series is designed to optimize power consumption across all available modes. Depending on the consumption strategy and V_{DD} voltage value, it is possible to disable the SMPS and switch between SMPS and LDO modes dynamically. This change can be implemented using the same schematic and controlled through firmware.

The STM32WBA5xxx/WBA6xxx supports both types of sequences: PWM and PFM. PFM is used for low-power modes, and an automatic switch between PFM and PWM methods is employed in high-power modes.

The supply voltage of the SMPS is the same as other parts of the SoC: 1.7 V < VDDSMPS < 3.6 V.

- High-side P-channel MOS transistor (SW1): R_{DSON} = 160 mΩ
- Low-side MOS transistor (SW2): R_{DSON} = 180 mΩ

For PWM sequences, the frequency of the switch control can have two values:

- FSW = 1.50 MHz if V_{DD} is lower than 1.9 V

- FSW = 3.00 MHz if V_{DD} is higher than 1.9 V

For PFM sequences, the ripple current is fixed for each power mode. The internal circuitry always drives the same ripple current value for each power mode. As shown above, the ripple current is equal to the peak current on the coil ($\Delta I_L = I_{L\_PEAK}$).

Several output voltage values are fixed internally. These values depend on the mode used. Table 1 summarizes the different modes available and the corresponding output voltage values, along with the maximum peak current on the coil.

Table 1. Output voltage and maximum output current by power mode

Mode	STM32WBA5xxx and STM32WBA6xxx		
	V_{OUT}	I_{L_PEAK}	Sequence
STOP 3	0.68 V	150 mA	PFM
STOP 1 and STOP 2	0.9 V	180 mA	PFM
RUN 2	0.9 V	180 mA	PFM
RUN 1	1.2 V	I_{LOAD} +50 mA	PFM/PWM
RUN 0	-	-	-

Important: The information listed above is necessary to understand how the SMPS embedded in the STM32WBA series operates. All these values are typical values. It is important to verify the complete specifications in the product datasheet.

4 Selection of the external components

In the case of the SMPS embedded inside the STM32WBA5xxx/WBA6xxx, the converter automatically switches between the PWM and PFM sequences, and the low-power modes depending on the current requested and the V_{IN} voltage level.

4.1 Selection of coil

The SMPS is designed around a coil value of 2.2 µH. The stability of this SMPS is not guaranteed for other values.

4.1.1 PFM sequence

For all power management modes (see Table 1), the output voltage and the maximum output current are known. To optimize the quiescent current, as well as the complexity and size of the SMPS IP, only one coil value is used. This approach limits the stability compensation to this specific value.

Below are the specifications for the coil to be used:

- The required coil value for the STM32WBA series is 2.2 µH ±20%.
- The DC resistance (RDC) must be lower than 500 mΩ.
- The operating current must exceed 200 mA.
- The saturation current (I_{PEAK}) must exceed 800 mA.

Example of compatible part:

- Manufacturer: MURATA
- Part numbers: LQM21PN2R2MGS, LQM21PN2R2MGE, or LQM21PN2R2MGH

4.1.2 PWM sequency

The coil value used for PFM sequencing is also used for PWM sequencing. The stability of the SMPS in PWM sequencing is also guaranteed by the design of this coil value.

For general knowledge, this value can be verified with PWM sequencing. To calculate the inductance value (coil) in a DC-DC step-down converter (or buck converter), several circuit parameters and desired performance characteristics must be considered.

The inductance L*L* is generally calculated to control the ripple current in the inductor ΔI_L. The standard formula is:

$$\Delta I_L = \frac{V_{OUT} \times \left(1 - \frac{V_{OUT}}{V_{DD}}\right)}{F_{SW} \times L}$$

Where:

- ΔI_L: Current ripple in the inductor.
- V_{DD}: Input voltage.
- V_{OUT}: Output voltage.
- F_{SW}: Switching frequency.
- L: Value of the coil (2.2 µH for STM32WBA series).

This formula can be simplified as:

$$\Delta I_L = \frac{V_{DD} \times D \times (1 - D)}{F_{SW} \times L}$$

Where:

$$D = \frac{V_{OUT}}{V_{DD}}$$

Note: Ensure that the peak current does not exceed the saturation current of the coil. The peak current is calculated as:

$$I_{PEAK} = I_{OUT} + \frac{\Delta I_L}{2}$$

4.2 Selection of input capacitor

The input capacitor must be 10 µF (±20%) with low ESR. An MLL capacitor is ideal, with ESR < 50 mΩ. Ensure that the selected capacitor has minimal DC bias drift, which is generally related to the rated voltage. It is recommended to choose a capacitor rated for 10 V or higher. This capacitor ensures that the SMPS has the necessary energy to operate in all modes and sequences.

Example of a compatible part:

- Manufacturer: Murata
- Part number: GRM188C81A106MA73

4.3 Selection of output capacitor

4.3.1 PFM sequency

Like the coil, the output capacitor is fixed by design. The value cannot be modified as it guarantees the stability of the SMPS.

The value of C_{OUT} must be 4.7 µF (±20%), and its ESR must be lower than 50 mΩ.

Example of a compatible part:

- Manufacturer: Murata
- Part Number: GRM155R60J475ME47D

4.3.2 PWM sequency

The output capacitor of a step-down converter is primarily used to filter the voltage ripple caused by the current ripple in the inductor. Its value depends on the following factors:

- The acceptable voltage ripple.
- The current ripple in the inductor.
- The switching frequency.

The output voltage ripple can be calculated using the following formula:

$$\Delta V_{OUT} = \frac{\Delta I_L}{8 \times F_{SW} \times C_{OUT}}$$

Where:

- ΔI_L = current ripple in the inductor (calculated or assumed).
- F_{SW} = switching frequency.
- ΔV_{OUT} = output voltage ripple (≤ 5 mV typical).

In practice, this capacitor is tested and simulated over a larger range to account for ESR and tolerances. Use several low-ESR ceramic capacitors in parallel for better performance. Pay attention to the capacitor's ESR, as it can also generate ripple:

$$\Delta V_{ESR} = \Delta I_L \times ESR_C$$

Ceramic MLL capacitors are good candidates because they naturally offer low ESR. However, in some cases, it is possible to further reduce the ESR value by connecting several capacitors in parallel. Ensure that the global tolerance value remains within the acceptable range (the total value should stay within 4.7 µF ±20%).

An example of a compatible part is the same as for PFM sequence:

- **Manufacturer**: Murata.
- **Part Number**: GRM155R60J475ME47D.

5 Efficiency estimation with PWM and PFM sequency

To calculate the efficiency of a buck converter based on parameters such as current, inductance value, and capacitance, it is necessary to understand how these components influence losses in the circuit. The following methodology estimates efficiency by considering these elements.

The efficiency is the ratio between the output power and the input power:

$$\eta = \frac{P_{OUT}}{P_{IN}} \times 100$$

$$P_{IN} = P_{OUT} + \Sigma_{LOSS}$$

Where:

- Σ_{LOSS}: Sum of losses.

Losses in all components, including the inductor, capacitor, and internal parts of the STM32WBAxxxx, must be considered to estimate efficiency.

5.1 Losses in the inductor

The inductance contributes to resistive losses due to its equivalent series resistance (ESR or R_{DC}), denoted as R_L.

These losses are calculated as follows:

$$Loss_L = {I_{RMS}}^2 \times R_L$$

The RMS current inside the coil is:

$$I_{RMS} = \sqrt{{I_{OUT}}^2 + \frac{{\Delta I_L}^2}{12}}$$

For PFM sequences, the current ripple is fixed for each power mode (see Table 1).

For PWM sequences, the equation for the current ripple is:

$$\Delta I_L = \frac{V_{IN} \times D \times (1 - D)}{F_{SW} \times L}$$

Where:

- F_{SW} is the switching frequency.
- D is the duty cycle.
- L is the inductance value.

5.2 Losses in the capacitor

The capacitor is also responsible for resistive losses due to its equivalent series resistance (ESR).

These losses are given by:

$$Loss_C = {\Delta I_C}^2 \times ESR_C$$

The ripple current on the capacitor (ΔI_C) is approximately equal to the ripple current on the inductor (ΔI_L).

As mentioned earlier, ceramic MLL capacitors are good candidates as they naturally offer a low ESR. This capacitor technology significantly reduces losses.

5.3 Losses in the STM32WBA series microcontrollers

The internal components of the STM32WBA series microcontrollers contribute to losses. These losses originate from MOS transistors and parasitic components:

$$Loss_{STM32WBA} = Loss_{RMOS} + Loss_{RPCK} + Loss_{SW} + Loss_{Q}$$

Where:

- $Loss_{RMOS}$: conduction loss in power MOS.
- $Loss_{RPCK}$: conduction loss in the package.
- $Loss_{SW}$: switching loss.
- $Loss_{Q}$: SMPS control loop consumption.

5.3.1 Conduction losses in the MOS transistors and in the package

The architecture and technology of the MOS transistors (high side and low side) significantly contribute to efficiency. For the STM32WBA series, this aspect is carefully considered. The MOS transistors are designed to ensure the expected performance.

The R_{DSON} parameter is used to calculate the losses, referred to here as RMOS.

For the MOS transistors used in the SMPS of STM32WBA series, RMOS = 160 mΩ for both high-side and low-side transistors.

RPKG represents the resistance of the access pin to the die inside the package. For QFN packages, this is primarily the resistance of the bonding. For other packages, it includes the resistance and the redistribution of the ball on the die. To simplify, the worst-case scenario is used for efficiency estimation. For all STM32WBAxxx devices, RPKG = 120 mΩ.

For the PWM sequence:

$$Loss_{RMOS} + Loss_{RPKG} = (RMOS + RPKG) \times {I_{RMS}}^2$$

For the PFM sequence:

$$Loss_{RMOS} + Loss_{RPKG} = F_{SW} \times (RMOS + RPKG) \times {I_{RMS}}^2$$

Where:

$${I_{RMS}}^2 = \frac{I_{PEAK}}{\sqrt{3}}$$

$$F_{SW} = \frac{2 \times I_{LOAD} \times V_{OUT} \times (V_{DD} - V_{OUT})}{V_{DD} \times L \times {I_{PEAK}}^2}$$

5.3.2 Switching losses

$$Loss_{SW} = C_P \times {V_{DD}}^2 \times F_{SW}$$

Where:

Cp ≈ 100 pF (parasitic capacitor)

F_{SW} switching frequency

For PWM:

F_{SW} = 3 MHz if V_{DD} ≥ 1.9 V

or

F_{SW} = 1.5 MHz if V_{DD} < 1.9 V

For PFM: F_{SW} depends on load and on V_{DD}

$$F_{SW} = \frac{2 \times I_{LOAD} \times V_{OUT} \times (V_{DD} - V_{OUT})}{V_{DD} \times L \times {I_{PEAK}}^2}$$

5.3.3 SMPS control loop consumption

Even if the currents are small, when estimating efficiency, it is necessary to account for the quiescent current of the SMPS control loop in the losses.

$$Loss_Q = V_{DD} \times I_Q$$

Table 2. I_Q versus STM32WBA version and power mode

Power mode	Quiescent current (I_Q)
	STM32WBA5xxx and STM32WBA6xxx
Run 1	420 µA
Run 2	2.5 µA
Stop 1	100 nA
Stop 3	100 nA

6 Other recommended or optional components

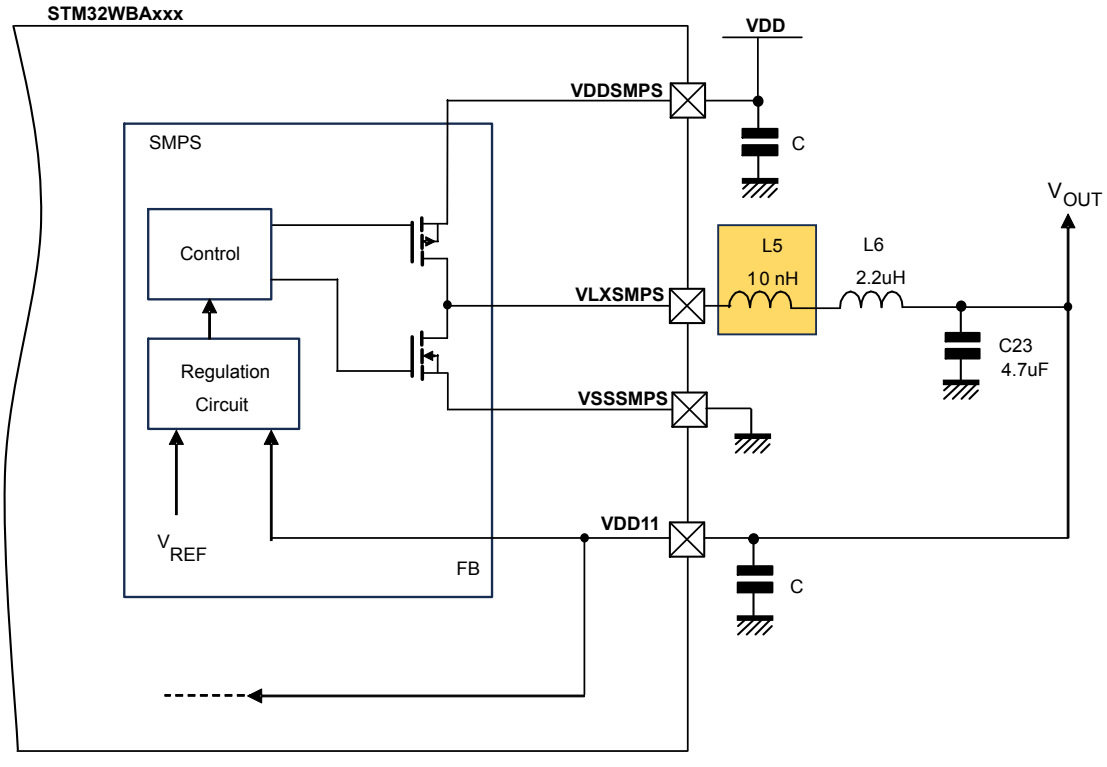
6.1 Noise reduction for RF stage

On the different reference designs (ST-DES) or the NUCLEO boards, there is a small coil, L5, with a value of 10 nH in series with the SMPS coil. It is used to reduce conductive and radiated noise to the RF stage of the circuit.

The value is fixed at 10 nH due to its low value compared to the SMPS coil value.

It is important to ensure that the maximum current rating of this coil is not exceeded. The coil used on the ST boards is the LQG15HS10NJ02D from Murata (10 nH, I_{MAX} = 500 mA, R_{DC} = 0.26 Ω).

Figure 8. Add-on RF coil to reduce RF noise



6.2 Limitation of SMPS switching noise on VDD

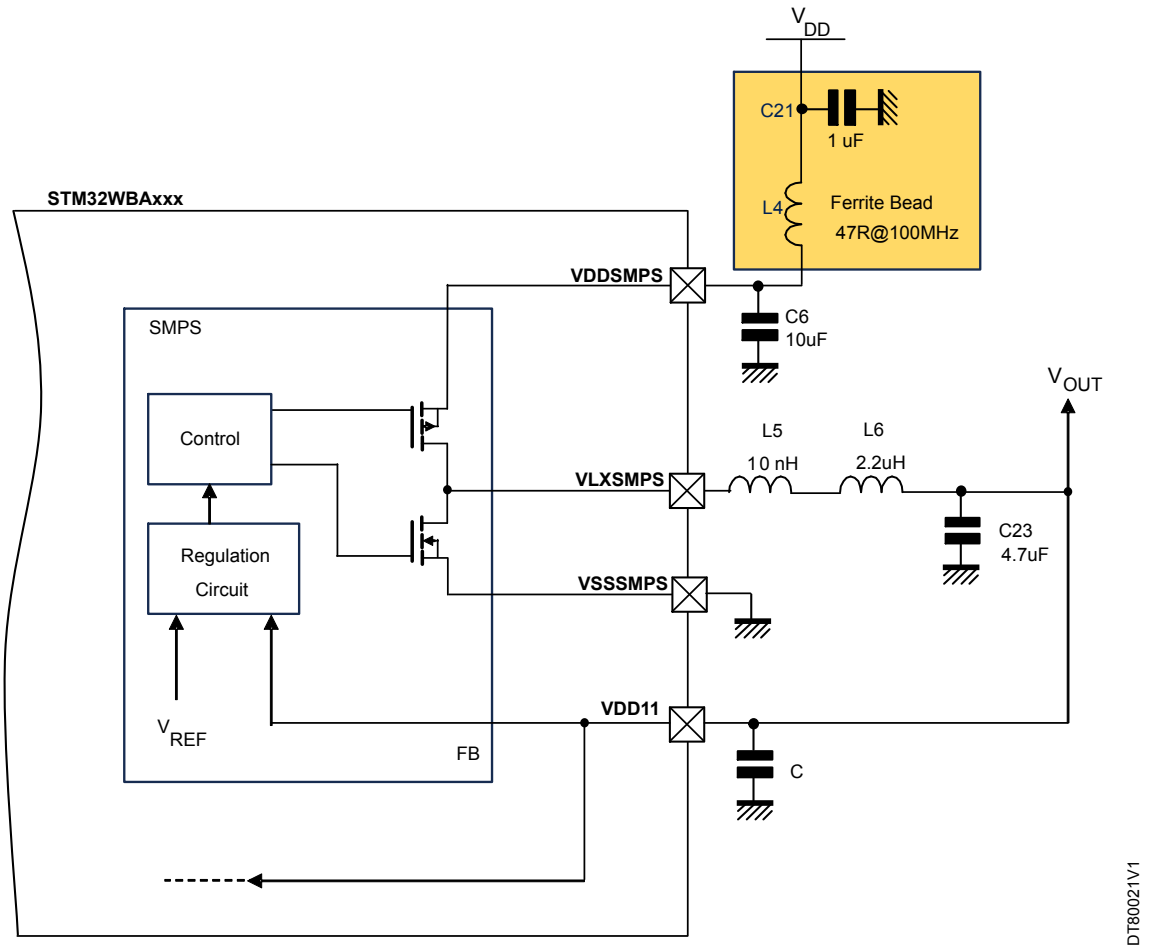
The converter draws current from the general power supply. This current draw consists of slots, as explained in the operation of the SMPS.

These current slots may generate some EMI perturbations for analog (ADC/comparator) and RF stages. For this reason, it is recommended to use a filter. An example of a filter includes a ferrite bead (47 Ω @ 100 MHz) and a 1 µF capacitor. Note that the DC resistance of the ferrite bead should be lower than 200 mΩ.

Example of a compatible part:

- Manufacturer: TAIYO YUDEN
- Part Number: LSMGA160808T470RG

Figure 9. Add-on LC filter to reduce noise on V_{DD}



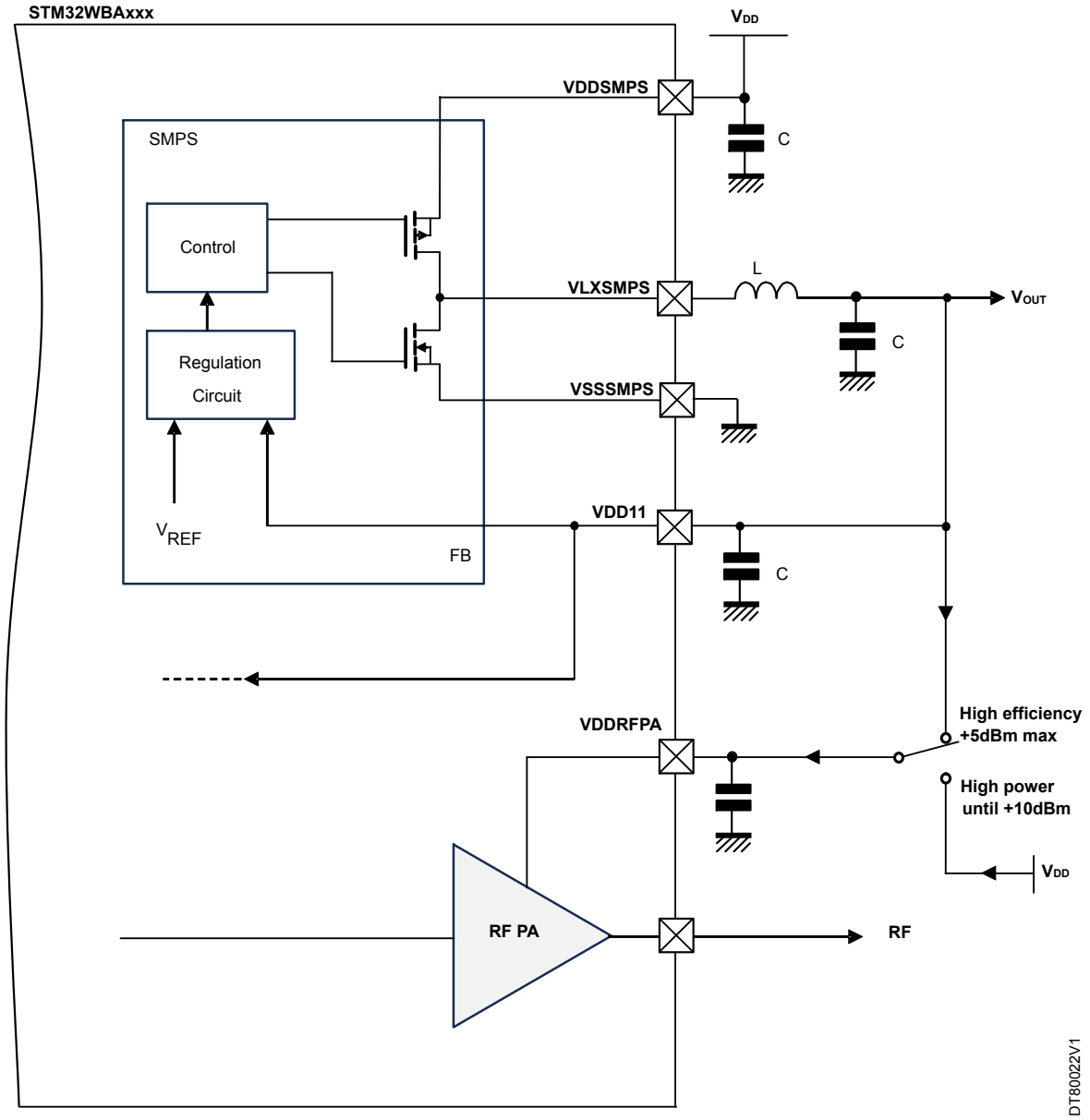
7 Using V_{OUT} SMPS to supply the internal RF power amplifier

The SMPS is designed to supply the main analog and digital parts of the circuit. It can also supply, with some limitations, the internal RF power amplifier (RF PA). The objective is to benefit from the power consumption efficiency for the RF PA, which requires a significant amount of current. To achieve this, connect the output of the SMPS to VDDRFPA.

However, this configuration has a limitation. Specifically, the output voltage of the SMPS is 1.2 V in TX mode, which is insufficient for the RF PA to drive an RF signal to +10 dBm. When VDDRFPA is connected to the SMPS output, the RF output level is limited to approximately +5 dBm.

If achieving +10 dBm is mandatory, VDDRFPA must be connected directly to VDD. In this case, the power efficiency gain from the SMPS is not applicable to the RF PA.

Figure 10. VDDRFPA connection (VDD or VOUT_SMPS)



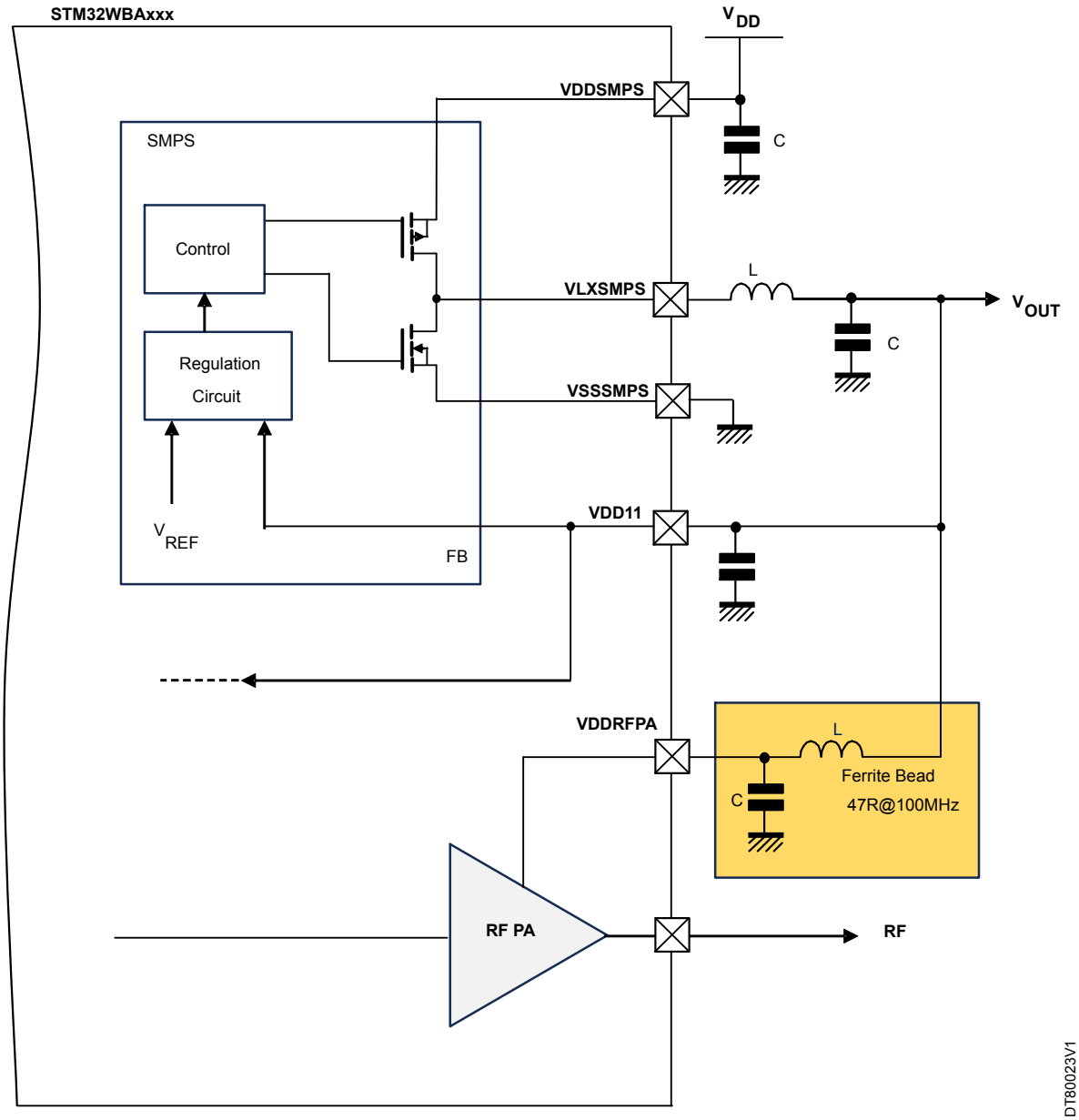
Depending on the choice of external components used for the SMPS, as well as the placement and layout of the SMPS section, it may be necessary to add a filter to supply the RF PA stage. The V_{RIPPLE} of the converter can generate additional spurious RF signals.

As described in Section 6.2: Limitation of SMPS switching noise on VDD, the DC resistance should be as low as possible.

Example of compatible part:

- Manufacturer: TAIYO YUDEN
- Part Number: LSMGA160808T470RG

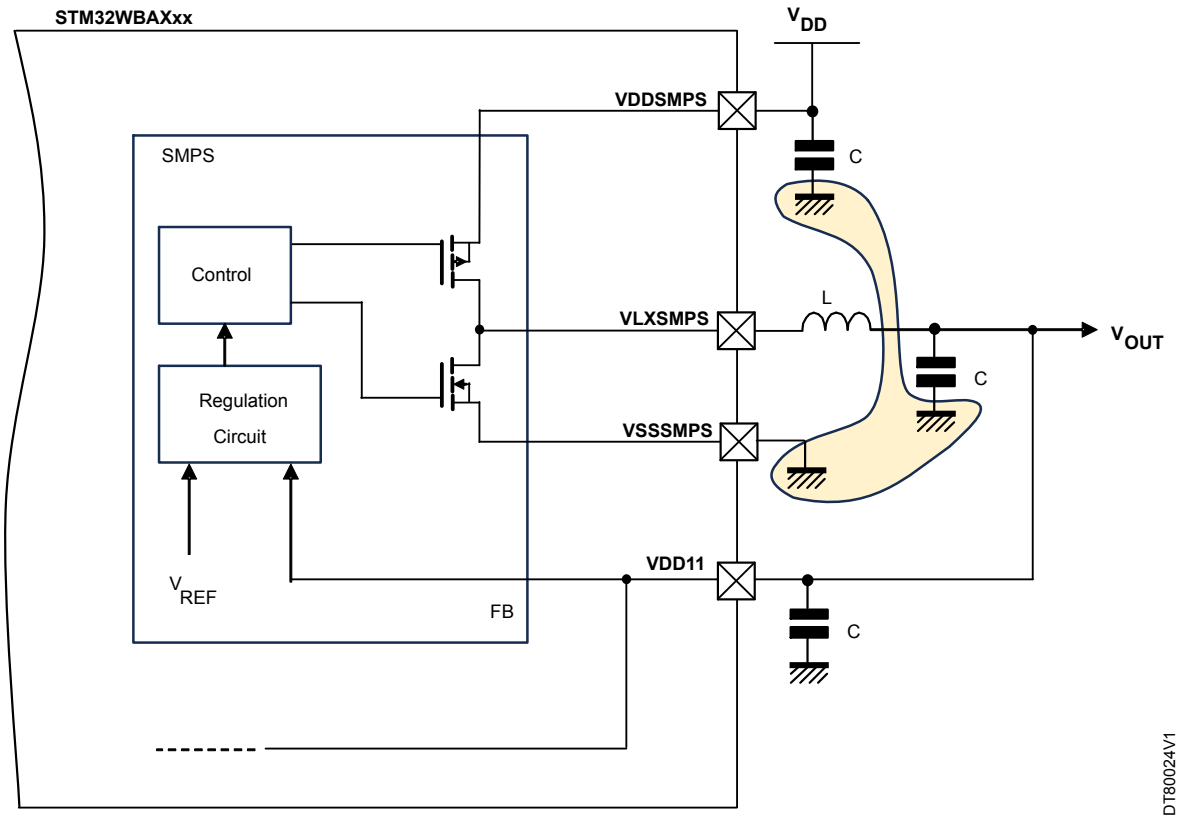
Figure 11. VDDRFPA Filter



8 PCB layout aspects

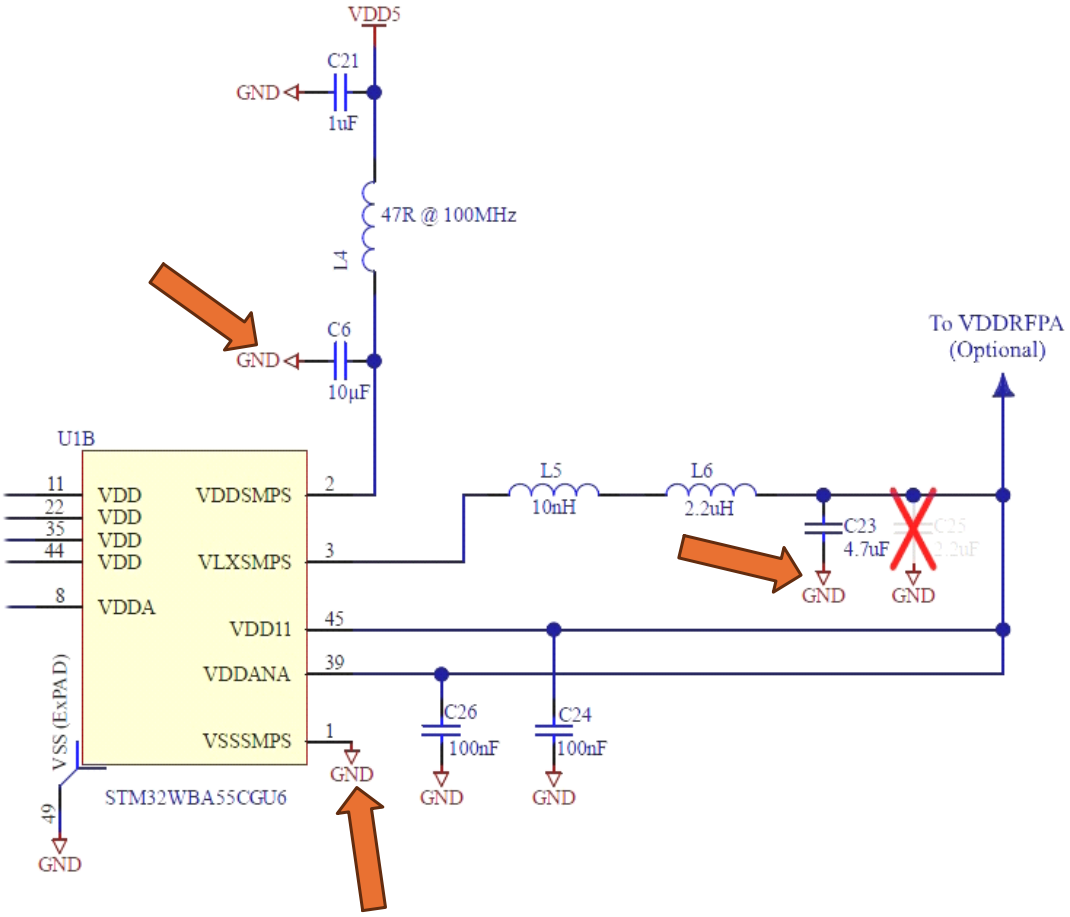
The layout of the SMPS section is critical to optimize its performance. The GND pin of the SMPS must be carefully connected to ensure optimal efficiency. If this precaution is not followed, the PCB tracks introduce resistance in series with both capacitors and the low-side MOSFET. As shown in the efficiency calculation above, this resistance reduces the performance of the SMPS.

Figure 12. Highlight of the important ground connection



As an example, consider the layout of the MB1803 (embedded on the NUCLEO-WBA55CG). The GND connections of C6, C23, and VSSSMPS (Pin 1 of the STM32WBA55) should be as short as possible. The schematic below identifies the relevant components.

Figure 13. SMPS part of the MB1803 (with highlight of important ground connection)



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In the figures below, the GND layout is shown in red. The GND pins of the capacitors and VSSSMPS are located very close to each other and are connected by a large area.

Figure 14. 2D view of the SMPS part of the MB1803

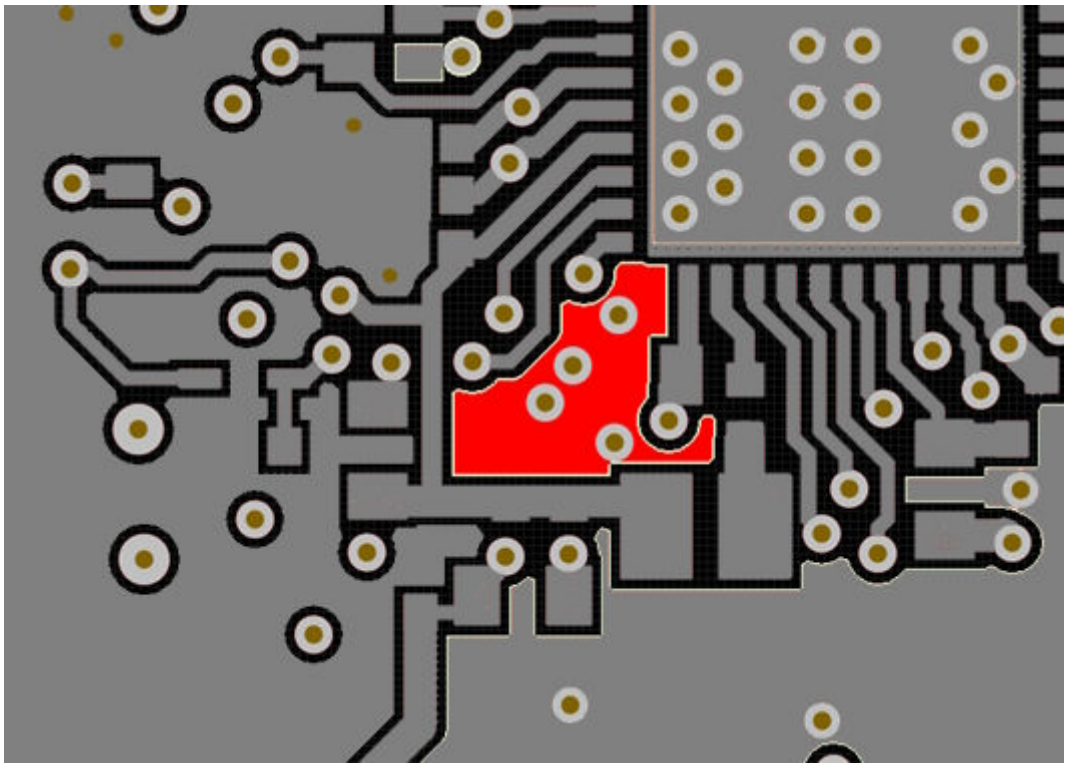
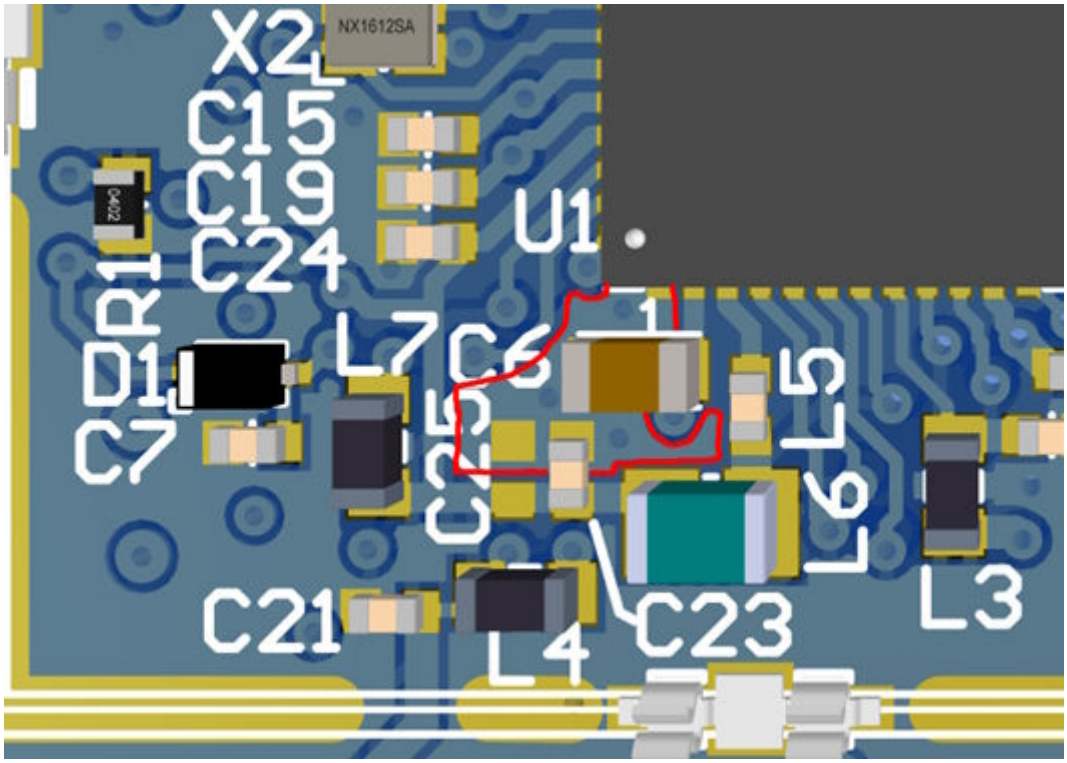


Figure 15. 3D view of the SMPS part of the MB1803



Revision history

Table 3. **Document revision history**

Date	Version	Changes
23-Oct-2025	1	Initial release.
13-Jan-2026	2	Reduced document scope to STM32WBA5xxx and STM32WBA6xxx MCUs. Updated Section 1: General information.

Contents

List of tables

List of figures