AN6323

Application note

Guidelines to select the right IPD MLPF-WL-0xD3 for STM32WL3x reference design

Introduction

This application note is dedicated to selecting the right IPD MLPF-WL-0xD3 according to the desired frequency band and power level associated with STM32WL3 MCUs.

STMicroelectronics develops integrated passive device (IPD) companion chips for optimized matching and harmonic filtering. The IPD is a very compact solution covering each of the main use cases such as 20 dBm at 915 MHz, 16 dBm at 868 MHz, 16 dBm at 433 MHz, and 10 dBm at 433 MHz.

1 IPDs for STM32WL3 and reference designs

7 integrated passive devices (IPD) companion chips are available to match each STM32WL3 configuration. The IPD integrates Tx matching networks, Rx matching networks, harmonics filter, and ESD shunt inductor. IPD is a very compact solution with a size of 1.47*1.87 mm² (see Figure 1).

Figure 2 shows RF IPD companion chips for STM32WL3. For more information on MLPF-WL-0xD3, refer to the website https://www.st.com.

Figure 1. RF matched filter MLPF-WL-0xD3

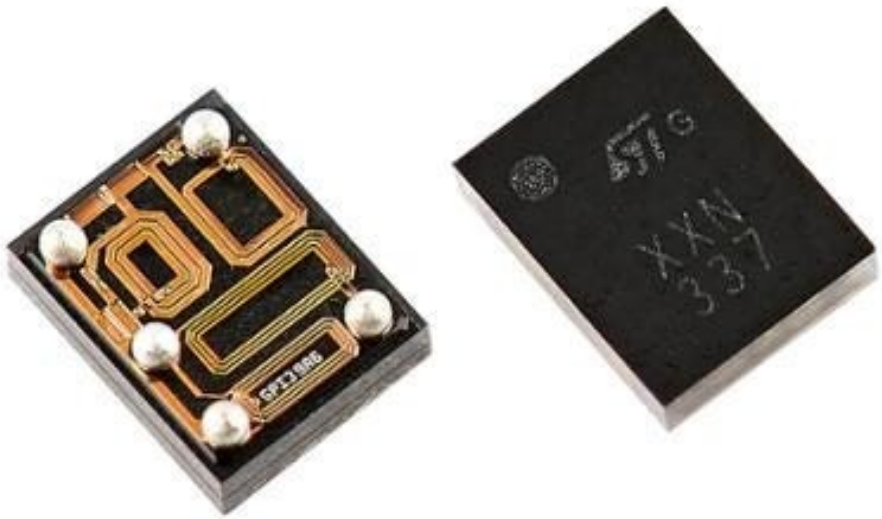
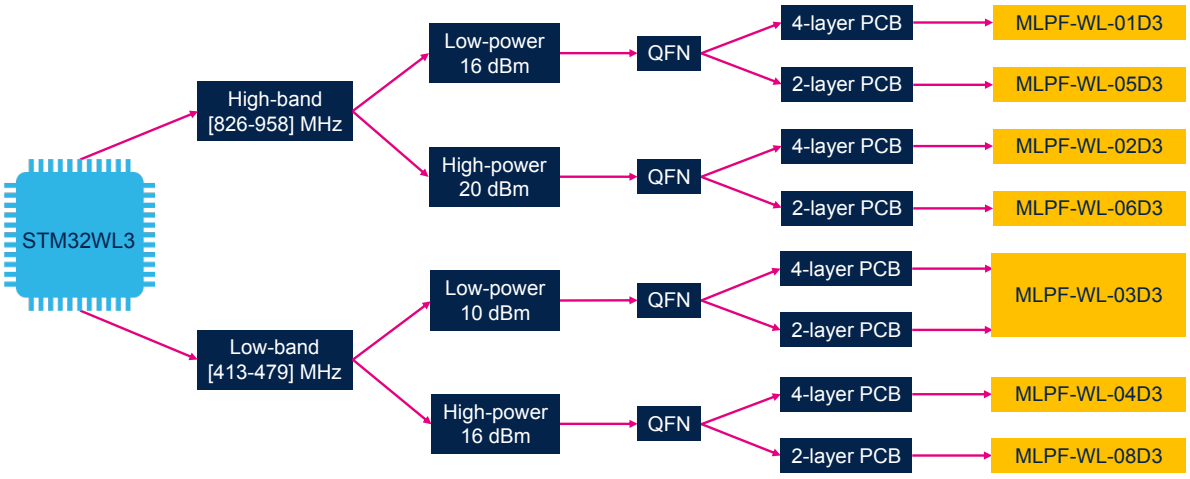


Figure 2. RF IPD companion chips for STM32WL3

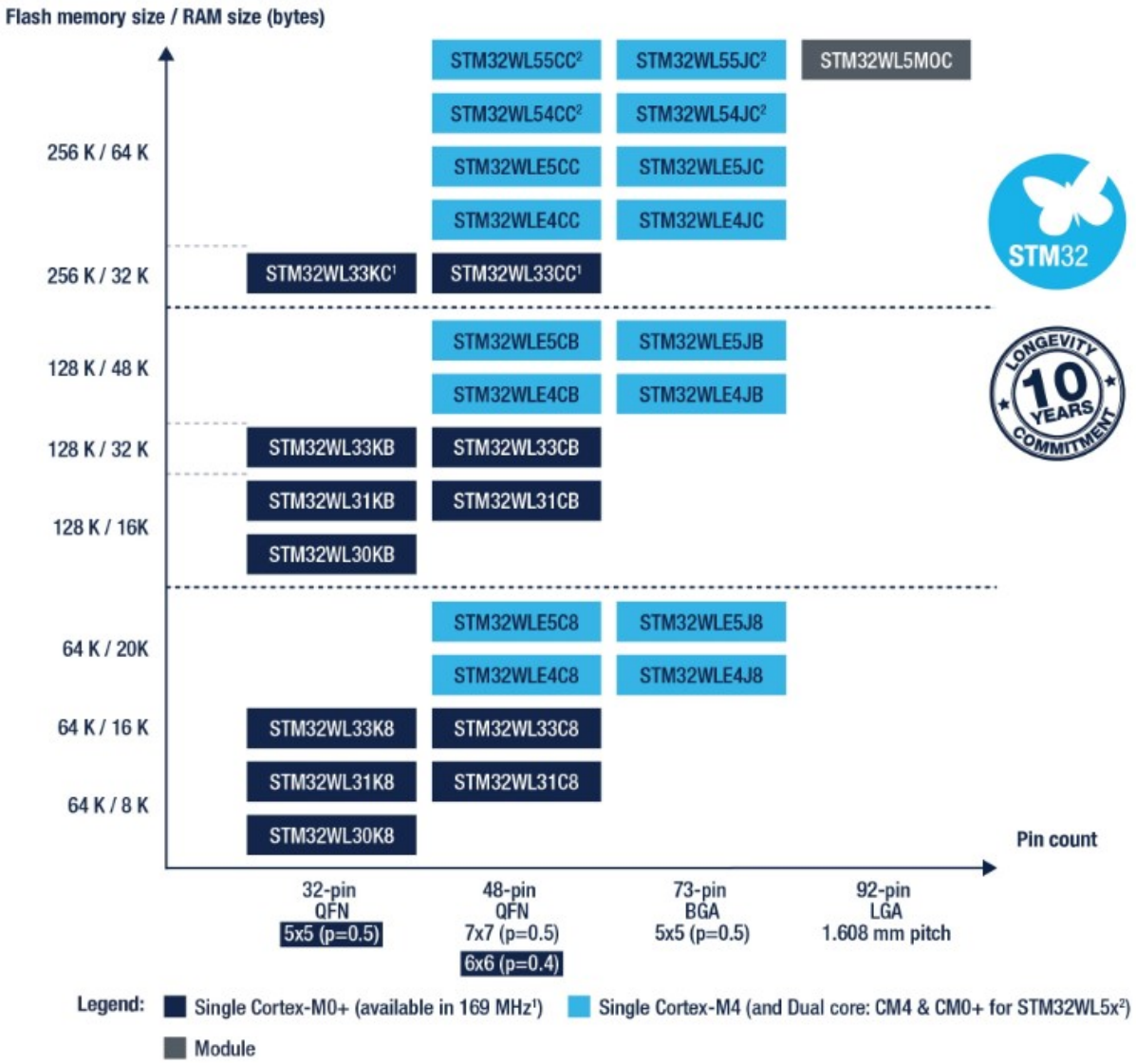


The STM32WL series provides a portfolio of System-On-Chip solutions integrating both a low-power microcontroller and a long-range, energy-efficient sub-GHz radio on the same chip.

For more information on the STM32WL series, refer to the website https://www.st.com.

A portfolio of companion integrated passive devices (IPD) integrates in a tiny footprint the RF fine-tuned BOM, such as harmonic filters, impedance matching available for each STM32WL3. Figure 3 lists the STM32WL series available, this application note refers to STM32WL3 (dark blue reference).

Figure 3. **STM32WL series portfolio**



Firstly, it is important to define the best package and STM32WL3 part number suited for the user application. For more information on the STM32WL3 series, refer to the website https://www.st.com.

Once the package and MCU part number are selected, this allows the user to select the layers number of the PCB in Table 1 for a 2-layer PCB or for a 4-layer PCB.

For 32-pin or 48-pin QFN, it is possible to choose between a 2-layer or 4-layer PCB. See for more details paragraph on 2-layer or 4-layer PCB recommendations for 48-pin QFN package.

Finally, the user must select the desired frequency and power level to choose the recommended IPD reference.

Table 1. IPDs for STM32WL5/E MCUs and web reference

STM32WL3 Part number	MCU Package	PCB # of layers	Power/ frequency	IPD	Web reference	Board reference
STM32WL33KC, STM32WL33KB, STM32WL31KB, STM32WL30KB, STM32WL33K8, STM32WL31K8, STM32WL30K8	QFN32	4	16 dBm / 868 MHz	MLPF-WL-01D3	NUCLEO-WL33CC1	MB2029
			20 dBm / 915 MHz	MLPF-WL-02D3	TBD	TBD
STM32WL33CC, STM32WL33CB, STM32WL31CB, STM32WL33C8, STM32WL31C8	QFN48		10 dBm / 433 MHz	MLPF-WL-03D3	TBD	TBD
			16 dBm / 433 MHz	MLPF-WL-04D3	NUCLEO-WL33CC2	MB2029
STM32WL33KC, STM32WL33KB, STM32WL31KB, STM32WL30KB, STM32WL33K8, STM32WL31K8, STM32WL30K8	QFN32	2	16 dBm / 868 MHz	MLPF-WL-05D3	STDES-WL3C2IMH	MB2176
			20 dBm / 915 MHz	MLPF-WL-06D3	TBD	TBD
STM32WL33CC, STM32WL33CB, STM32WL31CB, STM32WL33C8, STM32WL31C8	QFN48		10 dBm / 433 MHz	MLPF-WL-03D3	STDES-WL3C2ILL	MB2176
			16 dBm / 433 MHz	MLPF-WL-08D3	STDES-WL3C2IML	MB2176

Once the IPD reference has been selected for the user application, it is important to obtain reference designs, layout, and associated BOM recommendations to help the user in the design of the user application to get the right RF performance and to pass certification.

When all the parameters of the user application are known as well as the required IPD reference. Table 1 is used to obtain web references associated with IPD. These web references allow the user to obtain layout and associated BOM recommendations.

2 2-layer or 4-layer PCB recommendations

Integrated passive device (IPD) companion chips are tested and validated for achievable right power level on 4-layer PCB with 0.254 mm gap between the top layer and first ground inner layer (see Table 2, row 3), and on 2-layer PCB with 0.914 mm thickness (see Table 3, row 3).

Table 2. Stack-up recommendation for 4-layer PCB

Layer name	Material	Thickness (µm)	Dielectric constant
Top solder	Solder resist	10	3.5
Top Layer	Copper	41	
Prepreg 1	PP-VT47	254	4.4
Layer 1	Copper	18	
Core	Core-VT47	914	4.4
Layer 2	Copper	18	
Prepreg 2	PP-VT47	254	4.4
Bottom Layer	Copper	41	
Bottom solder	Solder resist	10	3.5

Table 3. Stack-up recommendation for 2-layer PCB

Layer name	Material	Thickness (µm)	Dielectric constant
Top solder	Solder resist	10	3.5
Top Layer	Copper	41	
Core	FR4	914	4.3
Bottom Layer	Copper	41	
Bottom solder	Solder resist	10	3.5

The recommended stack-up can be changed but it is important to respect some rules on the distance between the top layer and first ground inner layer (Table 2, column 3, row 3), or ground bottom layer for a 2-layer PCB (Table 3, column 3, row 3). These rules are described in more detail in the following paragraph.

The distance between the top layer and first ground inner layer of a 4-layer PCB should be close to 0.254 mm. The recommendation is to use IPD companion chips reference for 4-layer PCB (see Table 1). IPDs optimized for achieving the right power level on 4-layer PCB configurations with a separation of minimum 0.180 mm and of maximum 0.330 mm between the top layer and first ground inner layer (see Table 4). The other parameters of the stack up can vary slightly without having a major impact on the overall functioning of the product.

Table 4. Prepreg 1 thickness variation for 4-layer PCB

Stack up 4-layers	Min thickness (µm)	Recommended thickness (µm)	Max thickness (µm)
Prepreg 1	180	254	330

The distance between the top layer and ground bottom layer of a 2-layer PCB should be close to 0.914 mm. The recommendation is to use IPD companion chips reference for 2-layer PCB (see Table 1). IPDs optimized for achieving the right power level on 2-layer PCB configurations with a separation of minimum 0.650 mm and of maximum 1.200 mm between the top layer and ground bottom layer (see Table 5). The other parameters of the stack up can vary slightly without having a major impact on the overall functioning of the product.

Table 5. Core thickness variation for 2-layer PCB

Stack up 2-layers	Min thickness (µm)	Recommended thickness (µm)	Max thickness (µm)
Core	650	914	1200

Note: For thinner 2-layer PCB, if the distance between layers 1 and layer 2 is close to 0.300 mm, the user should choose IPD dedicated to 4-layer PCB.

3 Example to select the right IPD and reference design associated

For example, the user application needs:

- 128 Kbytes flash memory and 32 Kbytes RAM and 48-pin QFN package. Using Figure 3, the MCU STM32WL33CB can be suitable.
- Using Table 1 to select the right column and row for the package and MCU reference.
- The user application is manufactured on a PCB with a distance between the top layer and the first inner layer around 0.230 mm. The recommendation is to use a 4-layer PCB (Table 1, column 3, row 1)
- The user application operates at a power of 16 dBm at the frequency of 868 MHz (Table 1, column 4, row 1).
- Using Table 1, we can find that the IPD that is recommended for the user application is MLPF-WL-01D3 (Table 1, column 5, row 1).

Now that we have selected the right MLPF-WL-01D3 IPD for the user application, the web reference is available (Table 1, column 6, row 1). This web reference NUCLEO-WL33CC1 allows the user to reach the CAD resources for MLPF-WL-01D3 IPD.

In the CAD resources tab, all information about board manufactured specifications, bill of materials and schematics are available to help the user to design the user application.

4 Conclusion

In summary, to select the right MLPF-WL-0xD3 IPD for the user application:

1. Choose the reference for *ST32WL3x MCUs* and the *package* needed.
2. Choose a *2-layer* or *4-layer* for manufactured PCB.
3. Choose the desired frequency and power level.
4. Choose the right MLPF-WL-0xD3 based on the information from the points above and using Table 1.
5. Obtain the *web reference* of the selected MLPF-WL-0xD3 using Table 1 to have all the information about board manufactured specifications, bill of materials and schematic are available to help the user to design the user application.

Revision history

Table 6. **Document revision history**

Date	Revision	Changes
27-Jun-2025	1	Initial release.

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