Application note

Layout recommendations for the design of boards with the ST25R300, ST25R500, ST25R501 and ST25R210 devices

Introduction

This application note provides important information and guidelines to properly implement ST25R300, ST25R500, ST25R501 and ST25R210 ground handling, layout, and decoupling capacitor placement.

The following chapters explain the mechanisms to mitigate unwanted emissions, and to keep the overall noise floor to a low level.

Table 1. **Applicable products**

Type	Product
ST25 NFC / RFID Tags and readers	ST25R300
	ST25R500
	ST25R501
	ST25R210

1 General recommendations

The guidelines to optimize EMC performance for PCB design are detailed in this section.

- Always consider and determine where and how the return currents are flowing.
- Do not route signals over ground gaps.
- Partition mixed-signal PCBs with separate analog and digital sections.
- Do not split the current return plane; use one solid plane under both analog and digital sections of the board.
- Route digital signals only in the digital section of the board (for all digital related layers).
- Route analog signals only in the analog section of the board (for all analog related layers).
- In case ground or power planes are split for a specific reason (that is, mechanical and or electrical), do not run any traces across the split on an adjacent layer.
- Traces (analog or digital) that must go over a power plane split must be on a layer adjacent to a solid ground plane (analog or digital).
- A/D and D/A converters, as well as most other mixed-signal ICs, should be considered as analog devices with a digital section, not digital devices with an analog section.
- The AGND and DGND designation on the pins of a mixed signal IC refers to where the pins are connected internally, and it does not imply where or how they should be connected externally. On most mixed-signal ICs, both the AGND and DGND pins should be connected to the analog return plane.
- The digital decoupling capacitor must be connected directly to the digital ground pin.
- The decoupling capacitors are needed to supply, through a low-inductance path, some or all of the transient power supply current required when an IC logic gate switches.
- Decoupling capacitors are needed to short out, or at least reduce the noise injected back into the power ground system.
- Decoupling is not the process of placing a capacitor adjacent to an IC to supply the transient switching current; rather it is the process of placing an L-C network adjacent to the IC to supply the transient switching current.
- The value of the decoupling capacitor(s) is important for the low-frequency decoupling effectiveness.
- The value of the decoupling capacitor(s) is not important at high frequencies. At high frequencies, the most important criteria is to reduce the inductance in series with the decoupling capacitors.
- Effective high-frequency decoupling requires the use of a large number of capacitors.
- Place decoupling capacitors as close as possible to the device.
- Route RFI and RFO signals symmetrically and avoid long signal traces for the matching network. Keep the traces between RFO1 and RFO2 close to each other, and do the same for RFI1 and RFI2.
- The matching components need to be placed close to each other, and symmetrically.
- Care needs to be taken on the placement of quartz crystal oscillator (XTAL) and its startup behavior must be carefully analyzed.. Long connections to the XTAL may cause negative effects on the system by adding parasitic capacitances, and be more prone to the influence of external signals/noise and impair the startup behavior.

2 Device specific layout requirements

2.1 Exposed pad

The exposed pad/thermal pad called VSS underneath the ST25R300, ST25R501, ST25R210 and ST25R500 provides both a ground plane and a thermal heat sink. This pad must be connected to the PCB ground plane by multiple through-vias and must be plated to have good soldering results. The multiple vias keep the total parasitic inductance in this area low.

Figure 1. Exposed pad top view and recommended QFN32 GND layout

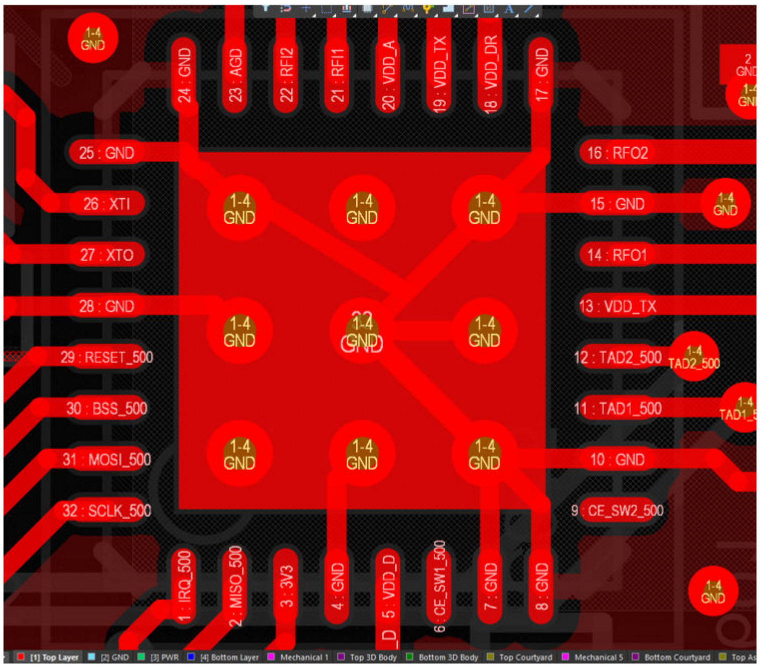


Figure 2. Exposed pad top view and recommended QFN24 GND layout

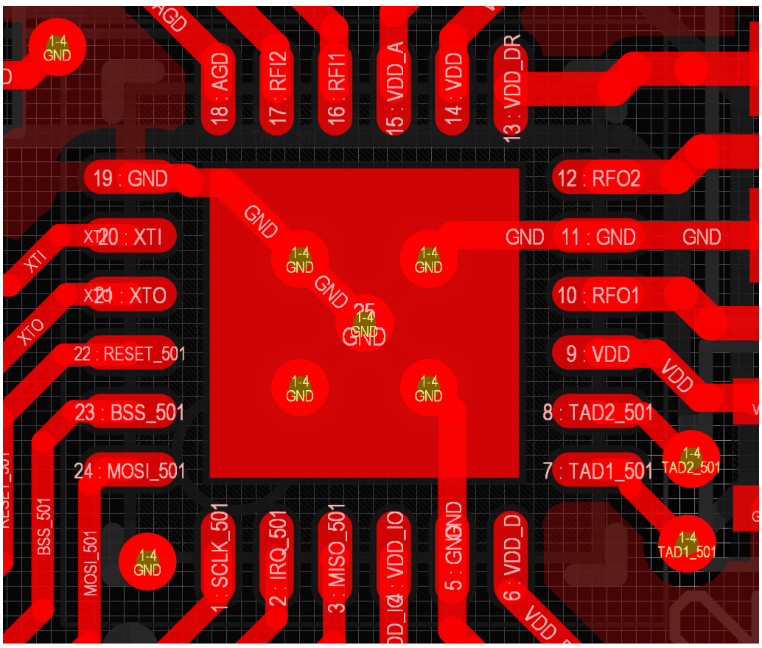
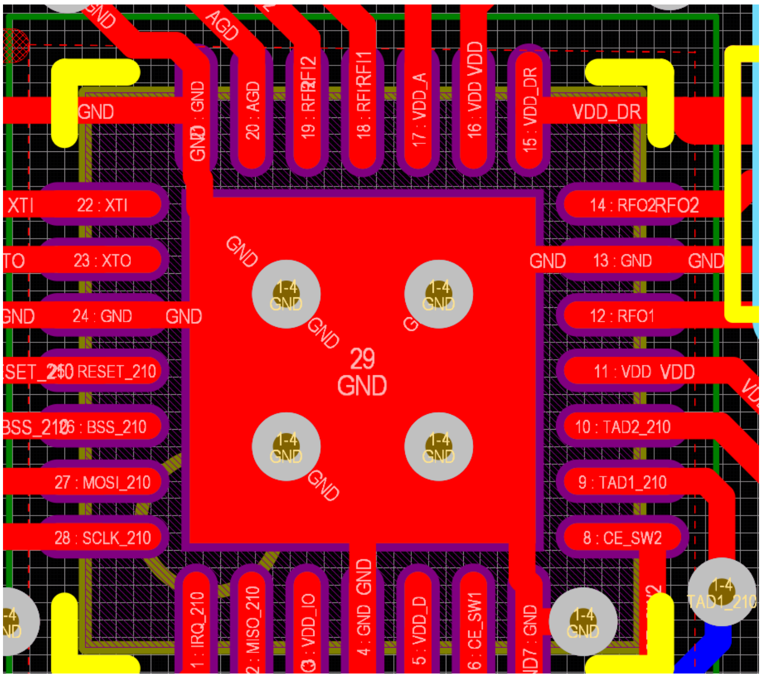


Figure 3. **Exposed pad top view and recommended QFN28 GND layout**



2.2 GND pins connection and routing

The ST25R300, ST25R500, ST25R501 and ST25R210 devices have five GND pins.

Table 2. **GND pins connection**

Function	UQFPN32, VQFN32	VFQFPN24	UFQFPN28
GND_D	Pin 4	Pin 5	Pin4
GND_GPIO	Pin 7	N/A	Pin 7
GND_DR	Pin 15	Pin 11	Pin 13
GND_A	Pin 25	Pin 19	Pin 21
VSS	EP / Pin 28	EP / Pin 25	EP / Pin 24

All these GND pins must be directly connected to the exposed pad in the shortest way from the pad to the center. A PCB trace width of at least 0.2 mm connecting the GND pins must be regarded. Figure 1 contains an example of recommended layout.

2.3 Decoupling capacitors

All capacitors associated with the ST25R300, ST25R500, ST25R501 and ST25R210 regulators and AGD voltage pins (VDD_D, VDD_TX, VDD_A, VDD_DR and AGD) must be positioned as close as possible to the device. A recommended distance of less than 3 mm for VDD_DR and AGD between the device pins and the capacitor should be regarded. A placement example of the decoupling capacitors is depicted in the figure below.

Table 3. **Recommended capacitor values**

Pin	Capacitor(1)	Capacitor (2)	Comment
VDD	10 nF	2.2 µF / 10 V	-
VDD_TX	10 nF	2.2 µF / 10 V	-
VDD_IO	100 nF	d.n.p.	-
VDD_DR	47 nF	d.n.p.	-

Pin	Capacitor(1)	Capacitor (2)	Comment
VDD_D	10 nF	d.n.p.	-
VDD_A	10 nF	2.2 µF / ≥10 V	-
AGD	10 nF	1.0 µF / ≥10 V	-

1. *Capacitor 1 should be placed as close as possible to the associate pin.*
2. *Capacitor 2 should be placed as close as possible to Capacitor 1.*

Note: ***d.n.p.*** *means "do not populate" (note to be placed on the PCB).*

Figure 4. Decoupling capacitors placement QFN32 package

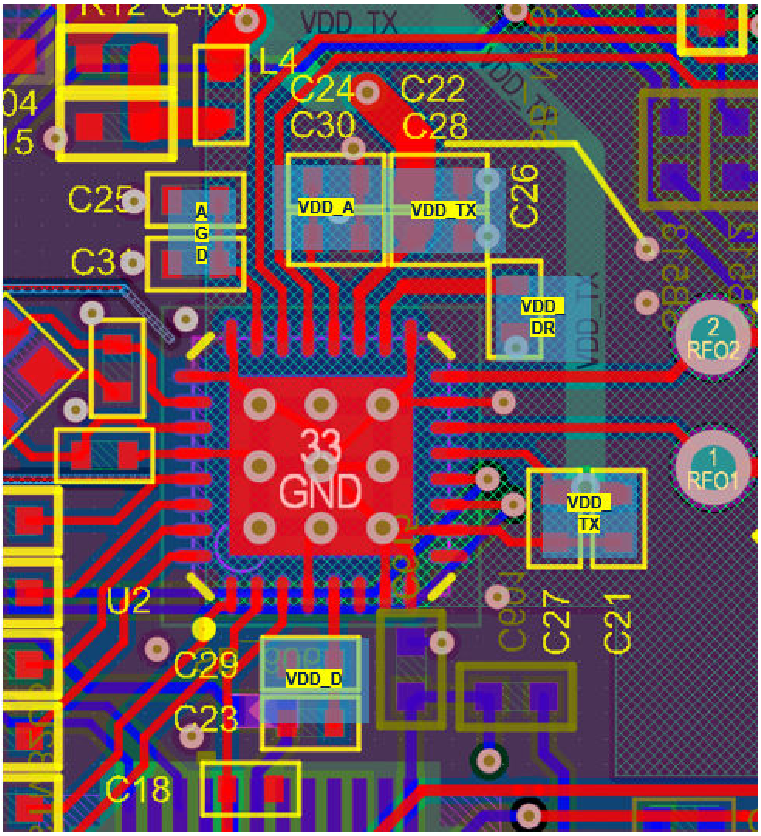
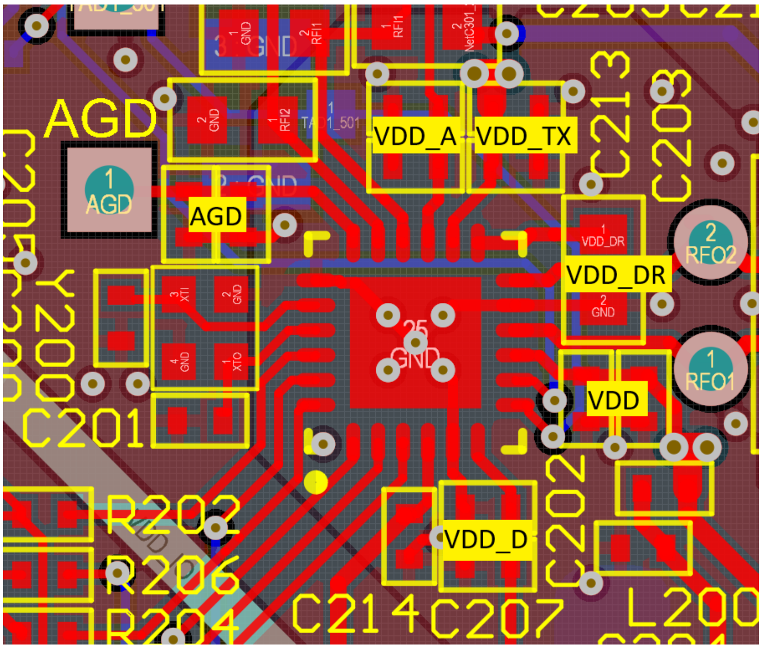


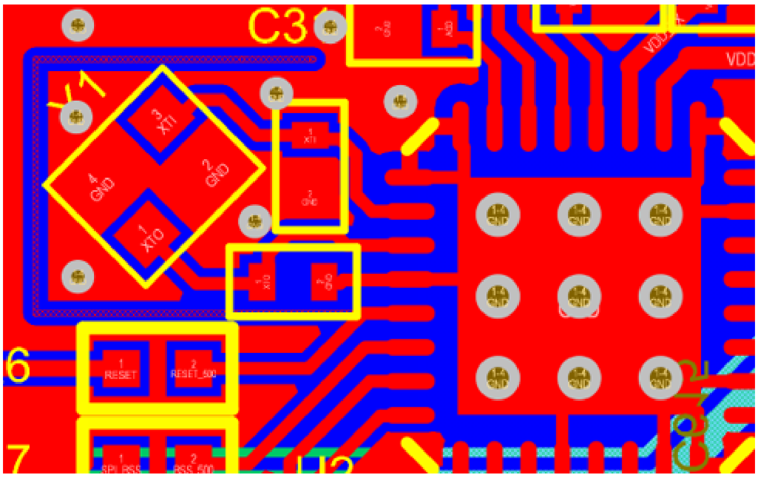
Figure 5. Decoupling capacitors placement QFN24 package



2.4 Crystal placement

In a similar way to the decoupling capacitors, the XTAL must be positioned as close as possible to the XTI/XTO pins. To avoid crosstalk from other signals, those PCB traces should be separated by a GND area. Figure 6 shows a layout example in which the GND area of the crystal is isolated from the remaining GND area to create a silent GND potential. The crystal area must be connected to GND through multiple vias.

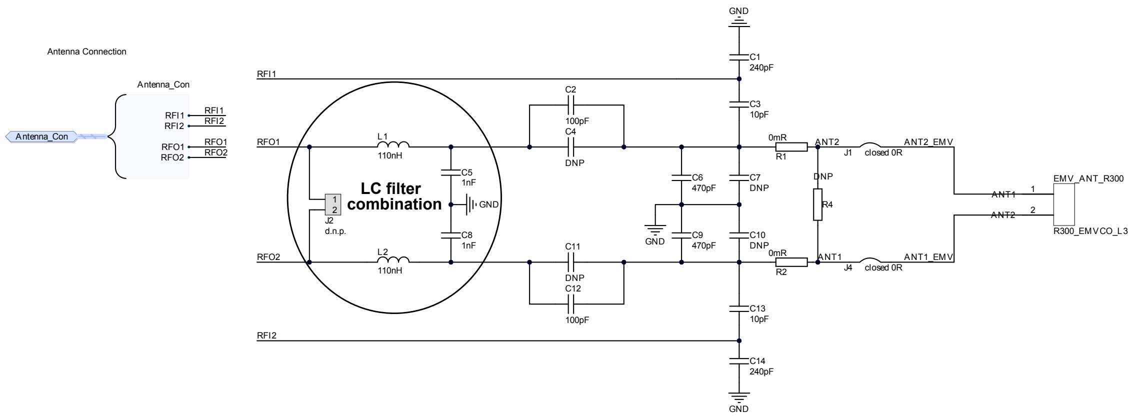
Figure 6. Crystal layout recommendation



3 General considerations

The generated RF signal at RFO1 and RFO2 is a rectangular-shaped signal, which must be fed into an antenna-matched LC tank for a proper RF communication. The RFOs are low-pass filtered with an inductance/capacitance combination to reduce harmonics. This is accomplished by an LC combination at the output of the RF drivers, as shown in the figure below.

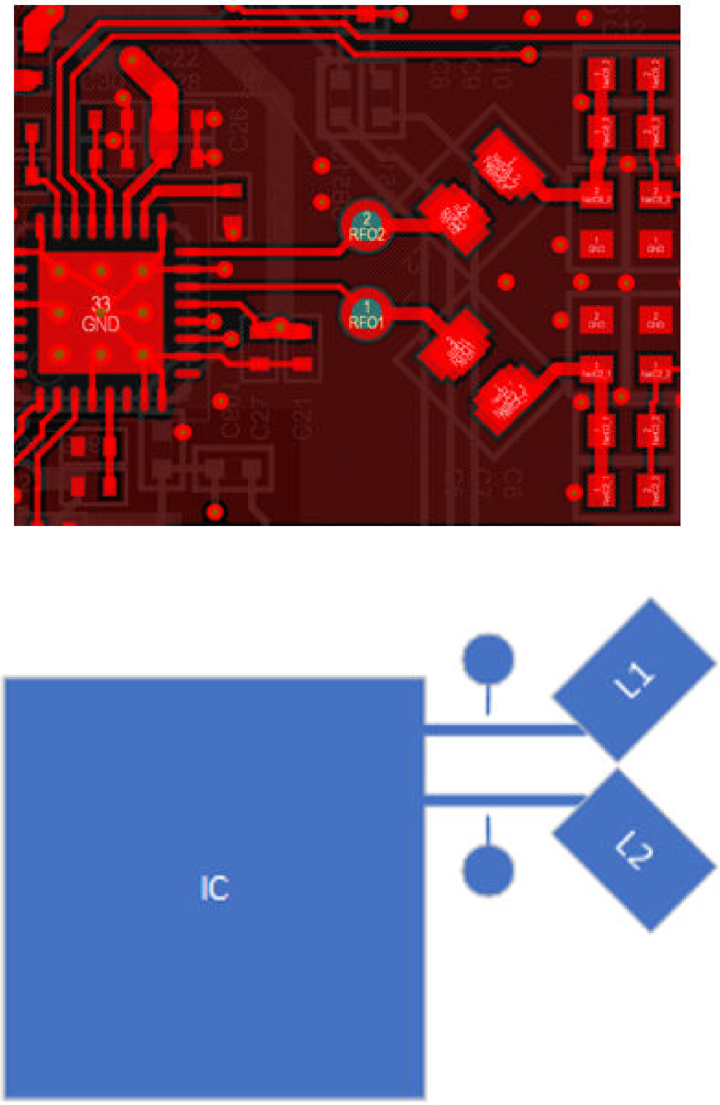
Figure 7. Antenna matching circuit and filtering



It is important to position the filter network as close as possible to the output stages (as in Figure 8. Positioning of the low-pass filter on the PCB and alternative RFO testpoints with solder bridges), to avoid unwanted radiation over long traces.

The LC filter in Figure 8. Positioning of the low-pass filter on the PCB and alternative RFO testpoints with solder bridges could have been placed closer to the RFO1/2 pins. However the space on the demonstration board is used for a 2-pin header to better probe the impedance curve for matching purposes. Such pin-header holes should be removed in the final design to avoid unwanted radiation throughout the openings. Alternatively, two test pads can be placed next to the RFO points to better probe the matching circuit.

Figure 8. Positioning of the low-pass filter on the PCB and alternative RFO testpoints with solder bridges



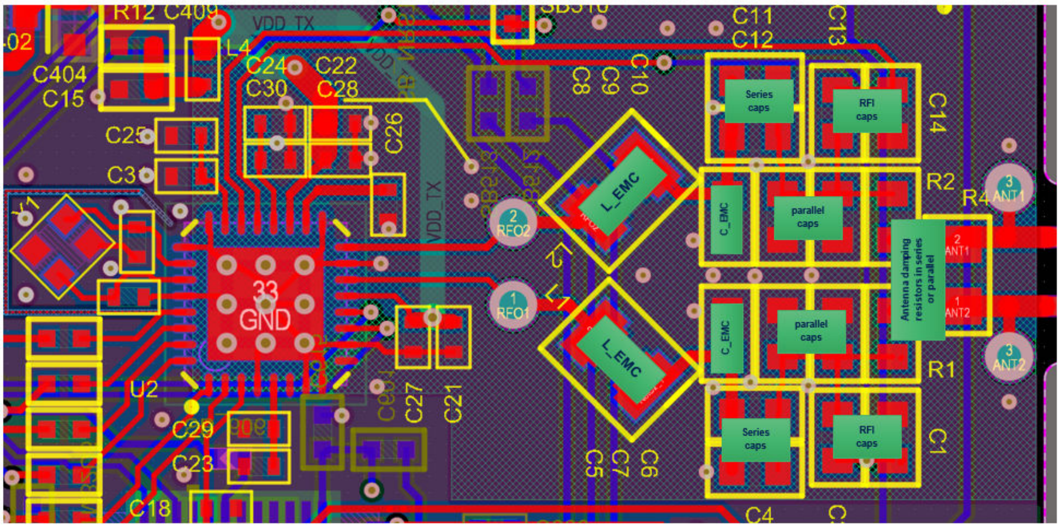
4 Radiation from traces

One of the sources of radiation can be identified in the exposed traces. To understand how traces radiate, the signals must be analyzed during their propagation. A signal propagating along traces can be divided into two main parts, namely a differential signal and a common-mode signal.

4.1 Differential signals

The total radiated field from a differential signal propagating along two traces tends to cancel itself, and in ideal conditions is zero. The same effect applies to the output drivers of ST25R300, ST25R500, ST25R501 and ST25R210, which are operating in differential mode. However, due to component tolerances and signal asymmetries along the traces, differences in the current flow may appear and consequently a non “quasi-zero” electric field is generated. Take care to lay out the matching topology in a symmetrical way.

Figure 9. Matching network components and layout



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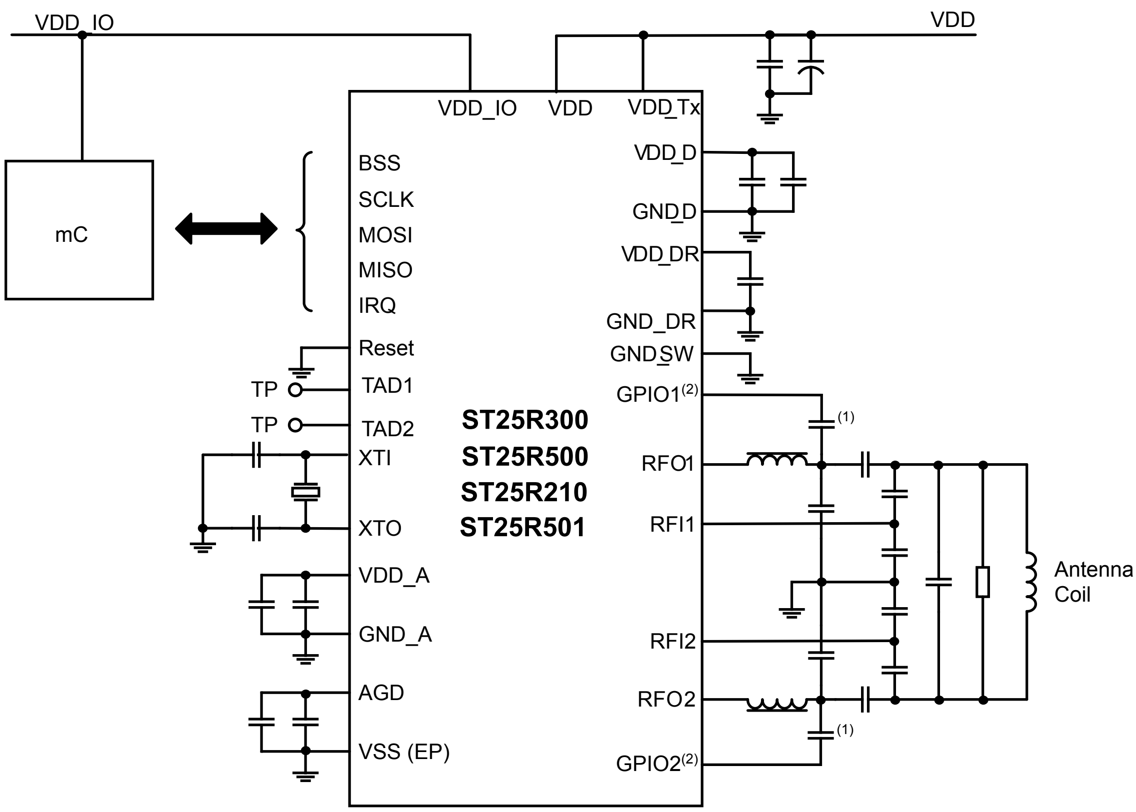
4.2 EMI capacitor switching via GPIO pins

Two GPIO pins can be used to change the matching between reader operation and card emulation operation. Figure 10 shows the minimum configuration including the possibility to switch the matching between reader and card emulation operation. The GPIO pins are not available on the ST25R501 and VFQFPN24 package.

Figure 10. EMI capacitor switching via GPIO pins



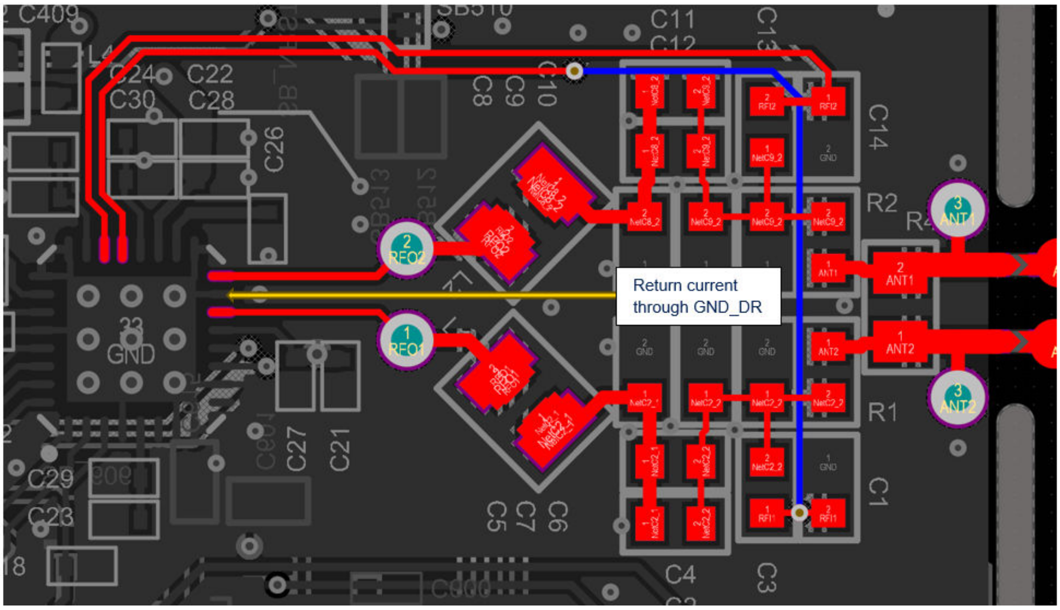
1. *Only required for CE operation. If only RW operation is required, the capacitor can be D.N.P and the pin left open.*
2. *Not available on VFQFPN24 package of ST25R501.*

When card emulation operation is not required, the capacitors connected to GPIO1 and GPIO2 should not be populated. The pins can be left floating. The capacitor connected between the EMI filter and GPIO1, and EMI filter and GPIO2 pin is pulled to GND through an internal MOS transistor. Since this capacitor can build a series resonating circuit with parasitic components (bond wires, PCB traces), special care must be taken when selecting the capacitor value. The NFC IC outputs a 13.56 MHz signal and its harmonics at its RFO pins. Radiated emission standards can be violated when the series resonating circuit has its resonance frequency at a multiple of 13.56 MHz. Selecting a different component value of the capacitor connected to the GPIO pins can reduce the emissions to a normal level.

5 RFO and RFI routing

The transmit and receive stages of the ST25R300, ST25R500, ST25R501 and ST25R210 are differential pairs and need to be treated carefully during the PCB layout to minimize unwanted signal coupling and radiated emissions. These signals should be routed in an internal layer, but to avoid a large number of vias interconnecting the traces with the matching components, the complete matching network is placed on one side (the top layer) of the PCB. The return current flows under the traces in the GND layer. It is important to have no cuts in the GND layer below the matching circuit.

Figure 11. **RFO and RFI routing**



It is essential to avoid so called through-vias in the matching layout, because they only contribute to unwanted emissions. Note how the matching components are close to each other to reduce the trace length from RFO to the antenna feed. It is not advised to having long signal traces between the LC filter and the remaining matching components. The inductors after the RFO should be positioned side by side or in 45-degree relation to each other depending on the coil technology to minimize coupling effects. The RFI lines are routed symmetrically, at a reasonable distance from the RFO lines. Never route the RFI signals separated from each other, and do not use different signal lengths. Alternatively, the RFI lines can be routed through the middle of the matching network back to the RFI pins.

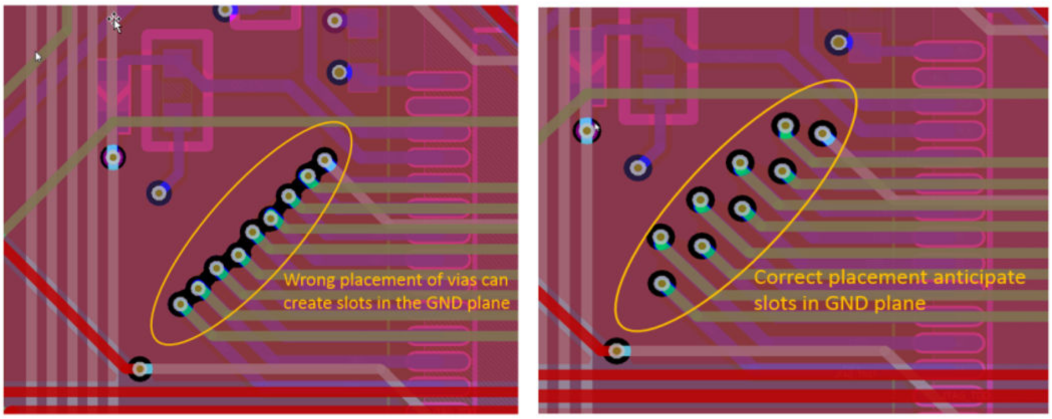
Additionally, all the components (capacitors) to GND along the RFO path are connected to GND by using multiple vias to minimize inductance, and consequently avoid unwanted resonances.

6 Common-mode signals

Common-mode radiation mainly emanates from the connected cables of a PCB system. The PCB reference ground plane inductance (and consequently the ground voltage) is the major contributor to the common-mode radiation. Common-mode radiation is produced more effectively than differential mode radiation. Even a small amount of common-mode current can result in significant emission problems. To reduce common-mode emissions:

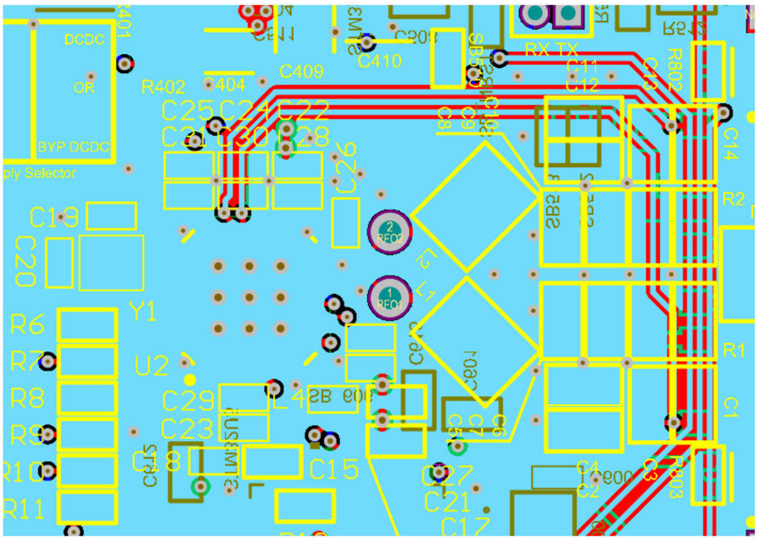
- Keep the current supply path close to the current return path.
- Reduce the cable length.
- Minimize the common-mode voltage (usually the ground potential). Reducing the ground impedance can be done by using solid ground planes or ground grids, and by avoiding slots in the ground plane (see the differences in Figure 8 and Figure 9).

Figure 12. Avoiding slots in the GND plane



Another example of incorrectly using the GND plane for signal traces is given in Figure 13. Some traces like the RFI lines are routed in the GND plane causing a cut in the plane and thus forcing the return current traveling a nonoptimal route.

Figure 13. Traces routed in GND plane



Take care of the connected cables (if any) and shield them properly. This can be done, for instance, using common-mode impedance choke in series with the cable, with some isolation between connections from the enclosed cable to the PCB ground. An integrated common-mode filter (ECMF02-4CMX8) for USB D+ and D- lines and ESD protection for all lines can be used, as exemplified in Figure 14 and Figure 15.

Figure 14. Common-mode filter - Position on the PCB

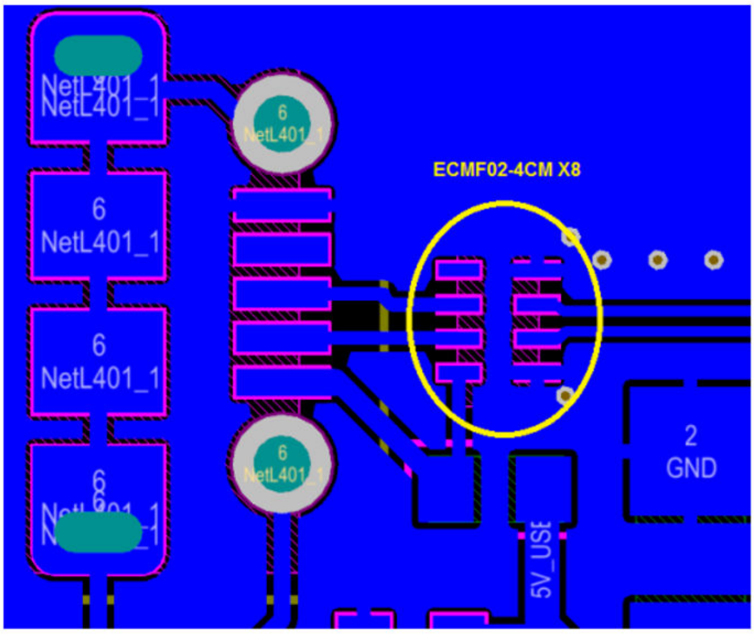
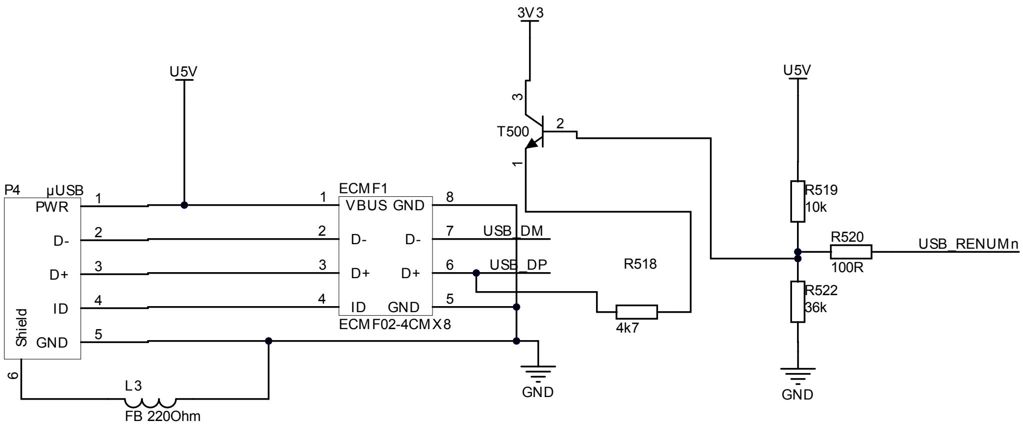


Figure 15. Common-mode filter - Schematic



6.1 SPI data signal routing

The SPI data signals from the ST25R300, ST25R500, ST25R501 and ST25R210 to the MCU must be routed (as much as possible) with equal length and controlled impedance. Keep the trace length of the SPI interface short and minimize the use of vias. Avoid routing the SPI signals over crystal oscillators (such as those generating the 27.12 MHz or 13.56 MHz frequencies), to minimize crosstalk and signal distortion.

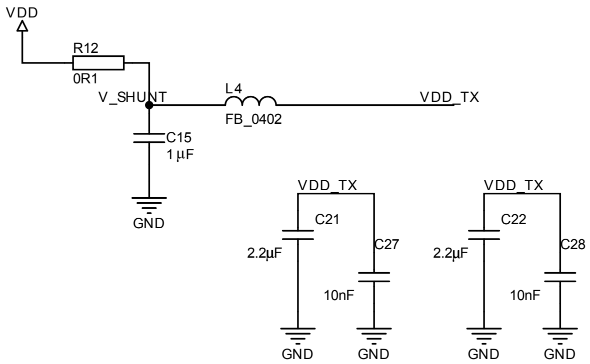
7 Parasitic components and current return paths

During the PCB design, pay attention when selecting of passive components and their parasitic contribution. Most of the time component manufacturers provide measured values only at low frequency, or in a frequency range not compatible with the one used in the PCB being designed. It is then critical for a designer to know the exact value and the parasitics within the whole considered frequency range for each passive component used in the design to avoid undesired system resonance that may lead to unintentional radiating effects. Together with the parasitic effect, the current return path on the PCB must be evaluated. All currents return to their source: they flow in loops, and the return path has a large impact on radiated emissions. Note that currents returning to the source follow different paths, depending upon the frequency: the path with the lowest resistance is the preferred one at low frequencies, the path with the lowest inductance prevails in the high frequency range. To understand return path resistance, it is important to calculate the impedance of a stripline and of a microstrip in the PCB, to identify paths with high and low impedance.

8 Power supply layout and filtering

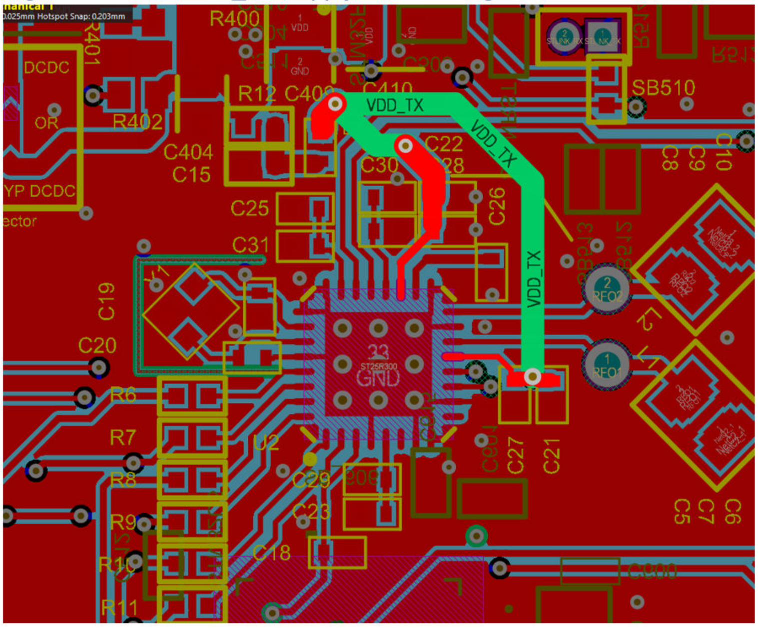
External noise may be injected into the system via the power supply, and, similarly, internal noise may be conducted to the outside of the board on the DC power leads. It is advised to put in place filters in the PCB power supply system design to reduce the effect of noise and transients on the lines. Both common mode filtering and differential mode filtering are applied on the PCB. The power supply filter of the ST25R300, ST25R500, ST25R501, and ST25R210 VDD pin can be formed by a PI filter. Typical values for capacitors range from 1 to 0.01 µF, and for the ferrite bead the typical resistance value varies from 50 to 1500 Ω in the frequency range of interest. Avoid saturation of ferrite bead by DC current.

Figure 16. **VDD/VDD_TX supply filtering**



The supply lines to the pins VDD and VDD_TX should be kept as short as possible from the supply source as outlined in Figure 17. Do not route the supply lines around components or in loops and avoid crossing components and traces whenever possible. Layout the VDD supply for the ST25R300, ST25R500, ST25R501, and ST25R210 devices in a star topology.

Figure 17. **VDD/VDD_TX supply lines routing**



9 Mixed signal PCB layout

When a designer faces the design of a mixed signal system, the main question that comes in the PCB layout definition is related to the separation of the analog and digital parts, and consequently on how to handle the separation of ground between the two subsystems. The origin of the split GND approach comes from the need to keep separated return currents for analog and digital subsystems. The separation between the two subsystems can be achieved by a physical separation of the two grounds (real cut) or by their spatial separation. When using more than one mixed signal IC with common GND connections for analog and digital signal, the approach of having separate grounds may cause more issues compared to a single GND configuration. In this case, it is recommended to use only one current return plane, paying attention to partition the PCB area into digital and analog sectors; route analog and digital signals only in the analog and digital sector, respectively, to keep the return current paths separated. The use of a split GND plane can create other problems because of the presence of possible multiple return paths of the supply current, and consequently of possible current loops. The supply current must return through a common ground terminal to which both the analog and the digital sub subsystem are referenced. The presence of the current loop generates radiated emission, with the emission level being proportional to the loop area and to the current intensity. A typical configuration for an 6 layer PCB is shown in Figure 18. The GND and power plane are realized in layer 2 and layer 5 respectively, while signal lines are routed on layer 1, 3, 4 and 6 .

Figure 19 shows a 4-layer PCB stack up configuration. Signals are routed on the top and bottom layer. The inner layers are composed of a separate GND and power supply layer.

Figure 18. 6-layer PCB configuration

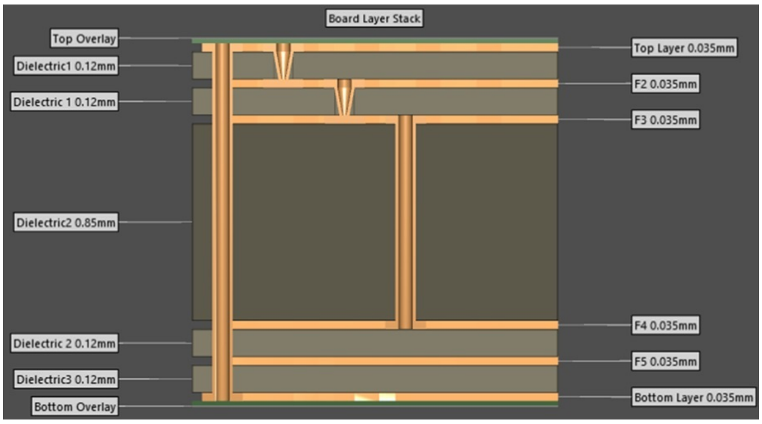
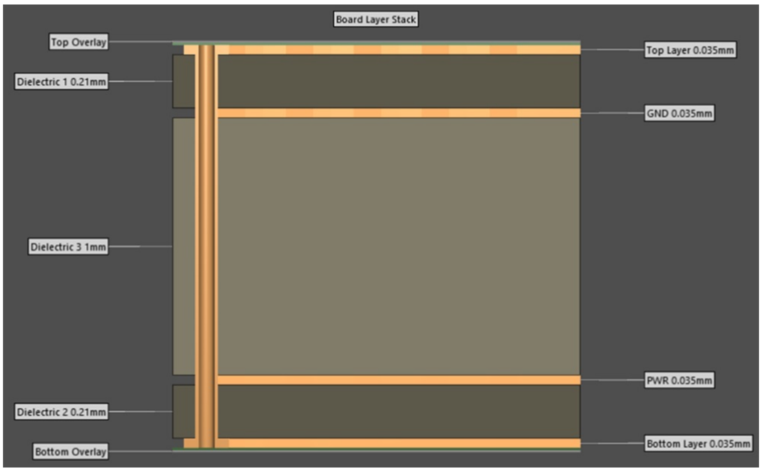


Figure 19. 4-layer PCB configuration



10 Conclusion

Many of the EMC problems and operational pitfalls that impact the design of high-power RF systems can be avoided following the guidelines illustrated in this document. Carefully check signal routing, on which PCB layer the signals are placed. PCB stack-up, placement of components, handling of multiple DC voltages, current return path and via placement must always be an integral part of the board design. The achievement of the required performance is often linked to an optimized PCB layout.

Revision history

Table 4. **Document revision history**

Date	Version	Changes
07-Mar-2025	1	Initial release.
24-Jun-2025	2	Added ST25R501.
01-Mar-2026	3	Added ST25R210. Updated: • Table 2. GND pins connection • Section 4.2: EMI capacitor switching via GPIO pins

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