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## STSPIN32G0x low voltage family layout guidelines



### Introduction

The low voltage **STSPIN32G0x** family's devices are systems-in-package integrating all the circuitry required for a three-phase brushless motor driving application:

- A triple half-bridge gate driver with a current capability of 600 mA (sink and source) and integrated bootstrap diodes.
- A complete power management circuitry composed of a buck converter and an LDO linear regulator provides both 12 V supply voltage for gate drivers and 3.3 V voltage for the MCU and external components.
- Up to three integrated operational amplifiers are available for signal conditioning, such as, current sensing through shunt resistors.
- A comparator with a programmable threshold is integrated to perform the overcurrent protection.
- The integrated MCU (STM32G031 with 64 kB flash and extended temperature range) allows performing field-oriented control, six-step, and other advanced driving algorithms including the speed and position control loop.

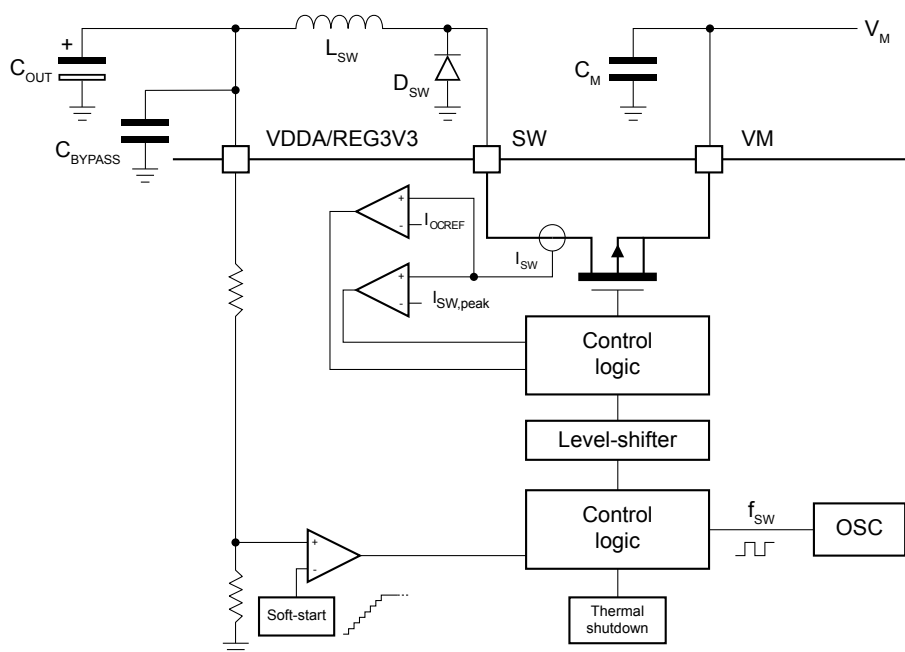
This document provides guidelines for the PCB layout of applications based on these devices.

## 1 Buck regulator and MCU supplies

The step-down buck regulator embedded in the devices is based on a hysteretic control, making it stable in a wide input voltage and load current ranges.

More details about the operation and selection of the external components are available in the dedicated Application Note [AN5128](#).

### Figure 1. Buck regulator block diagram and schematic

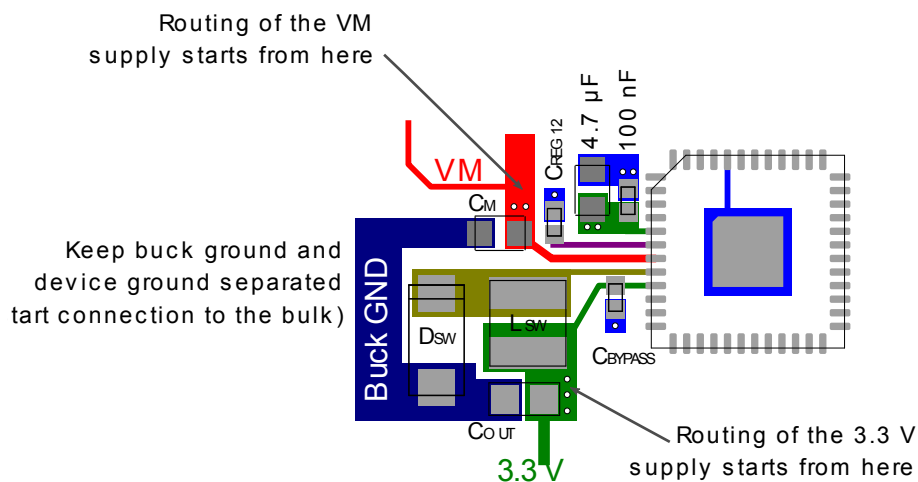


The positioning and layout of the buck regulator's components are critical from both a noise and EMI point of view.

The following is a list of the key points to be considered during the layout of this section:

- A ceramic input capacitor ( $C_M$ ) should be positioned as near as possible to the VM pin.
- Keep the loop area composed of a recirculation diode, inductor ( $L_{SW}$ ), and output capacitor ( $C_{OUT}$ ) as small as possible.
- One 100 nF ceramic bypass capacitor ( $C_{BYPASS}$ ) must be positioned as near as possible to the REG3V3 pin with the ground side directly connected to the device ground. Keep the bypass capacitor on the same side of the device.
- The output capacitor ( $C_{OUT}$ ) must be positioned between the inductor ( $L_{SW}$ ) and bypass capacitor ( $C_{BYPASS}$ ).
- The routing of the 3.3 V supply to other components should start from the output capacitor, before the bypass capacitor ( $C_{BYPASS}$ ).
- It is preferred to separate the ground connection of the output capacitor ( $C_{OUT}$ ) from device ground.
- Connection between bypass capacitors and respective pins must be direct, with no via or other traces in between.

**Figure 2. Buck regulator block layout example**



## 1.1 VDD, VBAT, and VREF+ supplies

All embedded MCU supplies require dedicated ceramic filtering capacitors as below:

- 100 nF + 4.7 μF ceramic capacitors on VDD.
- 100 nF ceramic capacitor on VBAT (STSPIN32G0A1 and STSPIN32G0B1 only).
- 100 nF + 1 μF ceramic capacitors on VREF+ (STSPIN32G0A1 and STSPIN32G0B1 only).

The capacitors must be positioned as near as possible to the respective pin with the ground side directly connected to the device ground. Keep the bypass capacitor on the same side of the device.

## 2 Linear regulator

The regulator requires an output capacitor ( $C_{\text{REG12\_POL}}$ ) making the control loop stable and a 100 nF bypass capacitor ( $C_{\text{REG12}}$ ) providing pulsed currents during gate driver commutations. The bypass capacitor must be placed as near as possible to the REG12 pin and on the same side of the device.

Routing of the 12 V supply to other components must start from the output capacitor avoiding connection between the bypass capacitor and the REG12 pin.

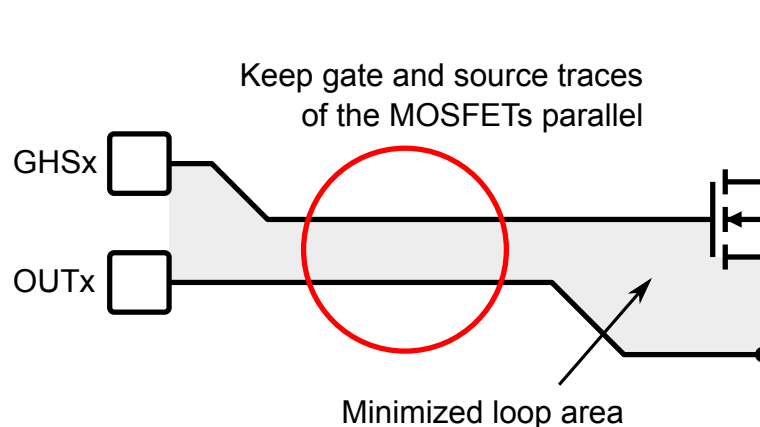
Both the output and bypass capacitor grounds should be directly connected to the device's ground. This ground is the return path of the low-side gate currents and the charging currents of bootstrap capacitors as described in [Section 3.3](#).

## 3 Gate drivers

### 3.1 High-side gate drivers

Connection between high-side gate drivers and gate must be as direct as possible, avoiding, if possible, via holes. The return path of the gate currents is the respective OUTx connection, and it should be parallel to the high-side gate trace. Minimizing this loop reduces EMI radiated emission.

**Figure 3. High-side gate driver layout**



### 3.2 Bootstrap capacitors

Bootstrap capacitors should be positioned as near as possible to the device between the BOOTx and OUTx pins. If possible, keep the bootstrap capacitors on the same side of the device.

If a decoupling resistance between the OUTx pin and high-side MOSFET's source is present, it must be positioned after the bootstrap capacitor.

### 3.3 Low-side gate drivers

Connection between low-side gate drivers and gate must be as direct as possible, avoiding, if possible, via holes. The return path of the gate currents is the device ground, in particular the 12 V regulator ground. Minimizing this loop reduces EMI radiated emission.

In this case, the best approach is having a dedicated layer for the ground layout.

### 3.4 Below-ground and overshoot protection diodes (optional)

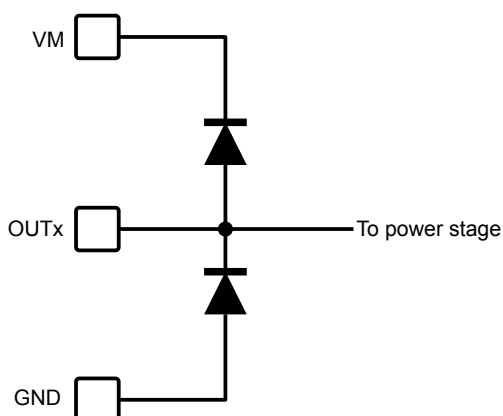
If, for any reason, the power stage output shows below-ground or overshoot ringings violating the absolute rating of the device, some protection diodes on the OUTx pin could be required.

In this case, the diodes should be positioned as near as possible to the pin.

If a decoupling resistance between the OUTx pin and the high-side MOSFET's source is present, it must be positioned after the diodes.

Connect the below-ground protection diodes between the OUTx pin (cathode) and the device's ground (anode) in the most direct way possible. The same for the overshoot protection diodes between the OUTx pin (anode) and VM supply of the device (cathode).

**Figure 4. Protection diodes positioning**



## 4 Power stage

The power stage is a switching circuitry composed by three half-bridges having a high-side and a low-side MOSFET. The high powers managed by the inverter make it particularly sensitive to parasitics introduced by the layout: fast voltage transitions are easily coupled through parasitic capacitance and commutated currents could cause ringing when flowing into parasitic inductance.

Considering the cross section of the board, the capacitive coupling occurs when the switching node's trace overlaps with other traces routed on a different layer. For this reason, it is important to avoid positioning of signals and analog/digital supplies directly below the switching circuitry. The only traces that can overlap with the switching node are the inverter supply bus and the power ground. If more than 2 layers are available, it is possible to route other signals below the switching circuitry putting a power ground shield in the intermediate layer.

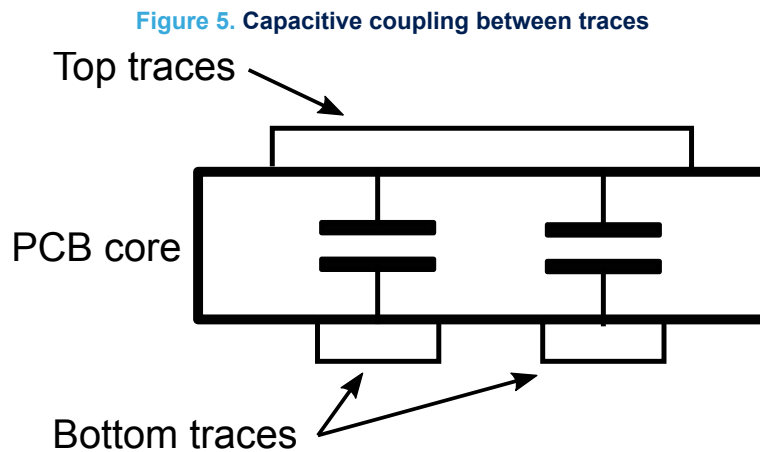
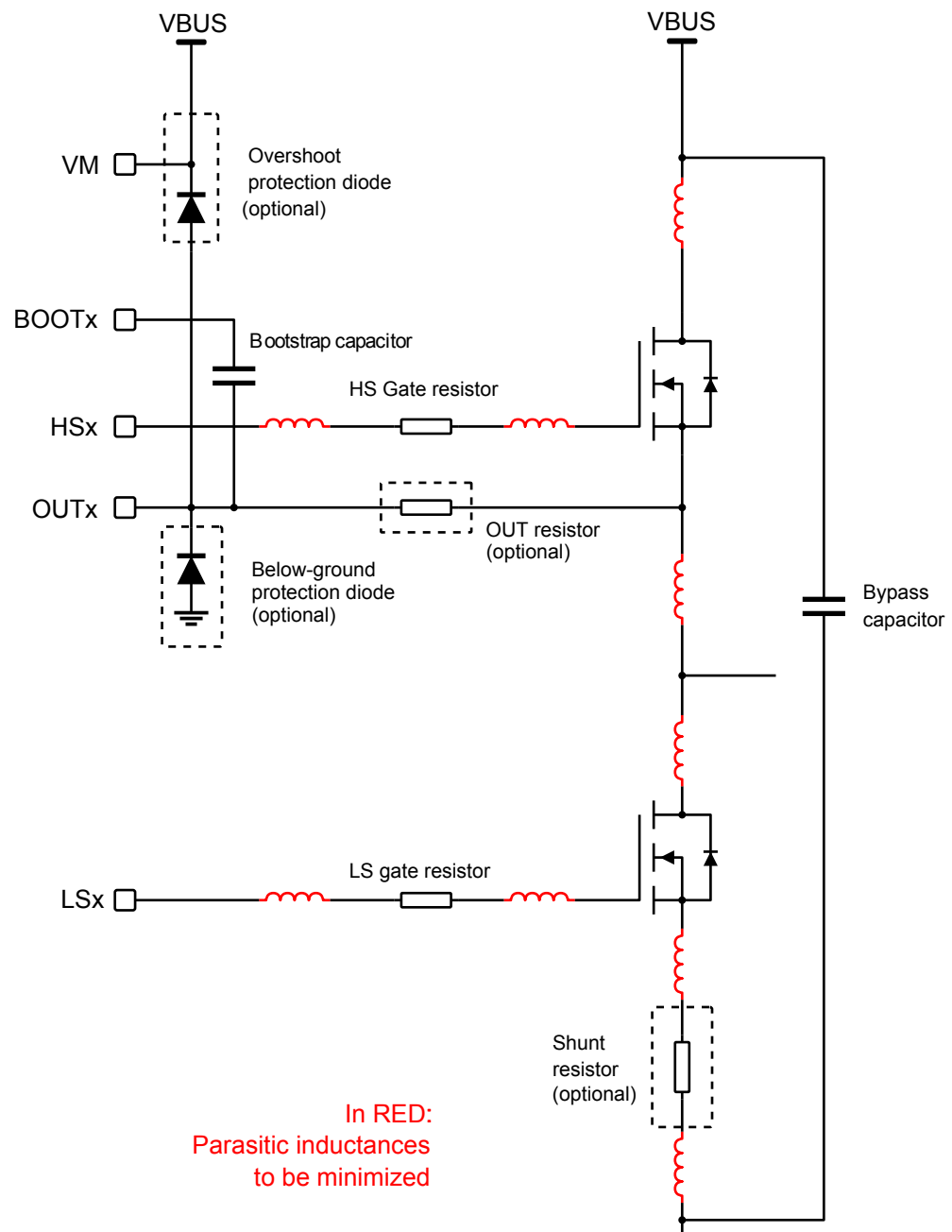


Figure 5 shows the half-bridge schematic with the primary parasitics introduced by connections between the MOSFETs. All these effects should be minimized by making the respective connection as short and wide as possible. Use of vias on these critical paths is not recommended but if not possible to avoid, place multiple vias.

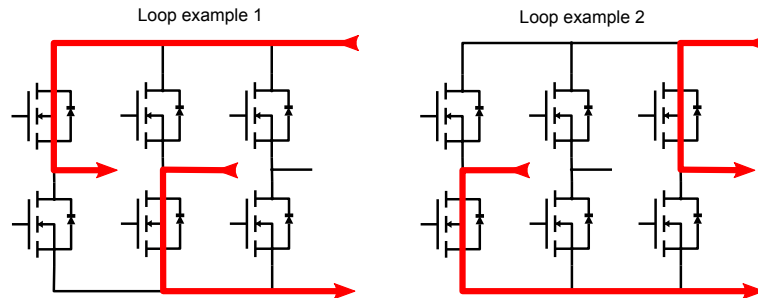
**Figure 6. Half-bridge schematic including primary parasitics**




## 4.1 Current loops

The supply input, the power stage, and the motor phases are part of some high-current loops. In fact, according to the control algorithm, the power stage sources current from the power supply input, distributes it into the motor phases, and closes the loop on the power supply negative lead.

**Figure 7. Current loops in three-phase motor applications**

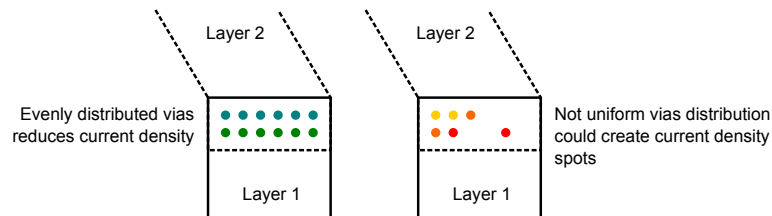


These loops are subject to high switching currents, so it is important to keep their area as small as possible, preventing ringing and radiated EMI.

Guidelines for the layout of these loops are:

- Minimize distances between loop components (high-side and low-side switches, shunt resistors, bulk and bypass capacitors). In this way both loop area and parasitics are minimized.
- Keep the trace size wide (lower parasitics).
- Connection between layers must be performed using multiple vias distributed over the entire width of the trace.
- Take advantage of different layers allowing the return current to flow back to the negative supply lead parallel to the one coming from the positive lead.

**Figure 8. Via positioning for connection between layers**



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## 5 Bulk and bypass capacitors

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In most of the applications a bulk capacitor mitigates the effects of switched currents on the supply inputs providing a fast current source available during load transitions. In fact, the parasitic inductance of the connection cables could limit the supply current during transients.

For this purpose, low ESR parts are recommended. Multiple capacitors in parallel help to achieve high capacitance values reducing the total ESR.

The bulk should be positioned between the supply input and the power stage: the supply line of all the half-bridges must pass through the bulk capacitor to make it effective.

A bypass capacitor of few hundreds of nF should be placed next to each half-bridge filtering high-frequency currents from MOSFETs' commutation.

When ceramic capacitors are selected, particular attention must be paid to the voltage derating factor. The actual capacitance value decreases when the components are biased with a DC voltage, with a derating factor that could reach 50%. For this reason, it is recommended a voltage rating two times the supply voltage that must be filtered.

## 6 Ground layout

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Ground separation is a key point, in particular for high current applications.

Three main grounds should be considered:

1. Device ground (pin 44 and exposed pad): It is the ground reference for the MCU, operational amplifiers, comparators, 12 V regulator, and low-side gate drivers.
2. Buck ground: It is the ground of the buck's output capacitor.
3. Power ground: It is the power stage ground where the inverter current flows.

The connection point of the three grounds is the input bulk capacitor.

The exposed pad of the device should be connected to the ground plane using multiple via holes. This has the main purpose of improving the heat dissipation of the device.

## Revision history

**Table 1. Document revision history**

Date	Version	Changes
10-Feb-2025	1	Initial release.

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