Single channel pyrofuse driver

Introduction

The L9965P / L99BM2P is a single-channel pyrofuse driver that can quickly and reliably break a high-voltage battery line in the event of a short circuit or car crash.

To accomplish this function, the device integrates a dual FET output stage consisting of a high-side and a low-side power MOSFET. The stage is equipped with a closed-loop current feedback and can be configured to deliver controlled firing profiles by programming both current intensity and duration. Moreover, the power stage is able to perform a defined number of auto-retry attempts based on the success or failure of the deployment.

The device embeds a programmable firing logic allowing it to generate the fire trigger from two SPI commands or two digital inputs (FENH/FENL). The digital input triggers are compatible with both level and PWM encoding, supporting 16 kHz and 125 kHz encoded signals.

The device supports an external capacitor as an energy reserve (ER). An internal boost regulator can be used to control the ER cap voltage around a programmable setpoint.

A low-power operation strategy allows minimizing the idle consumption, keeping the device in an ultralow-power state while still performing all the diagnostic sweeps with a programmable periodicity. During such an ultralow-power state, the device is still sensitive to wake up sources to be ready to fire at any time.

Operation in conjunction with the L9965C/L99BM2C companion chip simplifies IC control loops, as many safety mechanisms are already implemented by the L9965C/L99BM2C.

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1 Application scenarios

In case the IC is directly connected to the battery, it is recommended to implement the application circuits shown in Figure 1.

**Figure 1. Application circuit with battery supply**
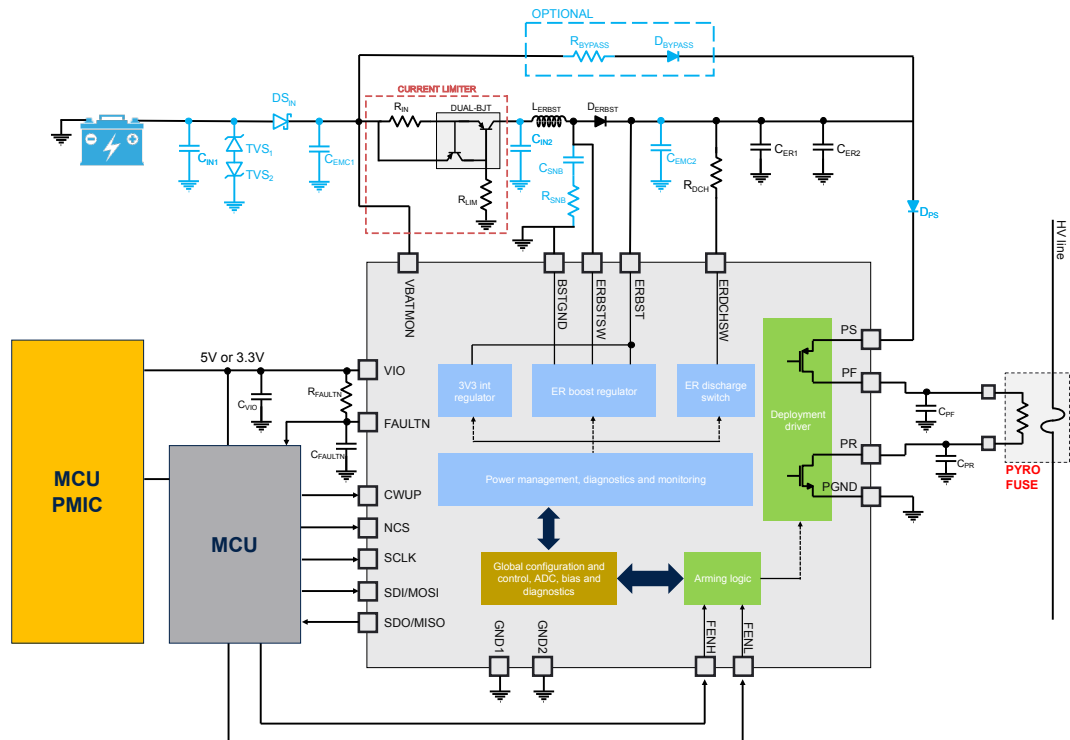
The current limiter circuit has the aim to avoid uncontrolled inrush current from battery towards C_{ER} and could be removed in case the energy source is limited in alternative way. The presence of the feed forward path (D_{BYPASS}/R_{BYPASS}) is only needed in case the device is expected to be able to deploy immediately after power-up, before the BOOST circuit charged the tank capacitor.

If the device is supplied by a DC-DC converter, it is recommended to use the fallowing circuit as shown in Figure 2.

Figure 2. Application circuit with DC-DC converter
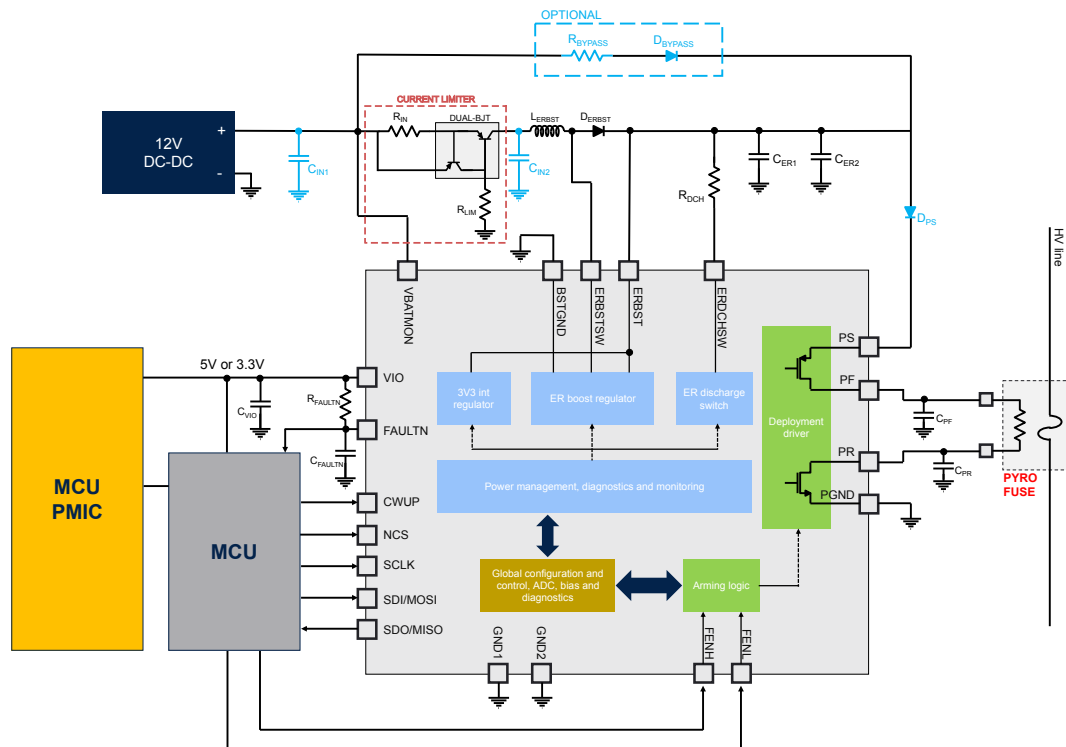
In this scenario the current limiter circuit cannot be mounted if the DC-DC converter has got its own current limitation.

If the ERBST is not needed, the recommended application circuit is the Figure 3.

Figure 3. Application circuit without boost converter
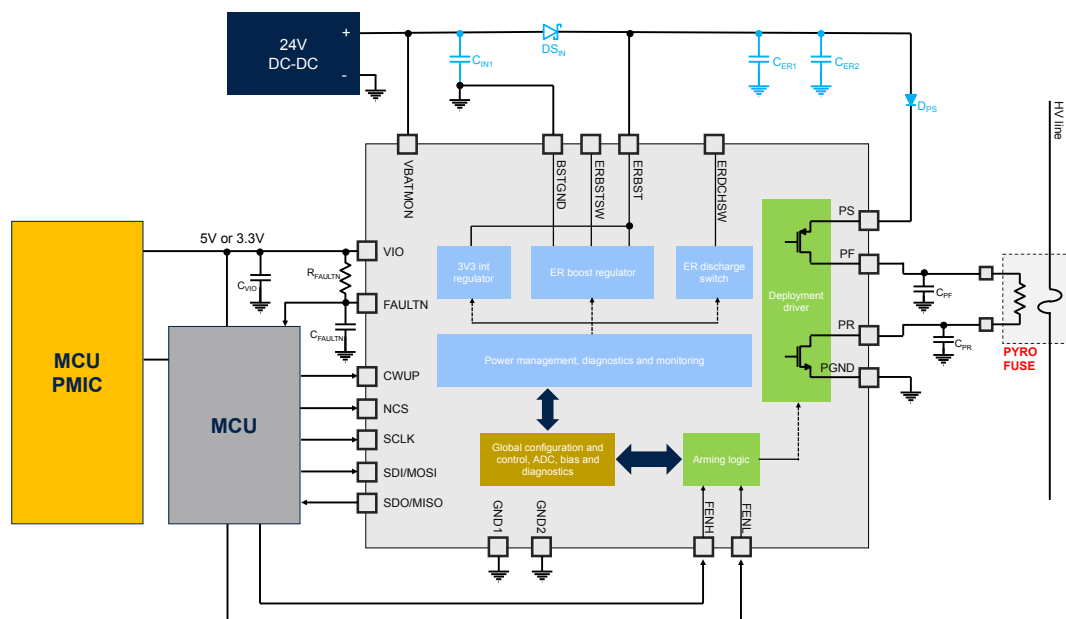
2 External components sizing

2.1 ERBST components

The suggested inductor value for L_{ERBST} is 33 µH ± 20 %, with a maximum DCR of 1.5 Ω. An example is the VLS4020CX-330M-H from TDK.

The diode for D_{ERBST} shall be a Schottky diode and shall sustain a maximum current of 500 mA (input power limitation disabled), with a maximum forward voltage of 1.2 V. An example is the STPS1L40ZFY from STMicroelectronics.

To limit the inrush current from the battery in the PS node during the system power-on and avoid an unwanted trigger of the ERBST overcurrent fault (ERBST_OC bit in the ERBOOST register), a current limiter can be placed before the ERBST branch (L_{ERBST} and D_{ERBST}) and after the VBATMON. In this application can be used a double BJT, as example the ZXTP56060FDBQ.

These are the possible scenarios:

- In normal condition, the first PNP connected to the L_{ERBST} is turned-on and the supply current flows through ERBST, instead, the second PNP turns off through the pull-down resistor.
- Once of target current limit is reached, the second PNP connected to R_{LIM} is turned-on modulating the V_{BE} at the first PNP which keeps the current near to the target.

Figure 4. Inrush current limit
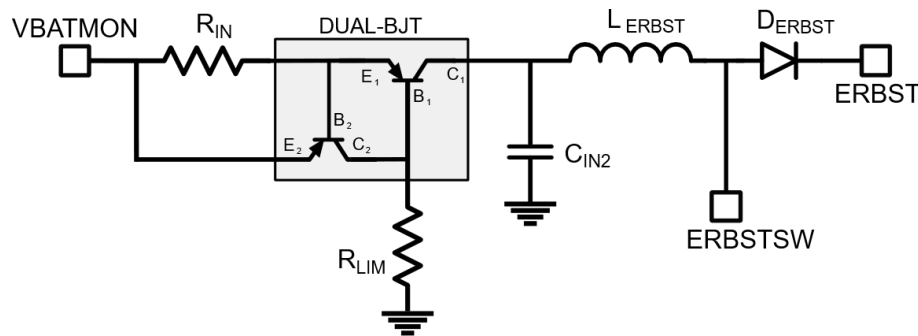
To allow this behavior, it is needed to size R_{IN} and R_{LIM} according to the maximum current desired and the $V_{BE,on}$ of the chosen BJT.

The R_{IN} is sized to avoid reaching the OC threshold, as example considering:

- $I_{ERBST\ PEAK\ LIM\ 0,min}$ = 330 mA → $I_{CE,max}$ = -300 mA
- $V_{BE,on}$ = -0.7 V
- $R_{IN} = V_{BE,on} / I_{CE,max}$ = 2.33 Ω

The R_{LIM} is sized to ensure that second BJT operates in the linear region even at minimum operating battery, as example for the ZXTP56060FDBQ:

- Current gain $h_{FE,min} = I_{C1} / I_{B1}$ = 50
- for I_{C1} ~ 300 mA → $I_{B1,max}$ = 6 mA
- $V_{C2} = V_{B1} = R_{LIM} \times I_{B1,max}$
- and: $V_{C2} = V_{bat,min} + V_{CE2,ON}$

considering: $V_{CE2,ON}$ = - 2V; $V_{bat,min}$ = 6 V; R_{LIM} = 667 Ω

In case an immediate deploy ability is requested after the power up, a feed-forward branch composed of a R_{BYPASS} and D_{BYPASS} can be mounted. The diode is sized to sustain the maximum deployment current I_{DEPLOY}.

The resistance R_{BYPASS} can be sized considering the desired deploy current, as example:

- supposing: I_{DEPLOY} = 1.5 A, V_{batt} = 12 V
- $V_{batt} - V_{bat,min} - V_{DBYPASS} = I_{DEPLOY} \times R_{BYPASS}$
- $R_{BYPASS} = (V_{batt} - V_{bat,min} - V_{DBYPASS}) / I_{DEPLOY}$ = 3.5 Ω

To improve the EMC performance can be added a snubber circuit between the ERBSTSW pin and the BSTGND. The suggested values are: C_{SNB} = 220 pF and R_{SNB} = 10 Ω.

By the way, the values of this snubber, and the related cutoff frequency should be tuned according to the emission performance at the system level.

2.2 Energy reserve capacitor

The minimum value of the energy reserve capacitor must be sized considering the amount of charge that it has to provide during the deployment event.

According to this, the following parameters must be considered:

- Deployment current, I_{DEPLOY}
- Deployment time, t_{DEPLOY}
- Minimum PS voltage, set by the minimum ERBST wake-up threshold or by minimum IC operating voltage
- Voltage drop at tank capacitor terminals, $\Delta V_{DROP,max}$

Regarding the minimum PS voltage, it is considered under the condition of maximum ERBST regulated voltage and minimum ERBST wake-up threshold, to minimize power consumption as much as possible (ERBST switching activity reduced to a minimum).

The formula to size the value of the energy reserve capacitor is the following:

$$C_{min} = \frac{I_{DEPLOY}*t_{DEPLOY}}{\Delta V_{DROP}} \tag{1}$$

The worst case is obtained considering:

- Minimum deployment current, I_{DEPLOY} = 1.5 A
- Maximum deployment time, t_{DEPLOY} = 1.05 ms
- Minimum PS voltage, $V_{ER\_WKUP\_TH0}$ = 16 V
- Minimum PS voltage, $V_{PS,min}$ = 6 V
- Maximum voltage drop, $\Delta V_{DROP,max}$ = $V_{ER\_WKUP\_TH0}$ − $V_{PS,min}$ = 16 V − 6 V = 10 V

So, the minimum value of the energy reserve capacitor can be calculated as:

$$C_{min} = \frac{I_{DEPLOY,min}*t_{DEPLOY,max}}{\Delta V_{DROP,max}} = \frac{1.5A*1.05ms}{10V} \sim 200\mu F \tag{2}$$

This value is calculated considering only the deployment current. If a battery loss scenario must also be considered, the IC consumption has to be included in the calculation. In any case, since I_{BASE_NORM} = 2.4 mA, the main contribution is due to deployment current. To allow multiple deployments, the tank capacitor must be sized accordingly.

For safety reasons, to account for ER capacitor degradation due to temperature and aging, it is recommended to mount two capacitors in parallel, either of the same value or with different sizes.

A typical value of the ER capacitors based on standard deployment profile could be 2 x 330 µF. An example is the EEEFK1V331P capacitor from *Panasonic*.

When the system powers off, to avoid residual charge on the energy reserve capacitor, a passive pull-down path can optionally be mounted. A suggested value of about 1 kΩ is recommended to avoid significant consumption from battery when the system is off. Be careful with the resistor's power rating to avoid unwanted leakage occurring during lifetime.

2.3 Battery filter

Based on customer application, the following additional components may be useful (highlighted in light blue in Figure 1):

- TVS diode to clamp the input voltage (IC AMR is 40 V) and the reverse voltage (-14 V for 12 V system, -26 V for 24 V system)
- DS_{IN} diode to prevent damage from reverse polarity. It is recommended to use a Schottky diode to keep the series voltage drop as low as possible on the battery line.
- Tank capacitors (C_{IN1}, C_{IN2}) after the supply and before the L_{ERBST} to mitigate voltage drops due to current spike.

- A capacitor bank, C_{EMC1} and C_{EMC2}, serves as a filter stage useful for improving EMC performance by filtering noise from the battery and voltage spikes. In a typical application scenario, a range of different value capacitors can be mounted (1 µF, 100 nF, 10 nF, 1 nF).

2.4 Power stage filter

The power stage consists of two power MOSFETs (triggered by two independent paths) connected to the pyrofuse through the PF and PR pins.

In order to improve EMC performance, it is required to add the C_{PF} and C_{PR} capacitors (minimum value 13 nF) on the PF and PR pins.

In a typical application scenario:

- 100 pF and 1 nF capacitors are mounted near the PF and PR pins.
- A TVS diode can be optionally mounted near the PF and PR pins.
- A 100 nF capacitor is mounted near the connector of the pyrofuse element.
  In case the system shall survive to PF and PR shorted to permanently supplied battery line with IC power off, D_{PS} diode can be optionally mounted in series to PS pin to protect the device from back feeding towards the ERCAP.

3 Device configuration

3.1 NVM configuration (write command)

The MCU shall write the following commands to configure the NVM:

1. Write 0x55 in the SPECIAL_KEY register for partial unlock
2. Write 0x33 in the SPECIAL_KEY register for full unlock
3. Write NVM configuration in **CLIENT_NVM_REG_x** registers
4. Write 0x3 in the NVM_OP_CMD register to upload data into the NVM
5. Write 0xAA in the SPECIAL_KEY register for lock restoring, or wait for $t_{CFG\_TIMEOUT}$ expiration for automatic locking.

Every time the NVM is downloaded, the **CLIENT_CONFIG_CRC** bit field is internally written.

Every time the NVM is written, the **NVM_UPLOAD_COUNT** decreases by 1, starting from 0x1F.

3.2 ERBST configuration

By default, the ERBST is disabled.

Together with the enabled bit, there are other bitfields to be configured in the NVM:

- **ERBST_EN** = 1 enables the ERBST regulator
- **ERBST_SET** bitfield selects the regulated voltage between 18 V and 24 V
- **VER_WKUP** bitfield selects the wake up threshold between 16 V and 22 V
- **PIN_LIMIT** = 1 limits the peak input current to 440 mA.

3.3 Load thresholds configuration

When the pyro igniter resistance measurement diagnostic is executed, the result is compared with the low and high thresholds stored in the NVM.

The relationship between the low-resistance threshold and the $V_{RES\_LOW\_TH}$ code is the following:

$$R_{LOW} = \frac{4*(VRES\_LOW\_TH)_{dec}*LSB_0}{I_{PF\_PU}} \tag{3}$$

$$Example: R_{LOW} = \frac{4*(0xF)_{dec}*0.651mV}{40mA} = 1\Omega$$

The relationship between the high-resistance threshold and the $V_{RES\_HIGH\_TH}$ code is the following:

$$R_{HIGH} = \frac{4*(VRES\_HIGH\_TH)_{dec}*LSB_0}{I_{PR\_PD}} \tag{4}$$

$$Example: R_{HIGH} = \frac{4*(0x2E)_{dec}*0.651mV}{40mA} = 3\Omega$$

3.4 Energy reserve capacitor diagnostic

The diagnostic of an energy reserve capacitor is done by estimating its capacitance value and its ESR (equivalent series resistance) value by means of an external R_{DCH} resistor.

The R_{DCH} resistor limits the current that flows inside the IC and it is sized considering a typical diagnostic current of 0.5 A. The value used in simulations is 62 Ω, so the commercially suggested value is 68 Ω.

Considering a typical scenario with 2 x 330 µF, the low capacitance threshold can be set to approximately 400 µF (middle value between 1 x 330 µF and 2 x 330 µF).

The following formula can be used for **ERCAP_C_THR**:

$$C_{LOW}[\mu F] = \frac{("00"\&ERCAP\_C\_THR[7:0]\&"0000")_{dec}*LSB_C}{R_{ERDCHSW}} \tag{5}$$

$$Example: C = \frac{("00"\&0x40\&"0000")_{dec}*25.35\mu F*\Omega}{68\Omega} = 381.74\mu F$$

Taking the EEEFK1V331P capacitor as a reference, the ESR value is 80 mΩ.

Considering a typical scenario with 2 x 330 µF, the high ESR threshold can be set near 160 mΩ.

The following formula can be used for **ERCAP_ESR_THR**:

$$ESR[m\Omega] = (ERCAP\_ESR\_THR[6:0]\&"0000")_{dec}*\frac{LSB_{ESR}*R_{ERDCHSW}}{1000} \tag{6}$$

$$Example: ESR = (0x4\&"0000")_{dec}*\frac{38.52\mu*68\Omega}{1000} = 167.64m\Omega$$

3.5 Deployment configuration

The deployment current is set through the I_DEP_CFG bitfield in the NVM:

1. **I_DEP_CFG** = 00 sets 1.50 A min
2. **I_DEP_CFG** = 01 sets 1.75 A min
3. **I_DEP_CFG** = 10 sets 2.00 A min
4. **I_DEP_CFG** = 11 sets 3.50 A min.

The deployment time is set through the **T_DEP_CFG** bitfield in the NVM.

The relationship between deployment time and **T_DEP_CFG** code is the following:

$$t_{DEPLOY} = (T\_DEP\_CFG)_{dec}*t_{DEPLOY\_RES} \tag{7}$$

$$Example: t_{DEPLOY} = (0x2F)_{dec}*16\mu s = 752\mu s$$

The deployment timer resolution t_{DEPLOY_RES} is affected by an error of ±8.1 %.

The deployment time monitor is set through the **DEP_MON_THR** bitfield in the NVM.

The relationship between deployment timer threshold and **DEP_MON_THR** code is the following:

$$t_{DEP\_MON\_TH} = (DEP\_MON\_THR)_{dec}*t_{DEP\_MON\_TH\_RES} \tag{8}$$

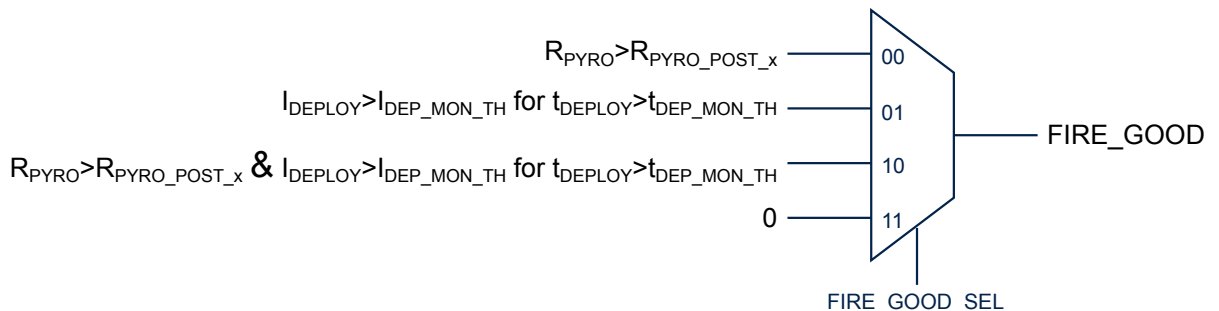$$Example: t_{DEP\_MON\_TH} = (0x16)_{dec}*32\mu s = 704\mu s$$

The **HS_RET_CFG** bitfield sets the number of deploy retries (1, 2, 3 or 4).

The **HS_RET_DLY_CFG** bitfield sets the delay between retries (0.5 ms, 1 ms, 1.5 ms, or 2 ms) in case of deployment by FENH/FENL.

The **FIRE_GOOD_SEL** bitfield selects the source of the FIRE_GOOD signal, as shown in Figure 5.

Figure 5. FIRE_GOOD signal selection

3.6 FAULTN pin masking

It is possible to mask the effects of faults on the FAULTN pin. This is shown in Table 1.

Table 1. FAULTN pin masking summary

Bit	Register	FAULTN masking
ERBST_OV_FAULTN_MSK	CLIENT_NVM_REG_0	ERBST_OV fault masked
PYRO_HIGH_RES_FAULTN_MSK	CLIENT_NVM_REG_1	PYRO_HIGH_RES fault masked
PYRO_LOW_RES_FAULTN_MSK	CLIENT_NVM_REG_1	PYRO_LOW_RES fault masked
ERBSTSW_OT_FAULTN_MSK	CLIENT_NVM_REG_2	ERBST_OT fault masked
ERBSTSW_OC_FAULTN_MSK	CLIENT_NVM_REG_2	ERBST_OC fault masked
ERBST_DLOSS_FAULTN_MSK	CLIENT_NVM_REG_3	ERBST_DLOSS fault masked
PF_FET_FAIL_FAULTN_MSK	CLIENT_NVM_REG_5	PF_FET_FAIL fault masked
PF_PR_STB_STG_FAULTN_MSK	CLIENT_NVM_REG_6	PF_STG, PF_STB, PR_STG and PR_STB faults masked
ERCAP_FAULTN_MSK	CLIENT_NVM_REG_6	ERCAP faults masked
LEAK_LOW_FAULTN_MSK	CLIENT_NVM_REG_6	VRCM_STB_FAIL and VRCM_STG_FAIL faults masked
VRCM_HWSC_FAULTN_MSK	CLIENT_NVM_REG_6	VRCM_HWSC_FAIL fault masked
PF_PR_POST_HWSC_FAULTN_MSK	CLIENT_NVM_REG_6	PF_PR_POST_HWSC_FAIL fault masked
PF_PR_PRE_HWSC_FAULTN_MSK	CLIENT_NVM_REG_6	PF_PR_PRE_HWSC_FAIL fault masked
PR_FET_FAIL_FAULTN_MSK	CLIENT_NVM_REG_8	PF_FET_STG and PF_FET_FAIL faults masked
FENX_TIMEOUT_FAULTN_MSK	CLIENT_NVM_REG_10	FENx_PWM_TIMEOUT and FENx_LEV_TIMEOUT faults masked
FENX_LOW_FREQ_FAULTN_MSK	CLIENT_NVM_REG_10	FENx_LOW_FREQ fault masked
FENX_HIGH_FREQ_FAULTN_MSK	CLIENT_NVM_REG_10	FENx_HIGH_FREQ fault masked
PS_OV_FAULTN_MSK	CLIENT_NVM_REG_11	PS_OV fault masked

3.7 Deployment inhibition masking

It is possible to mask the effects of faults on the fire inhibition. This is shown in Table 2.

Table 2. Deployment inhibition masking summary

Bit	Register	Deployment inhibition masking
ERBST_OV_FIRE_MSK	CLIENT_NVM_REG_0	Inhibition from ERBST_OV masked
PF_FET_FAIL_FIRE_MSK	CLIENT_NVM_REG_7 q	Inhibition from PF_FET_STG and PF_FET_FAIL masked
PR_FET_FAIL_FIRE_MSK	CLIENT_NVM_REG_8	Inhibition from PR_FET_STB and PR_FET_FAIL masked
GND_LOSS_BSTGND_MSK	CLIENT_NVM_REG_9	Inhibition from BSTGND_LOSS masked
PS_OV_FIRE_MSK	INTERNAL_CFG	Inhibition from PS_OV masked

3.8 Device configuration example

3.8.1 Example of non-volatile memory (NVM) configuration

An example of how the non-volatile memory can be configured is shown in Table 3. The following configuration is referred to the application scenario in Figure 1.

Table 3. NVM configuration example

Register name	Address	Data	Notes
SPECIAL_KEY	0x30	0x055	0x55 = partial unlock
SPECIAL_KEY	0x30	0x033	0x33 = full unlock
CLIENT_NVM_REG_0	0x20	0x077	ERBST_OV_FIRE_MSK = 0 (no fire mask) ERBST_OV_FAULTN_MSK = 0 (no FAULTN mask) FENL_PU_PD = 0 (pull-up enabled) FENH_PU_PD = 1 (pull-down enabled) FENL_FREQ = 1 (16 kHz) FENH_FREQ = 1 (16 kHz) FENL_LEVEL = 0 (deploy trigger: low level if FENL_MODE = 0, 25 % duty cycle if FENL_MODE = 1) FENH_LEVEL = 1 (deploy trigger: high level if FENH_MODE = 0, 75 % duty cycle if FENH_MODE = 1) FENL_EN = 1 (FENL decoded enabled) FENH_EN = 1 (FENH decoded enabled)
CLIENT_NVM_REG_1	0x21	0x1C5	FENX_FAULT_PERIOD = 01 (8 periods filter if FENx_MODE = 1) FENX_DEGLITCH = 11 (1280 us filter if FENx_MODE = 0) PYRO_HIGH_RES_FAULTN_MSK = 0 (no FAULTN mask) PYRO_LOW_RES_FAULTN_MSK = 0 (no FAULTN mask) I_DEP_CFG = 01 (1.75 A deployment current) FENX_DLY_CFG = 01 (2 ms deploy trigger delay)
CLIENT_NVM_REG_2	0x22	0x00F	ERBSTSW_OT_FAULTN_MSK = 0 (no FAULTN mask) ERBSTSW_OC_FAULTN_MSK = 0 (no FAULTN mask) VRES_LOW_TH = 0xF (equivalent resistance = 1 Ω)
CLIENT_NVM_REG_3	0x23	0x35C	HS_RET_CFG = 0x3 (4 deploy retries) VRES_HIGH_TH = 0x2E (equivalent resistance = 3 Ω) ERBST_DLOSS_FAULTN_MSK = 0 (no FAULTN mask)
CLIENT_NVM_REG_4	0x24	0x1F6	VRES_THR_POST_SEL = 0 (pyrofuse resistance after deployment equal to 99 Ω) PYRO_RES_EN = 1 (cyclic pyrofuse res meas enabled) LEAK_EN = 1 (cyclic VRCM and leakage test enabled) ADC_HWSC_EN = 1 (cyclic HWSC enabled) FET_EN = 1 (cyclic FETs tests enabled) ER_CAP_EN = 1 (cyclic ER cap diag enabled) DIAG_ROUTINE_PERIOD = 01 (300 ms diagnostic period) HS_RET_DLY_CFG = 10 (1.5 ms between deploy retries)
CLIENT_NVM_REG_5	0x25	0x216	FET_NCYCLE = 10 (16 cycles as periodicity) PYRO_RES_NCYCLE = 00 (1 cycle as periodicity) PF_FET_FAIL_FAULTN_MSK = 0 (no FAULTN mask)

Register name	Address	Data	Notes
			DEP_MON_THR = 0x16 (22*32 = 704 us as deploy timer threshold for fire good signal)
CLIENT_NVM_REG_6	0x26	0x301	ER_CAP_NCYCLE = 11 (64 cycles as periodicity)
			PF_PR_STB_STG_FAULTN_MSK = 0 (no FAULTN mask)
			ERCAP_FAULTN_MSK = 0 (no FAULTN mask)
			LEAK_LOW_FAULTN_MSK = 0 (no FAULTN mask)
			VRCM_HWSC_FAULTN_MSK = 0 (no FAULTN mask)
			PF_PR_POST_HWSC_FAULTN_MSK = 0 (no FAULTN mask)
			PF_PR_PRE_HWSC_FAULTN_MSK = 0 (no FAULTN mask)
			ADC_HWSC_NCYLE = 01 (4 cycles as periodicity)
CLIENT_NVM_REG_7	0x27	0x02F	PF_FET_FAIL_FIRE_MSK = 0 (no FAULTN mask)
			LEAK_NCYCLE = 00 (1 cycle as periodicity)
			T_DEP_CFG = 0x2F (47*16 = 752 us deployment time)
CLIENT_NVM_REG_8	0x28	0x134	VER_WKUP = 100 (20 V as wake-up threshold)
			ERBST_SET = 110 (24 V as target threshold)
			PIN_LIMIT = 1 (input limitation enabled)
			PR_FET_FAIL_FIRE_MSK = 0 (no fire mask)
			PR_FET_FAIL_FAULTN_MSK = 0 (no FAULTN mask)
CLIENT_NVM_REG_9	0x29	0x140	GND_LOSS_BSTGND_MSK = 0 (no FAULTN mask)
			ERBST_EN = 1 (ERBST enabled)
			ERCAP_C_THR = 0x40 (equivalent to 382 uF)
CLIENT_NVM_REG_10	0x2A	0x004	FENX_TIMEOUT_FAULTN_MSK = 0 (no FAULTN mask)
			FENX_LOW_FREQ_FAULTN_MSK = 0 (no FAULTN mask)
			FENX_HIGH_FREQ_FAULTN_MSK = 0 (no FAULTN mask)
			ERCAP_ESR_THR = 0x4 (equivalent to 168 mΩ)
CLIENT_NVM_REG_11	0x2B	0x004	NVM_UPLOAD_COUNT (read-only content)
			FAULTN_DIS = 0 (FAULTN enabled)
			FIRE_GOOD_SEL = 01 (fire good set if deployment current exceeds threshold for longer than deploy timer threshold)
			PS_OV_FAULTN_MSK = 0 (no FAULTN mask)
CLIENT_NVM_REG_12	0x2C	-	CLIENT_CONFIG_CRC (read-only content)
NVM_OP_CMD	0x31	0x003	NVM upload and download
SPECIAL_KEY	0x30	0x0AA	0xAA = lock

3.8.2 Example of volatile memory configuration

An example of how the volatile memory can be configured is shown in Table 4.

Table 4. VM configuration example

Register name	Address	Data	Notes
CRC	0x07	0x000	NVM_CRC_FAIL_MSK = 0 (deploy inhibition and FAULTN assertion in case of NVM fail) CYC_CRC_DIS = 0 (cyclic CRC checks enabled)
INTERNAL_CFG	0x15	0x004	OSC_SS_EN = 1 (spread spectrum enabled) PR_PD_DIS = 0 (pull-down on PR enabled) PS_OV_FIRE_MSK = 0 (no fire mask)
LEVEL MODE (FENH_MODE = FENL_MODE = 0)			
FENH_L_CONFIG	0x03	0x000	FENL_MODE = 0 (FENL level based decoding) FENH_MODE = 0 (FENH level based decoding)
FAULT_DIAG_CONFIG	0x02	0x00D	FENL_INT_CHECK_EN = 1 (FENL integrity checks enabled when in level mode) FENH_INT_CHECK_EN = 1 (FENH integrity checks enabled when in level mode) FAULTN_FORCE = 0 (FAULTN forced high) FAULTN_CYCLIC_PULSE = 1 (FAULTN cyclic pulses enabled)
PWM MODE (FENH_MODE = FENL_MODE = 1)			
FENH_L_CONFIG	0x03	0x003	FENL_MODE = 1 (FENL PWM based decoding) FENH_MODE = 1 (FENH PWM based decoding)
FAULT_DIAG_CONFIG	0x02	0x001	FENL_INT_CHECK_EN = 0 (PWM mode) FENH_INT_CHECK_EN = 0 (PWM mode) FAULTN_FORCE = 0 (FAULTN forced high) FAULTN_CYCLIC_PULSE = 1 (FAULTN cyclic pulses enabled)

4 Device check

The user shall check the status of the IC by reading the following registers:

- BMS_ID, CHIP_ID and SPI_STATUS registers to check the integrity of SPI communication
- INTERNAL_STATUS register to check wake-up source and internal fails
- ERBOOST register to check the status of the ERBST regulator
- TEMPERATURE register to read the internal temperature of the IC.

The formula to convert the TEMPERATURE_CODE bitfield is the following:

$$T_J[°C] = 1.74192 * TEMPERATURE\_CODE - 89.988 \tag{9}$$

$$Example: T_J[°C] = 1.74192 * (0x40)_{dec} - 89.988 = 21.49$$

The error associated with the temperature measurement is ±10 ℃ (T_{J_ERR}).

5 Diagnostics

5.1 Available diagnostics

5.1.1 ABIST

The ABIST checks the analog comparators. In cyclic diagnostics, it is not possible to disable the ABIST, so it runs at every cycle. In case of fault, then ABIST_FAIL = 1.

5.1.2 Hardware self-check (HSWC)

The HWSC checks the integrity of PF-PR pre-deployment path, PF-PR post-deployment path, and VRCM path.

In case of fault, then respectively PF_PR_PRE_HWSC_FAIL = 1, PF_PR_POST_HWSC_FAIL = 1 and/or VRCM_HWSC_FAIL = 1.

5.1.3 Voltage regulator current monitor (VRCM) check

The VRCM is checked in two steps:

1. The I_{PF_PU} is enabled and the VRCM is connected to the PF pin. If the VRCM works properly, then VRCM_STB_FAIL = 0, otherwise VRCM_STB_FAIL = 1 (see Figure 6).

Figure 6. VRCM check: sink current
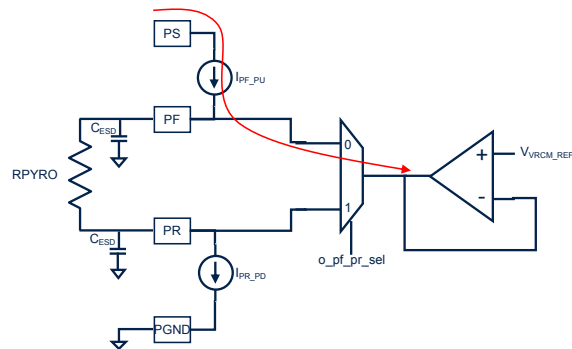
2. The I_{PR_PD} is enabled and the VRCM is connected to the PR pin. If the VRCM works properly, then VRCM_STG_FAIL = 0, otherwise VRCM_STG_FAIL = 1 (see Figure 7).

Figure 7. VRCM check: source current
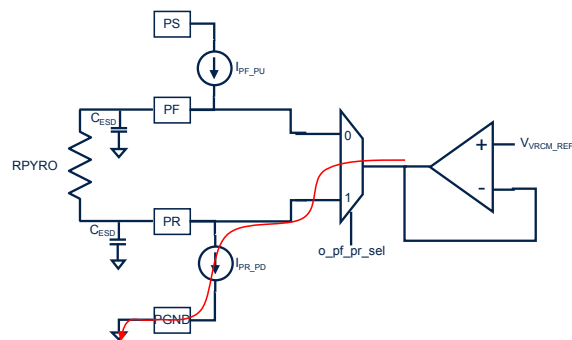
The active pull-down connected to the PR pin ($I_{ACT\_PD\_PR}$) is automatically disabled during this check.

5.1.4 Pyro outputs leakage test

The pyro outputs leakage test checks that no leakages are present on the PF and PR pins.

It works in two steps:

1. The VRCM is connected to PF pin
   a. If there is a leakage to the battery, then PF_STB = 1 (see Figure 8)

Figure 8. PF short to battery (PF STB)
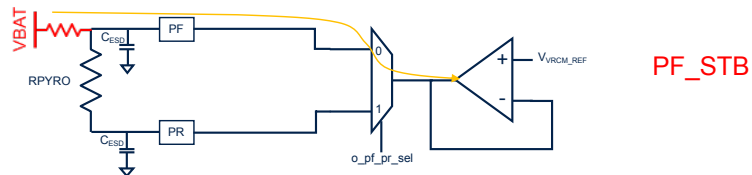
   b. If there is a leakage to the ground, then PF_STG = 1 (see Figure 9)

Figure 9. PF short to ground (PF STG)
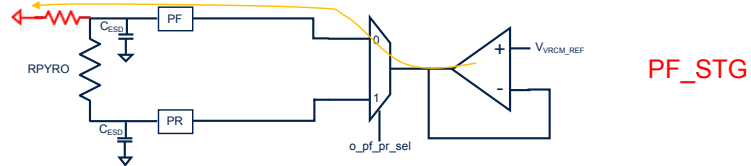
2. The VRCM is connected to the PR pin.
   a. If there is a leakage to the battery, then PR_STB = 1 (see Figure 10)

Figure 10. PR short to battery (PR STB)
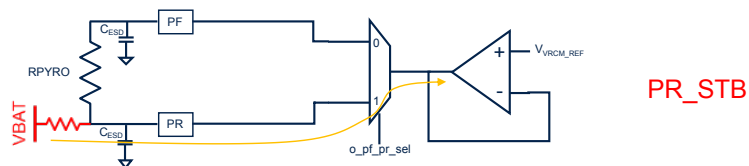
   b. If there is a leakage to the ground, then PR_STG = 1 (see Figure 11)

Figure 11. PR short to ground (PR STG)
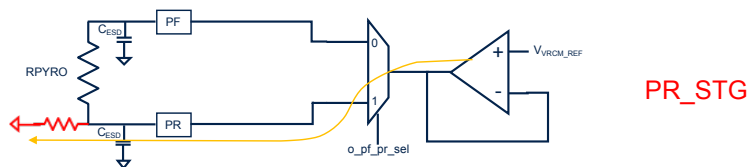
The active pull-down connected to the PR pin ($I_{ACT\_PD\_PR}$) is automatically disabled during this check.

5.1.5 Pyro igniter resistance measurement

Both I_{PF_PU} and I_{PR_PD} are enabled, and the I_{PF_PU} current flows in the external load generating a differential voltage across the load that is measured by the internal ADC (see Figure 12).

Figure 12. Load resistance measurement
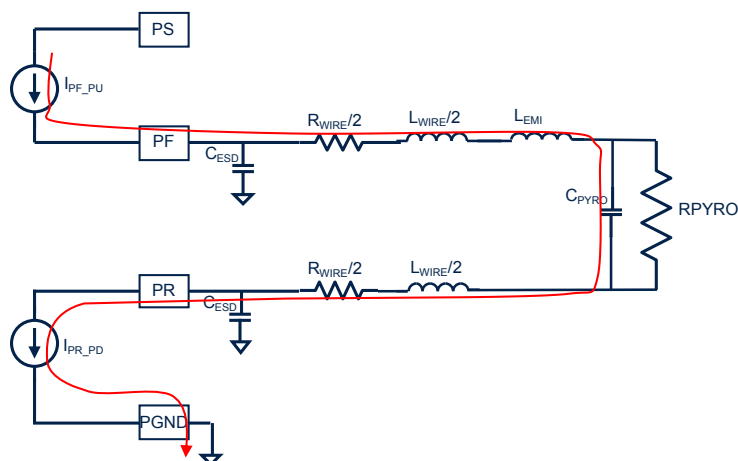
The result of the pre-deployment resistance measurement is stored in the RES_MEAS_PRE register and it is compared with the two thresholds stored in the $V_{RES\_LOW\_TH}$ and $V_{RES\_HIGH\_TH}$ bitfields.

- If the result is below the low threshold, then PYRO_LOW_RES = 1
- If the result is above the high threshold, then PYRO_HIGH_RES = 1.

Formula for the equivalent load resistance pre-deployment:

$$R_{MEAS\_PRE\_DEP} = \frac{0.651mV * RES\_MEAS\_PRE}{40mA} \tag{10}$$

The result of the post-deployment resistance measurement is stored in the RES_MEAS_POST register and it is compared with the $V_{RES\_THR\_POST}$ threshold, selectable between 99 Ω ($V_{RES\_THR\_POST\_SEL}$ = 0) and 49 Ω ($V_{RES\_THR\_POST\_SEL}$ = 1).

Formula for the equivalent load resistance post-deployment:

$$R_{MEAS\_POST\_DEP} = \frac{10.69mV * RES\_MEAS\_POST}{40mA} \tag{11}$$

The active pull-down connected to the PR pin ($I_{ACT\_PD\_PR}$) is automatically disabled during this check.

The error associated with the resistance measurement is ±8 % (ERR_{TOT_PRM}) for both the pre-deployment and post-deployment measurements.

5.1.6 Pyro deployment FETs test

The pyro deployment FETs test checks the integrity of the power MOSFETs.

It works in two steps:

1. The VRCM is connected to the PF pin and the HS pMOS is turned-on. If all works correctly, then PF_FET_STB = 1.

Figure 13. HS FET test
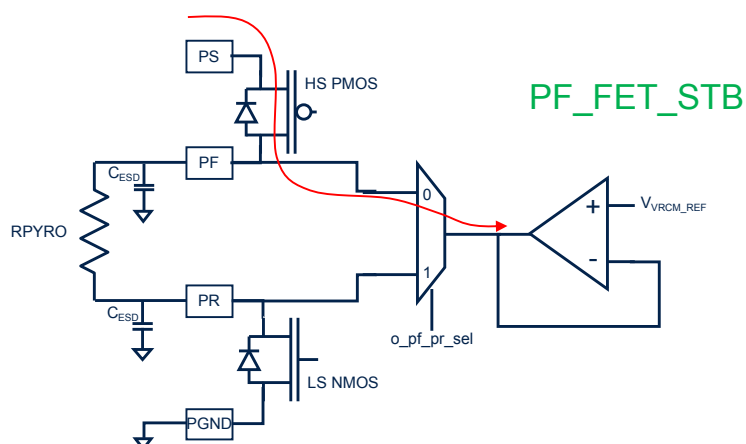
2. The VRCM is connected to the PR pin and the LS nMOS is turned-on. If all works correctly, then PR_FET_STG = 1.

Figure 14. LS FET test
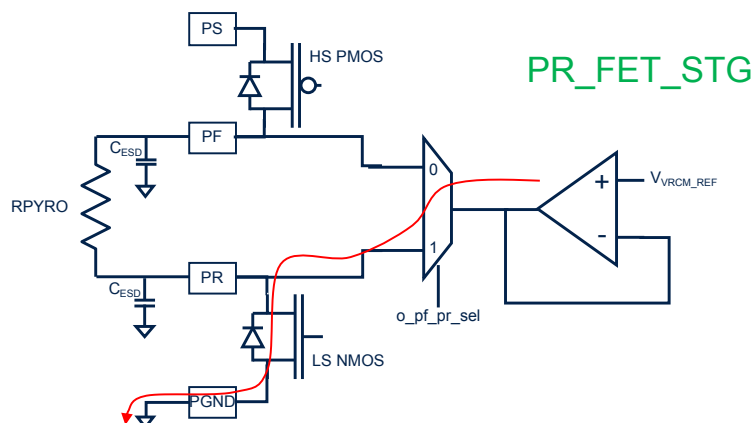
The active pull-down connected to the PR pin ($I_{ACT\_PD\_PR}$) is automatically disabled during this check.

The Table 5 summarizes the possible faults.

Table 5. FETs test faults

Figure	Fault
PF_FET_STG	If the VRCM current is above the $I_{LEAK\_SOURCE\_TH}$ threshold for $t > t_{FET\_TEST\_FLT}$, then PF_FET_STG = 1.
PR_FET_STB	If the VRCM current does not reach the $I_{LEAK\_SINK\_TH}$ threshold, after $t_{FET\_TEST\_TO}$ the HS FET is turned off and PF_FET_FAIL = 1.
PF_FET_FAIL	If the VRCM current is above $I_{LEAK\_SINK\_TH}$ threshold for $t > t_{FET\_TEST\_FLT}$, then PR_FET_STB = 1.
PR_FET_FAIL	If the VRCM current does not reach the $I_{LEAK\_SOURCE\_TH}$ threshold, after $t_{FET\_TEST\_TO}$ the LS FET is turned off and PR_FET_FAIL = 1.

5.1.7 ER capacitor diagnostic

The ER capacitor diagnostic measures the capacitance and the ESR of the ER capacitor.

The value of capacitance is stored in ERCAP_DIAG_CAP_READ_0 (LSB) and ERCAP_DIAG_CAP_READ_1 (MSB) registers, instead the value of ESR is stored in ERCAP_DIAG_ESR_READ_0 (LSB) and ERCAP_DIAG_ESR_READ_1 (MSB) registers.

The formula to convert the CAP_VALUE code in the capacitance value is the following:

$$C[\mu F] = \frac{(CAP\_VALUE\_MSB \& CAP\_VALUE\_LSB)_{dec} * LSB_C}{R_{ERDCHSW}} \tag{12}$$

$$Example: C = \frac{(0x1 \& 0x23E)_{dec} * 25.35\mu F * \Omega}{68\Omega} = 595.725\mu F$$

If the measured value stored in CAP_VALUE is lower than the threshold set in ERCAP_C_THR, the ERCAP_LOW_C fault flag is set in the ERCAP register.

The formula to convert the ESR_VALUE code in the ESR value is the following:

$$ESR[m\Omega] = (ESR\_VALUE\_MSB \ \& \ ESR\_VALUE\_LSB)_{dec} * \frac{LSB_{ESR} * R_{ERDCHSW}}{1000} \tag{13}$$

$$Example: ESR = (0x4 \& 0x19)_{dec} * \frac{38.52\mu * 68\Omega}{1000} = 49.768m\Omega$$

If the measured value in ESR_VALUE is higher than the threshold set in ERCAP_ESR_THR bit field, the ERCAP_HIGH_ESR fault flag is set in the ERCAP register.

- The accuracy of capacitance measurement is ±15 %.
- The accuracy of ESR measurement is ±50 mΩ.

5.2 On-demand diagnostics

The diagnostics can be requested on-demand using the DIAG_CMD register: there is a bit to enable each diagnostic (see Table 6), then the diagnostics start when the DIAG_START bit is written to "1".

Table 6. On-demand diagnostic bits

Diagnostic	Enable bit
Analog built-in self-test	ABIST
Analog-to-digital converter hardware self-check	ADC_HWSC
VRCM check and pyro output leakage test	VRCM_LEAK_TEST
Pyro igniter resistance measurement	PYRO_RES
Pyro deployment FETs test	FET_TEST
ER capacitor diagnostic	ER_CAP

If the on-demand diagnostic is running, then SPI_DIAG_RUNNING = 1. When the on-demand diagnostic is completed, then SPI_DIAG_END = 1.

If needed, the active pull-down connected to PR pin ($I_{ACT\_PD\_PR}$) can be disabled by setting PR_PD_DIS = 1.

5.3 Cyclic diagnostics

The diagnostics can be run cyclically by setting the proper bitfields in thr NVM (see Table 7).

Table 7. Cyclic diagnostic configuration

Diagnostic	Enable bit	Periodicity bit field
ADC hardware self-check	ADC_HWSC_EN	ADC_HWSC_NCYCLE
VRCM check and pro output leakage test	LEAK_EN	LEAK_NCYCLE
Pyro igniter resistance measurement	PYRO_RES_EN	PYRO_RES_NCYCLE
Pyro deployment FETs test	FET_EN	FET_NCYCLE
ER capacitor diagnostic	ER_CAP_EN	ER_CAP_NCYCLE

The period of a cyclic diagnostic routine is set by DIAG_ROUTINE_PERIOD bit field (between 100 ms, 300 ms, 500 ms and 700 ms).

When NCYCLE bitfield is different from 1, the diagnostic is executed with the periodicity set by the bitfield itself. For example, if NCYCLE = 4, the diagnostic runs at the fourth cycle.

If the cyclic diagnostic is running, then CYC_DIAG_RUNNING = 1. The number of cycles is reported in the CYC_DIAG_NCYCLE bitfield.

If needed, the active pull-down connected to the PR pin ($I_{ACT\_PD\_PR}$) can be disabled by setting PR_PD_DIS = 1.

5.4 Diagnostics routine sequence

The routine sequence followed by diagnostics both in on-demand diagnostic and in cyclic diagnostic is shown in Figure 15.

Figure 15. Diagnostics routine sequence

1=ERBST, 2=PF
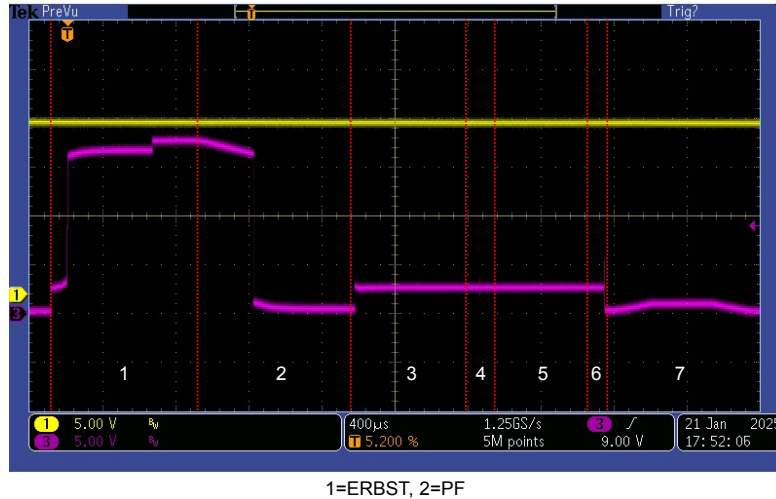
1. VRCM STB test:
   a. VRCM connected to PF
   b. I_{PF_PU} turned on
   c. VRCM disconnected from PF
2. VRCM STB test:
   a. VRCM connected to PR
   b. I_{PF_PU} turned off
   c. I_{PR_PD} turned on
3. LS leakage test:
   a. VRCM just connected to PR
   b. I_{PR_PD} turned off
4. LS FET test:
   a. VRCM just connected to PR
   b. LS FET turned on for $t_{FET\_TEST\_FLT}$
5. HS leakage test:
   a. VRCM connected to PF
6. HS FET test:
   a. VRCM just connected to PF
   b. HS FET turned on for $t_{FET\_TEST\_FLT}$
7. Resistance measurement:
   a. VRCM disconnected from PF
   b. I_{PF_PU} turned on
   c. I_{PR_PD} turned on

5.5 Diagnostics check

The status bits of diagnostics are summarized in Table 8.

Table 8. Diagnostics check

Diagnostic	Status bit	Register	Description
ABIST	ABIST_FAIL	INTERNAL_STATUS	Fail of ABIST
ADC HWSC	PF_PR_PRE_HWSC_FAIL	DEPLOY_DIAG_STATUS_1	Fail of PF-PR pre-deployment ADC HWSC
	PF_PR_POST_HWSC_FAIL	DEPLOY_DIAG_STATUS_1	Fail of PF-PR post-deployment ADC HWSC
	VRCM_HWSC_FAIL	DEPLOY_DIAG_STATUS_1	Fail of VRCM ADC HWSC
VRCM check	VRCM_STB_FAIL	DEPLOY_DIAG_STATUS_0	Fail of STB check
	VRCM_STG_FAIL	DEPLOY_DIAG_STATUS_0	Fail of STG check
Leakage Test	PF_STG	DEPLOY_DIAG_STATUS_0	PF leakage vs ground
	PF_STB	DEPLOY_DIAG_STATUS_0	PF leakage vs battery
	PR_STG	DEPLOY_DIAG_STATUS_0	PR leakage vs ground
	PR_STB	DEPLOY_DIAG_STATUS_0	PR leakage vs battery
Res Meas	PYRO_LOW_RES	DEPLOY_DIAG_STATUS_1	Low resistance value
	PYRO_HIGH_RES	DEPLOY_DIAG_STATUS_1	High resistance value
FETs Test	PF_FET_STG	DEPLOY_DIAG_STATUS_0	HS FET shorted to ground
	PF_FET_FAIL	DEPLOY_DIAG_STATUS_0	HS FET test fail (timeout)
	PR_FET_STB	DEPLOY_DIAG_STATUS_0	LS FET shorted to battery
	PR_FET_FAIL	DEPLOY_DIAG_STATUS_0	LS FET test fail (timeout)
ER Cap Diag	ECAP_LOW_C	ERCAP	Low capacitance
	ERCAP_HIGH_ESR	ERCAP	High ESR
	ERCAP_OUT_OF_RANGE	ERCAP	Cap or ESR out of range
	ERCAP_DIAG_END_TO	ERCAP	ER cap diag fail (timeout)

5.6 FAULTN check

The FAULTN line shall be checked for safety reasons, and it can be done:

- Automatically:
  - In low-power mode, at each CWUP low-to-high transition, the IC generates a pulse.
  - In full-power mode, setting FAULTN_CYCLIC_PULSE = 1, the IC generates a pulse every t$_{FAULT\_PERIOD}$.
- On-demand using FAULTN_FORCE bit: FAULTN_FORCE = 1 forces FAULTN low.

The MCU shall monitor the coherence between the FAULTN pin and its echo bit (FAULTN_ECHO) in GSW of SPI. The FAULTN output can be disabled by setting **FAULTN_DIS** = 1.

5.7 On-demand ADC request

When not used in diagnostics, the ADC can be used to measure main voltages on-demand.

According to the AMUX_CONF setting, the following analog-to-digital voltage conversions can be requested from the IC: PS, PF, PR, PF-PR (pre-deployment), PF-PR (post-deployment), ERBST and VRCM.

To start the conversion process, the user shall set ADC_CONV_CMD = 1.

During the conversion, the IC sets ADC_BUSY = 1 and then, once finished, ADC_CONV_RDY = 1.

The result is stored in the ADC_CONVERSION bitfield of the ADC_CONV_RESULT register.

Based on the voltage conversion required, the input range and the related LSB change, three formulas are available:

1. Formula for PF-PR pre-deployment measurement:

$$V_{MEAS} = 0.651mV*(\text{ADC\_CONVERSION})_{dec} \tag{14}$$

2. Formula for PF-PR post-deployment and VRCM measurements:

$$V_{MEAS} = 10.69mV*(\text{ADC\_CONVERSION})_{dec} \tag{15}$$

3. Formula for PS, PF, PR and ERBST measurements:

$$V_{MEAS} = 55.27mV*(\text{ADC\_CONVERSION})_{dec} \tag{16}$$

The ADC result is affected by error gain (max ±2 %) and by offset (max ±5 LSB).

6 Deployment

6.1 Deployment via FENH and FENL

The FENx decoders shall be enabled in the NVM by setting FENL_EN = 1 and FENH_EN = 1.

The deployment can be triggered in two ways based on the FENx_MODE bit selection:

1. FENL_MODE = FENH_MODE = 0: level mode
    Example: with **FENL_LEVEL** = 0 and **FENH_LEVEL** = 1, a low signal on FENL and a high signal on FENH trigger the deployment.
2. FENL_MODE = FENH_MODE = 1: PWM mode

Example: **FENL_LEVEL** = 0 and **FENH_LEVEL** = 1, a PWM signal with 25 % duty cycle on FENL and a PWM signal with a 75 % duty cycle on FENH trigger the deployment.

FENL_FREQ = **FENH_FREQ** = 1 sets the PWM frequency to 16 kHz.

If FENx_MODE = 0 (level mode):

*   **FENL_PU_PD** and **FENH_PU_PD** bits shall be set accordingly
*   **FENX_DEGLITCH** sets the deglitch filter on FENH and FENL signals
*   FENL_INT_CHECK_EN = 1 and FENH_INT_CHECK_EN = 1 enables the integrity check on FENL and FENH pins respectively.
    Two cases are possible:

    1. CWUP always high (full-power mode).
        Every t_{FAULTN_PERIOD} the IC generates a t_{FAULTN_PULSE} pulse on FAULTN pin and waits for a pulse on FENL and FENH pins before t_{FENx_PERIOD} expires.
    2. Cyclic CWUP (low-power mode).

At each CWUP rising edge, the IC generates a t_{FAULTN_PULSE} pulse on FAULTN pin and waits for a pulse on FENL and FENH pins before t_{FENx_PERIOD} expires.

*   The **FENX_DLY_CFG** bitfield sets the delay between trigger signal and deployment start (no delay, 2 ms, 4 ms or 8 ms)

If FENx_MODE = 1 (PWM mode):

*   **FENX_FAULT_PERIOD** bitfield sets the number of filtered PWM pulses on FENH and FENL signals
*   The integrity check on FENL and FENH in PWM mode is automatically enabled: the PWM signal is continuously monitored by an internal timer that measures the time between two rising edges, checking frequency and duty cycle.

When the integrity check is working, a fault is reported in the FENX_INTEGRITY_STATUS register:

*   FENH_HIGH_FREQ and/or FENL_HIGH_FREQ if high-frequency error is detected
*   FENH_LOW_FREQ and/or FENL_LOW_FREQ if low-frequency error is detected
*   FENH_PWM_TIMEOUT and/or FENL_PWM_TIMEOUT if PWM timeout error is detected
*   FENH_LEV_TIMEOUT and/or FENL_LEV_TIMEOUT if level timeout error is detected.

FENH_ECHO and FENL_ECHO are an echo of FENH and FENL pins respectively.

6.2 Deployment via SPI

The deployment can be triggered via the SPI by writing the proper code in the HS_CMD and LS_CMD registers:

- 0x155 in HS_CMD register
- 0x2AA in LS_CMD register.

6.3 Deployment status

In the DEPLOY_STATUS register, it is possible to check the information reported in Table 9:

Table 9. Deployment status bits

Bit field	Description
FIRE_INHIBIT	The status of the fire inhibit signal
DEPLOY_CNT	The number of performed deployments
FIRE_RUNNING	The status of deployment on-going
FIRE_GOOD	The status of right deployment sequence complete
FIRE_END_BY_FAULT	Deployment interrupted due to a fault
FIRE_END	End of deployment sequence
FENL_ARM	FENL ARM condition
FENH_ARM	FENH ARM condition

The value of time during which the deployment current is above the threshold set in DEP_MON_THR bitfield is stored in the DEP_CURR_MON bitfield of the DEPLOY_CURRENT_MONITOR register.

The relationship between the deployment current monitor and the DEP_CURR_MON code is the following:

$$t_{DEP\_MON\_TH} = (DEP\_CURR\_MON)_{dec} * t_{DEP\_CUR\_MON} \tag{17}$$

$$Example: t_{DEP\_MON\_TH} = (0x5D)_{dec} * 8\mu s = 744\mu s$$

7 Layout suggestions

Referring to the schematic in Figure 16, some layout suggestions are presented in this chapter.

Figure 16. Reference schematic
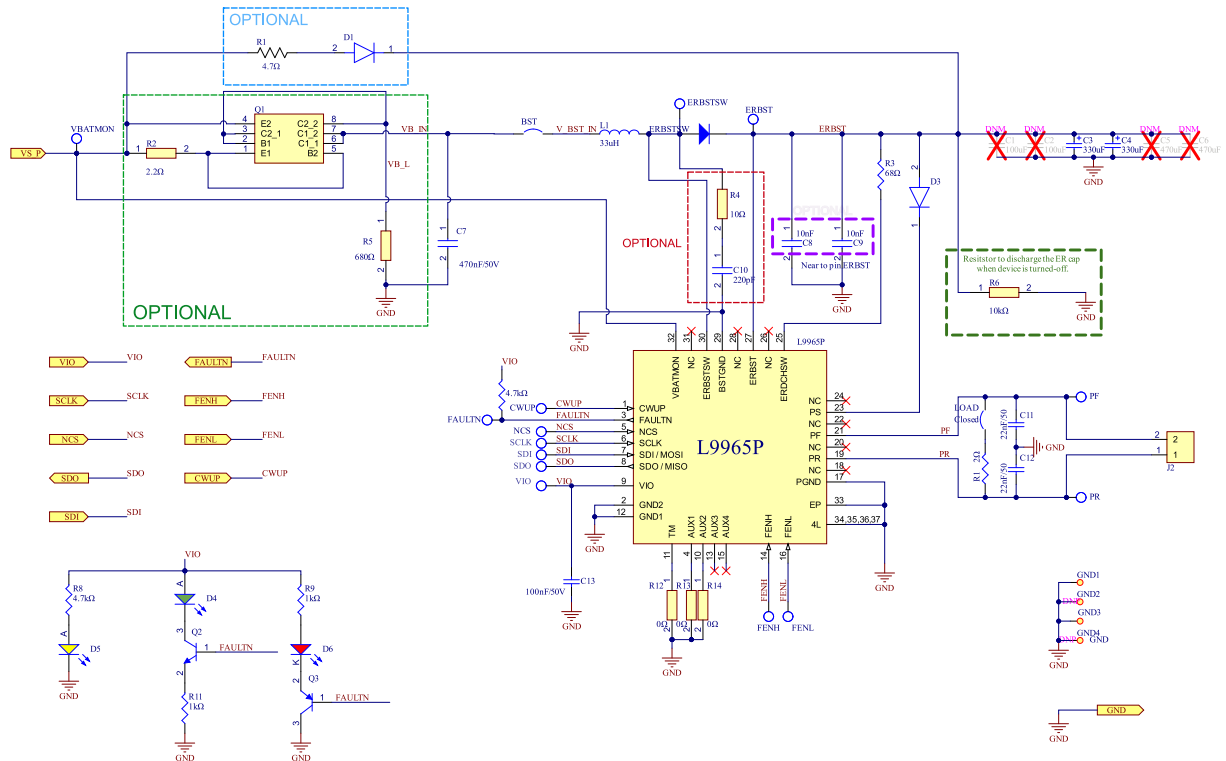
7.1 ERBST

Boost components (inductor L1 and diode D1) should be placed as near as possible to the IC to maximize efficiency (the fewer parasitic components, the smaller the loss) and reduce EMI, as shown in Figure 17.

If needed, a snubber circuit (R4, C10) tie to the BSTGND can be added.

Figure 17. ERBST external components
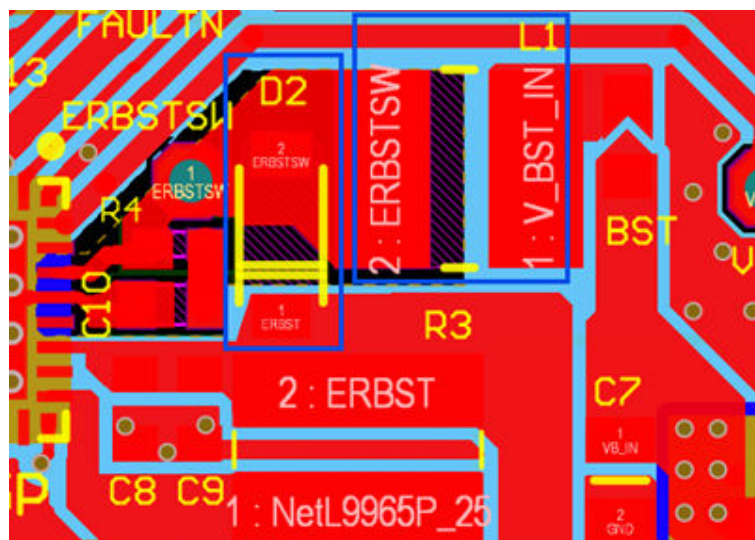
7.2 ER capacitor

Components involved in the ER capacitor diagnostic (capacitors C1 and C2, and resistor R3) should be placed as near as possible to the IC to minimize parasitics that can degrade the measurement of capacitance and ESR, as shown in Figure 18.

Note: *Two capacitors for safety, to cover the fault case in which one cap will open.*

Figure 18. ER capacitor
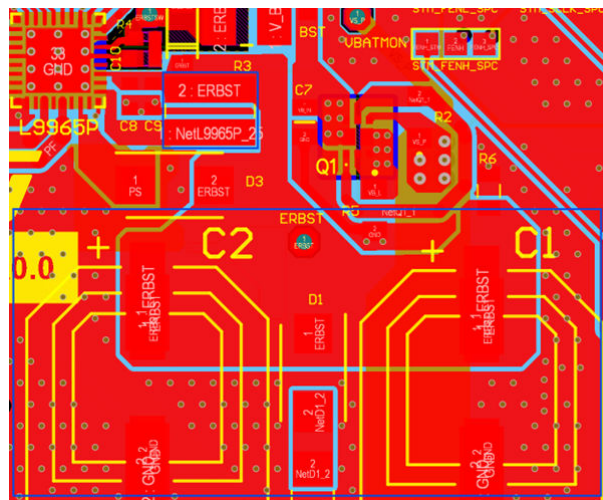
7.3 Deployment stage

ER capacitors (C1 and C2) should be placed near the PS pin in order to supply the deployment stage while minimizing parasitic components, as shown in Figure 19 (left). If necessary, can be added D3 as back feeding protection from the PS pin.

PF and PR traces shall be sized to sustain the desired deployment current profile. The IC is designed taking in consideration parasitics due to long wires.

C11 and C12 (typ. value 22 nF) shall be placed to protect both SF and SR pins from ESD spikes as shown in Figure 19 (right).

To improve EMC performance, it is suggested to place 100 pF + 1 nF near the IC pins, 100 nF near the pyrofuse connector.

Figure 19. Deployment stage

ER cap traces	PR/PF trace
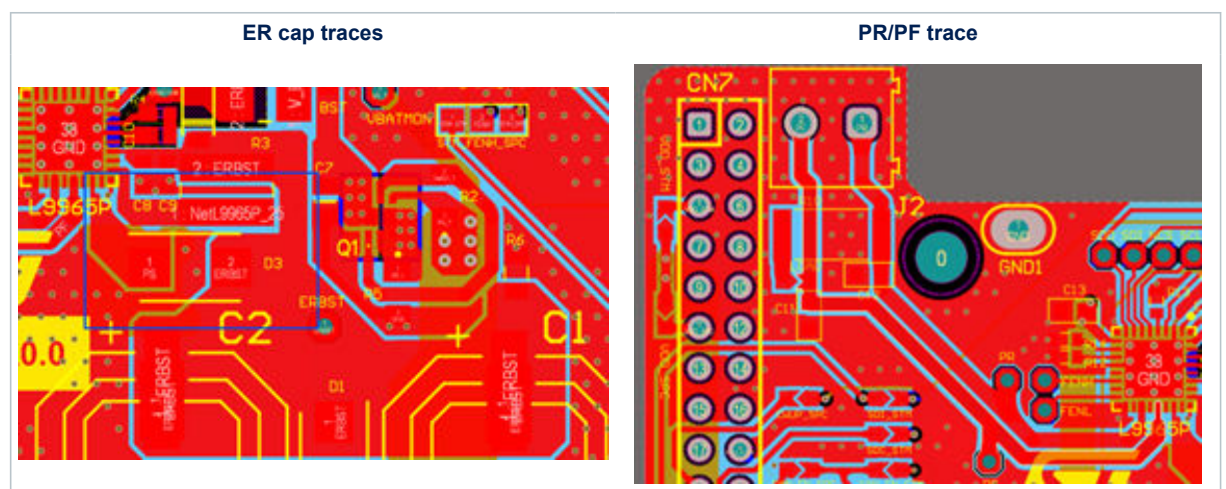
7.4 Optional components

The Q1 integrated circuit is used to limit the initial inrush current from VIN to the ER capacitors, in combination with resistors R2 and R5. To improve thermal performance, add an exposed pad on the bottom

The TVS diodes (D9 and D10) on VIN can be used to protect the device when spikes may exceed the AMR. The Schottky diode D8 may be added to add reverse battery protection.

Figure 20. Optional components
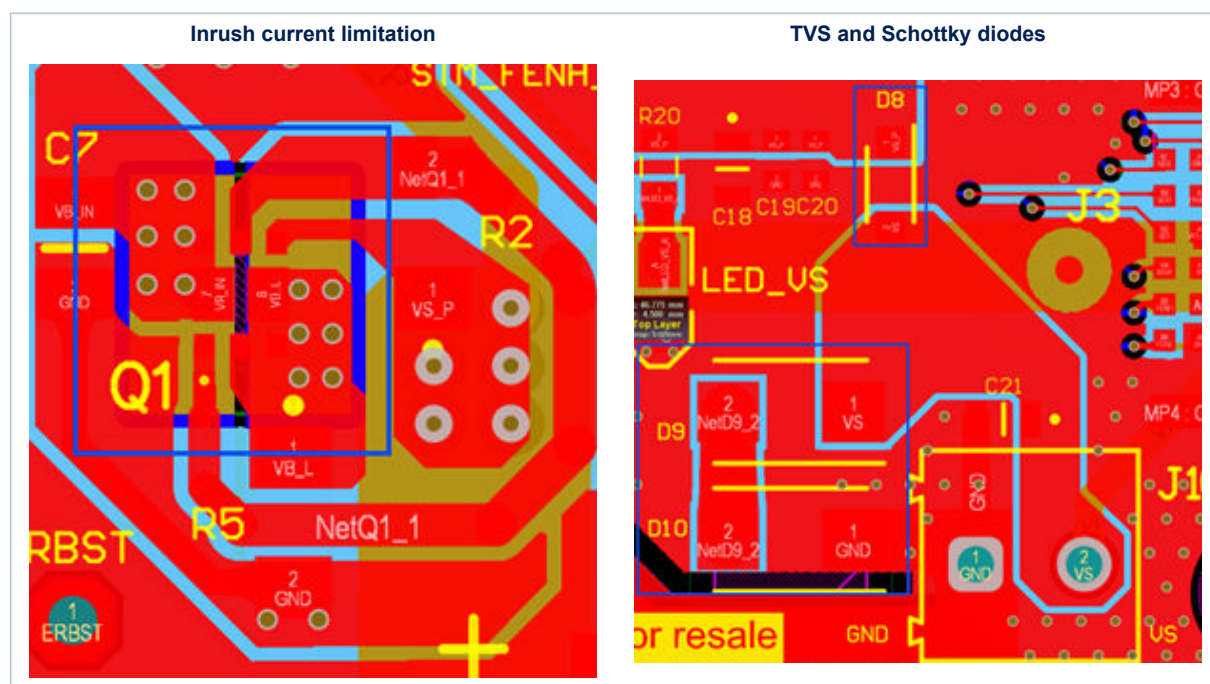
The battery filter stage (C18, C19, C20) and the input capacitor (C21) should be placed close to the input connector to filter noise from the battery and to avoid coupling around in the PCB (refer to Figure 21).

Figure 21. Filter stage
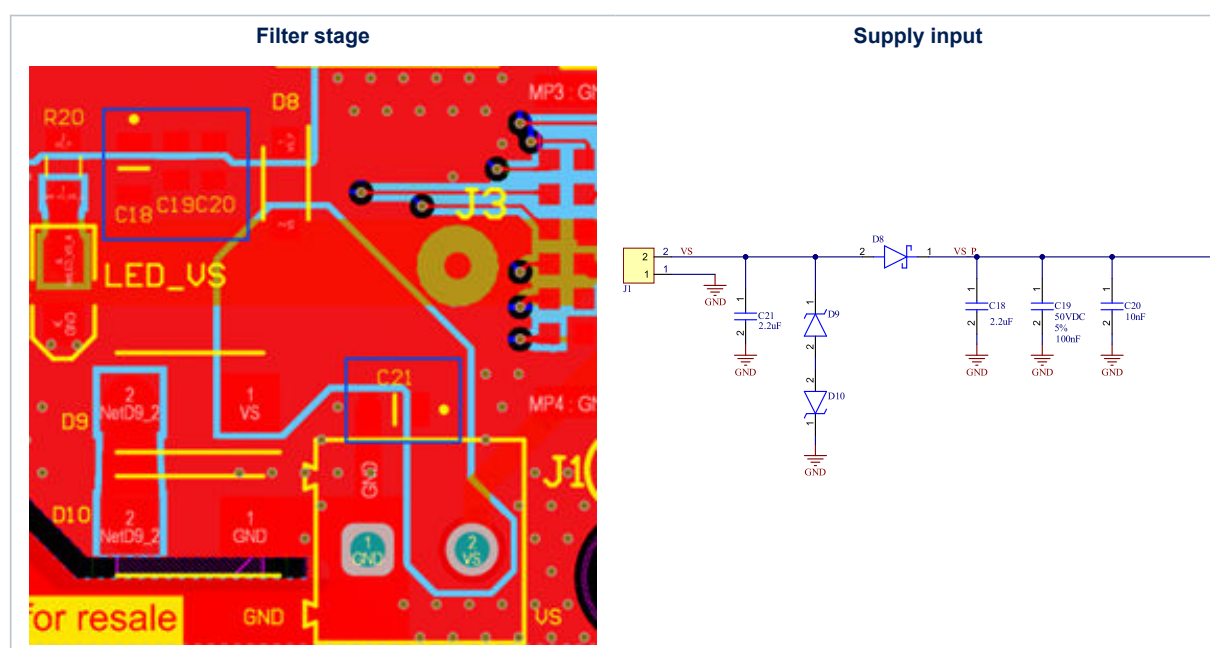
7.5 PCB suggestions

The reference design is done on a 4-layer PCB in 2s2p configuration, with GND and Power (VS) as external layers (TOP and BOTTOM). All GND planes should be tied together using an adequate number of vias (as much as possible). Reserve inner layers for sensing and communication lines.

To improve EMC robustness:

- Place all ERBST components as close as possible to the IC, minimizing parasitic effects. The PBC area under the boost coil should be free of metal layers/metal strips.
- Place protection components as close as possible to the relevant external connector: TVS diode, input filter stage, and ESD capacitors.

Revision history

Table 10. Document revision history

Date	Revision	Changes
01-Oct-2025	1	Initial release.
05-Dec-2025	2	Added L99BM2P and L99BM2C part numbers. Updated Section 1, Section 2 and all sub-sections, Section 3.8.1, Section 7 and all sub-sections. Added Section 5.1.7.

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