Migrating from the STM32WBA5xxx to the STM32WBA6xxx MCUs

Introduction

The designers of STM32 microcontroller applications must have the possibility to replace one microcontroller type easily by another from the same product family or by products from a different family. The reasons for migrating an application to a different microcontroller can be for example:

- To meet higher product requirements, extra demands on memory size, or an increased number of I/Os.
- To meet cost reduction constraints that require switching to smaller components and shrink the PCB area.

This application note details the steps required to migrate from a design based on an STM32WBA5xxx device to an application based on one of the STM32WBA6xxx MCUs.

This document provides guidelines for hardware and peripheral migration. To understand the information inside this application note better, the user must be familiar with the STM32 microcontroller family.

For additional information, refer to the product datasheets and reference manuals available on www.st.com.

Reference documents

This application note must be read with the following documents:

[1] STM32WBA6xxx reference manual (RM0515)

[2] STM32WBA6xxx datasheet (DS14736)

[3] STM32WBA5xxx datasheet (DS14127)

[4] STM32 microcontroller system memory boot mode (AN2606)

[5] STM32 Cortex®-M33 MCUs programming manual (PM0264)

[6] Cortex®-M33 processor technical reference manual, available on the Arm website

1 STM32WBA6xxx MCUs

The STM32WBA6xxx devices are ultra-low-power and wireless MCUs with enhanced efficiency, performance, and memory size as follows:

- Up to 2 Mbytes of dual-bank flash memory with ECC accelerated by instruction/data caches and up to 512 Kbytes of embedded SRAM with optional parity.

These devices reuse the same embedded 32-bit Arm® Cortex®-M33 core as the STM32WBA5xxx devices. This core runs at 100 MHz for both devices. It provides improved security features due to the presence of the ultra-low-power Arm® TrustZone® for Armv8-M.

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The STM32WBA6xxx devices includes a larger set of peripherals with more advanced features compared to the STM32WBA5xxx devices. These features include:

- Power consumption:
  - New low-power Stop 2 mode.
- Interfaces:
  - Voltage reference buffer for ADC: VREFBUF(1)
  - Additional GPIOs and secondary V_{DDIO2} supply
  - Additional touch sense channels: TSC
  - Improved random number generator: RNG
  - Additional 32-bit general-purpose timer: TIM4
  - Two additional I²C interfaces: I2C2(2) and I2C4(2)
  - One additional SPI: SPI2(2)
  - One additional USART: USART3(2)
  - Support for debug: ETM(1)
  - USB on-the-go high-speed (OTG) peripheral with embedded PHY and OTG 2.0 full-speed controller

1. *Feature only available on the STM32WBA62/65 devices.*
2. *Feature only available on the STM32WBA62/64/65 devices.*

Both the STM32WBA5xxx and STM32WBA6xxx MCUs embed high-speed memories and an extensive range of enhanced I/Os.

Table 1. Overview of the STM32WBA5xxx and STM32WBA6xxx

Package	Memory size		Device	
	Flash memory	SRAM	STM32WBA5xxx	STM32WBA6xxx
UFQFPN32	1 Mbyte	128 Kbytes	STM32WBA52KG	N/A
			STM32WBA54KG	
	512 Kbytes	96 Kbytes	STM32WBA52KE	
			STM32WBA54KE	
Thin WLCSP41 SMPS	1 Mbyte	128 Kbytes	STM32WBA55HG	N/A
	512 Kbytes	96 Kbytes	STM32WBA55HE	
UFQFPN48	1 Mbyte	128 Kbytes	STM32WBA52CG	N/A
			STM32WBA54CG	
	512 Kbytes	96 Kbytes	STM32WBA52CE	

Package	Memory size		Device	
	Flash memory	SRAM	STM32WBA5xxx	STM32WBA6xxx
UFQFPN48	512 Kbytes	96 Kbytes	STM32WBA54CE	N/A
UFQFPN48 SMPS	2 Mbytes	512 Kbytes	N/A	STM32WBA63CI
	1 Mbyte	256 Kbytes	N/A	STM32WBA63CG
		128 Kbytes	STM32WBA55CG	N/A
	512 Kbytes	96 Kbytes	STM32WBA55CE	
UFQFPN48 USB	2 Mbytes	512 Kbytes	N/A	STM32WBA64CI, STM32WBA62CI
	1 Mbyte	256 Kbytes	N/A	STM32WBA64CG, STM32WBA62CG
UFQFPN48 SMPS USB	2 Mbytes	512 Kbytes	N/A	STM32WBA65CI
	1 Mbyte	256 Kbytes	N/A	STM32WBA65CG
UFBGA59 SMPS	1 Mbyte	128 Kbytes	STM32WBA55UG	N/A
	512 Kbytes	96 Kbytes	STM32WBA55UE	
VFQFPN68 SMPS USB	2 Mbytes	512 Kbytes	N/A	STM32WBA65RI
	1 Mbyte	256 Kbytes	N/A	STM32WBA65RG
Thin WLCSP88	2 Mbytes	512 Kbytes	N/A	STM32WBA62MI
	1 Mbyte	256 Kbytes	N/A	STM32WBA62MG
Thin WLCSP88 SMPS	2 Mbytes	512 Kbytes	N/A	STM32WBA65MI
	1 Mbyte	256 Kbytes	N/A	STM32WBA65MG
UFBGA121	2 Mbytes	512 Kbytes	N/A	STM32WBA62PI
	1 Mbyte	256 Kbytes	N/A	STM32WBA62PG
UFBGA121 SMPS	2 Mbytes	512 Kbytes	N/A	STM32WBA65PI
	1 Mbyte	256 Kbytes	N/A	STM32WBA65PG

1.1 Memory availability

The STM32WBA6xxx MCUs embed more memory than the STM32WBA5xxx as shown in the table below.

Table 2. Memory size on the STM32WBA5xxx and STM32WBA6xxx

Product	Flash memory		SRAM1	SRAM2
	Size	Bank		
STM32WBA6xxx	Up to 2 Mbytes	Dual	Up to 448 Kbytes	64 Kbytes
STM32WBA5xxx	Up to 1 Mbyte	Single	Up to 64 Kbytes	

1.2 System architecture differences between the STM32WBA5xxx and STM32WBA6xxx MCUs

Both the STM32WBA5xxx and STM32WBA6xxx MCUs embed:

- High-speed memories
- An extensive range of enhanced I/Os and peripherals connected to:
  - APB buses
  - AHB buses
  - A 32-bit multi-AHB bus matrix

The bus matrix provides access from a manager to a subordinate, enabling concurrent access and efficient operation when several high-speed peripherals work simultaneously.

In addition, the STM32WBA6xxx MCUs connect more managers to the bus matrix than the STM32WBA5xxx. The STM32WBA6xxx MCUs also embed more peripherals on internal buses.

The figures below detail the system architectures of the STM32WBA5xxx and STM32WBA6xxx MCUs.

Figure 1. STM32WBA5xxx system architecture

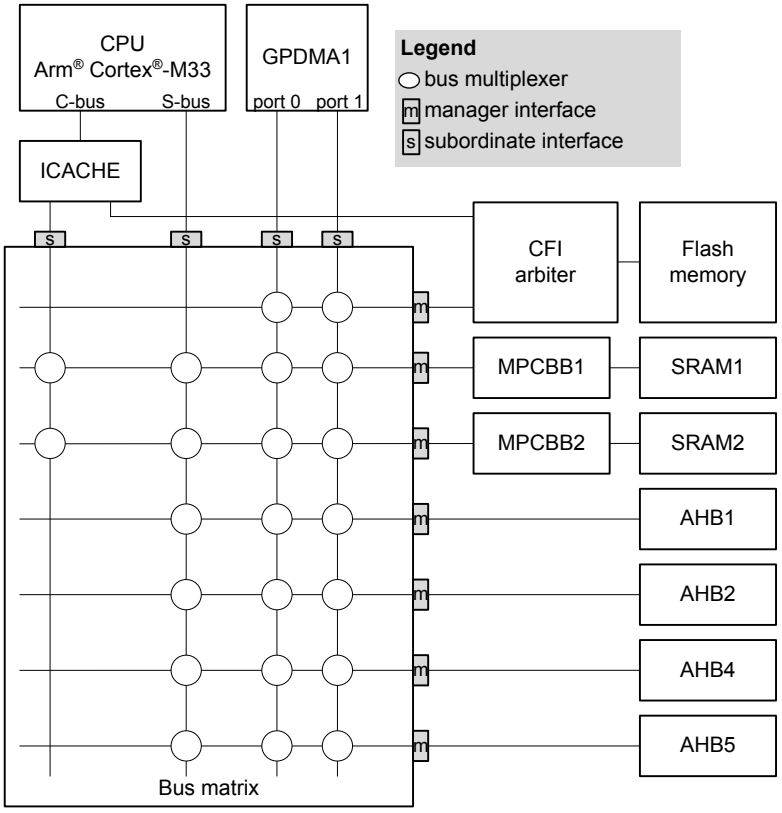
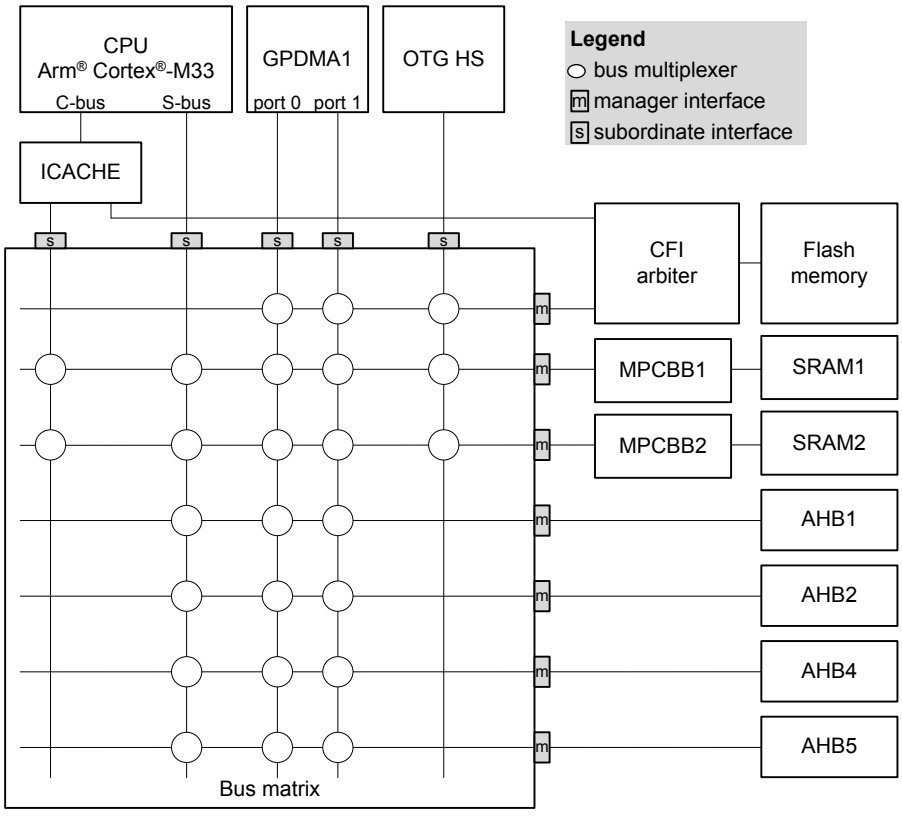


Figure 2. **STM32WBA6xxx system architecture**



2 Migrating the hardware

The STM32WBA6xxx MCUs offer:

- Several 48-pin packages with three versions of pinout:
  - Without an internal switched-mode power supply (SMPS) but with OTG: the 48-pin packages differ by nine pins. This difference is due to the presence of the internal OTG.
  - With an internal SMPS but without OTG: the package is then fully compatible with the 48-pin package of the STM32WBA5xxx MCUs.
  - With internal SMPS and with OTG: the 48-pin packages differ by nine pins. This difference is due to the presence of the internal OTG.
- 68-pin and 121-pin packages. Not available in the STM32WBA5xxx MCUs.

Note: OTG is available only on the STM32WBA62, STM32WBA64, and STM32WBA65 devices.
The SMPS is available only on the STM32WBA63 and STM32WBA65 devices.

The table below compares the packages with no SMPS available for the STM32WBA6xxx MCUs to those available for the STM32WBA5xxx MCUs. It lists the pinout compatibility and differences between these packages.

Table 3. Packages without SMPS on the STM32WBA5xxx and STM32WBA6xxx MCUs

Package (size in mm × mm)	STM32WBA6xxx versus STM32WBA5xxx	Pinout differences (pin name)		
		Pin number	STM32WBA5xxx	STM32WBA6xxx USB
UFQFPN48 (7 × 7) (1)	• Compatible with nine differences on pins 13 to 21 (the other pins are the same) • No PA0, PB9, and PB[7:5]. • PB8 and PC[15:13] have different pin positions.	13	PA0	VDDUSB
		14	PB9	PD9
		15	PB8	PD8
		16	PC15	PD7
		17	PC14	PD6
		18	PC13	PB8
		19	PB7	PC15
		20	PB6	PC14
		21	PB5	PC13
UFBGA121 (6 × 6) (2)	• Package not available for the STM32WBA5xxx MCUs.	-	-	-

1. *Available only for the STM32WBA62/64 devices.*
2. *Available only for the STM32WBA62 devices.*

The table below compares the packages with SMPS available for the STM32WBA6xxx MCUs to those available for the STM32WBA5xxx MCUs. It lists the pinout compatibility and differences between these packages.

Table 4. Packages with SMPS on the STM32WBA5xxx and STM32WBA6xxx MCUs

Package (size in mm × mm)	STM32WBA6xxx versus STM32WBA5xxx	Pinout differences (pin name)		
		Pin number	STM32WBA5xxx SMPS	STM32WBA6xxx SMPS USB
UFQFPN48 (7 × 7) (1) without OTG	Pin-to-pin compatible with the STM32WBA5xxx MCUs	-	-	-
UFQFPN48 (7 × 7) (2) with OTG	Compatible with nine differences on pins 13 to 21 (the other pins are the same): • No PA0, PB9, and PB[7:5] • PB8 and PC[15:13] have different pin positions	13	PA0	VDDUSB
		14	PB9	PD9
		15	PB8	PD8
		16	PC15	PD7
		17	PC14	PD6
		18	PC13	PB8
		19	PB7	PC15
		20	PB6	PC14
		21	PB5	PC13
VFQFPN68 (8 × 8) (2)	Package not available for the STM32WBA5xxx MCUs.	-	-	-
UFBGA121 (6 × 6) (2)	Package not available for the STM32WBA5xxx MCUs.	-	-	-

1. *Available only for the STM32WBA63 devices.*
2. *Available only for the STM32WBA65 devices.*

3 Boot mode compatibility

3.1 Boot mode selection

For the STM32WBA5xxx and STM32WBA6xxx MCUs, the BOOT0 input pin can come from the PH3-BOOT0 pin or from an option bit, depending on the value of a user option bit to free the GPIO pad if needed.

The bootloader is located in the system memory. It is used to reprogram the flash memory by using USART, I²C, SPI, or OTG in device mode through a DFU (device firmware upgrade).

Note: OTG is only available on the STM32WBA62/64/65 devices.

The STM32WBA5xxx and STM32WBA6xxx MCUs have compatible boot modes when TrustZone® is disabled or enabled (see the tables below). Refer to [1] for more details.

Table 5. Boot modes when TrustZone® is disabled (TZEN = 0) on the STM32WBA5xxx and STM32WBA6xxx MCUs

NBOOT0 FLASH_ OPTR[27]	BOOT0 pin PH3	NSWBOOT0 FLASH_OPTR[26]	Boot area	ST-programmed default value		
				Area	STM32WBA5xxx	STM32WBA6xxx
-	0	1	Boot address defined through the user option bytes NSBOOTADD0[24:0]	User flash memory:	0x0800 0000	
-	1	1	Boot address defined through the user option bytes NSBOOTADD1[24:0]	Bootloader:	0x0BF8 8000	0x0BF9 0000
1	-	0	Boot address defined through the user option bytes NSBOOTADD0[24:0]	User flash memory:	0x0800 0000	
0	-	0	Boot address defined through the user option bytes NSBOOTADD1[24:0]	Bootloader:	0x0BF8 8000	0x0BF9 0000

Table 6. Boot modes when TrustZone® is enabled (TZEN = 1)

BOOT_ LOCK	nBOOT0 FLASH_OPTR[27]	BOOT0 pin PH3	nSWBOOT0 FLASH_OPTR[26]	RSS command	Boot area	ST-programmed default value
0	-	0	1	0	Secure boot address defined through the user option bytes SECBOOTADD0[24:0]	User flash memory: 0x0C000000
	-	1	1	0	RSS:	0x0BF80000
	1	-	0	0	Secure boot address defined through the user option bytes SECBOOTADD0[24:0]	User flash memory: 0x0C000000
	0	-	0	0	RSS:	0x0BF80000
	-	-	-	≠0		
1	-	-	-	-	Secure boot address defined through the user option bytes SECBOOTADD0[24:0]	User flash memory: 0x0C000000

3.2 Embedded bootloader

ST programs the embedded bootloader located in the system memory during production. This bootloader allows the user to program the flash memory, using one of the serial interfaces listed in the table below.

Table 7. Bootloader interface on the STM32WBA5xxx and STM32WBA6xxx MCUs

Peripheral	Pin name (number)	STM32WBA5xxx	STM32WBA6xxx	
			STM32WBA63	STM32WBA62/64/65
OTG	USB_DM (PD7)	N/A	N/A	X
	USB_DP (PD6)			X
USART1	USART1_TX(PB12)	X	X	
	USART1_RX(PA8)	X	X	
USART2	USART2_TX(PA12)	X	X	
	USART2_RX(PA11)	X	X	
I2C1	I2C1_SCL(PB2)	X	X	
	I2C1_SDA (PB1)	X	X	
I2C3	I2C3_SCL(PA6)	X	X	
	I2C3_SDA (PA7)	X	X	
SPI2	SPI2_NSS (PA10)	N/A	N/A	X
	SPI2_SCK (PA9)			X
	SPI2_MISO (PB0)			X
	SPI2_MOSI (PB14)			X
SPI3	SPI3_NSS (PA5)	X	X	
	SPI3_SCK (PA0)	X	X	
	SPI3_MISO (PB9)	X	X	
	SPI3_MOSI (PB8)	X	X	

For more details on the bootloader, refer to [4].

4 Migrating the peripherals

4.1 STM32 product cross-compatibility

The STM32 microcontrollers embed a set of peripherals that can be classified into the following groups:

- Group 1: peripherals. By definition, common to all products.
  Those peripherals are identical, so they have the same structure, registers, and control bits. There is no need to perform any firmware change to keep the same functionality at application level after migration. All the features and the behavior remain the same.
- Group 2: peripherals shared by all products but with only minor differences (in general to support new features).
  The migration from one product to another is very easy and does not need any significant new development effort.
- Group 3: peripherals that have considerable changes from one product to another (new architecture or new features for example).
  For this group of peripherals, the migration requires a new development at the application level.

The security architecture of the STM32WBA6xxx and STM32WBA5xxx MCUs is based on the Arm® TrustZone® technology with the Armv8-M mainline extension. Each GPIO or peripheral, DMA channel, clock configuration register, ICACHE, or small part of flash memory or SRAM can be configured as trusted or untrusted.

The innovative features of the STM32WBA6xxx MCUs include a new Stop 2 mode architecture, allowing wake-up for a reduced set of peripherals down to Stop 2 mode.

The table below summarizes the available peripherals or features in the STM32WBA5xxx and STM32WBA6xxx MCUs as well as their compatibility.

Table 8. STM32 peripheral/feature compatibility between STM32WBA5xxx and STM32WBA6xxx MCUs

Peripheral or feature		STM32WBA5xxx	STM32WBA63	STM32WBA65	STM32WBA62	STM32WBA64
Core		Cortex®-M33 TZ, MPU, DFU, DSP				
Maximum CPU frequency		100 MHz				
Caches	ICACHE	1× ICACHE				
PWR/regulators	Power supply	1.71 V to 3.6 V				
	LDO	Available				
	SMPS	SMPS/LDO on-the-fly selection			N/A	N/A
	VOS range	Range 1				
		Range 2				
Low-power modes		Stop 0				
		Stop 1				
		N/A	Stop 2			
Flash memory	Size	Up to 1 Mbyte	Up to 2 Mbytes			
	Bank	Single-bank with TrustZone®	Dual-bank with TrustZone®			
SRAMs	SRAM1	Up to 64 Kbytes	Up to 448 Kbytes			
	SRAM2	64 Kbytes with parity				
DMA		GPDMA (8 channels each)				
PLL		PLL (main)				
		N/A	N/A	PLL for the OTG PHY		

Peripheral or feature		STM32WBA5xxx	STM32WBA63	STM32WBA65	STM32WBA62	STM32WBA64
GTZC (global TrustZone® controller)		Three independent 32-bit AHB interfaces for TrustZone® security controller (TZSC), TrustZone® illegal access controller (TZIC), and block-based memory protection controller (MPCBB). TZIC is accessible only with secure transactions. Secure and nonsecure access supported for the privileged and unprivileged parts of the TZSC. Set of registers to define product security settings.				
Antitamper detection		Six tamper input/output pins, 128-byte backup registers.				
CRC		1× CRC				
High-speed low-voltage (HSLV) mode		N/A	N/A	HSLV mode(1)		N/A
VDDIO2		N/A	N/A	PG[15:2]		N/A
GPIO	Port A	PA[15:5, 2:1]				
		PA[4]	N/A	PA[4]		N/A
		PA[3]	N/A	PA[3]		
		PA[0]				N/A
	Port B	PB[15:14, 12, 8, 4:0]				
		PB[13, 11:10]	N/A	PB[13]		
		PB[9, 7:5]				N/A
	Port C	PC[15:13]				
		N/A	N/A	PC[12:0]		N/A
	Port D	N/A	N/A	PD[15:10, 4:0]		N/A
				PD[9:5]		
	Port E	N/A	N/A	PE[6:0]		N/A
	Port G	N/A	N/A	PG[15:2]		N/A
	Port H	PH[3]				
Timers	Advanced control	TIM1 (16-bit)				
	General-purpose	TIM2 (32-bit) + TIM3 (16-bit)		TIM2/4 (32-bit) + TIM3 (16-bit		
	Basic	TIM16/17 (16-bit)				
	Low-power	LPTIM1/2 (16-bit) autonomous mode				
	Watchdogs	1× WWDG and 1× IWDG				
	RTC	1× RTC + binary mode selection				
	SysTick	2				
Communication interfaces	SPI	SPI1 + autonomous mode				
		N/A	N/A	SPI2 + autonomous mode		
		SPI3 + autonomous mode	SPI3 + autonomous mode, and Stop 2 mode			
	I²C	I2C1 + autonomous mode				
		N/A	N/A	I2C2 + autonomous mode		
		I2C3 + autonomous mode	I2C3 + autonomous mode, and Stop 2 mode			
		N/A	N/A	I2C4 + autonomous mode		
	USART	USART1/2 + autonomous mode				
		N/A	N/A	USART3 + autonomous mode		

Peripheral or feature		STM32WBA5xxx	STM32WBA63	STM32WBA65	STM32WBA62	STM32WBA64
Communication interfaces	LPUART	LPUART1 + autonomous mode	LPUART1+ autonomous mode, and Stop 2 mode			
	SAI (audio interface)	SAI1				
	OTG	N/A	N/A	OTG high-speed with embedded PHY		
Analog peripherals	ADC	1 × 12-bit ADC4 (2.5 Msps) + autonomous mode				
	COMP	COMP1				
		COMP2				N/A
	Voltage reference buffer	N/A	N/A	VREFBUF		N/A
Cryptographic peripherals		AES				
		AES				
		PKA				
		HASH				
		RNG 6 sources	RNG 3 sources			
Signal-processing coprocessor accelerators	TSC (touch sensing control)	Up to 12 channels		Up to 24 channels		Up to 10 channels
Debug		JTAG, SWD				
		N/A	N/A	ETM		N/A

1. *SomeI/Os can increase their speed at a low voltage when configured in HSLV mode.*

4.2 Secure and nonsecure boundaries of peripheral memory mapping

The peripheral address mapping is the same in the STM32WBA6xxx MCUs compared to the STM32WBA5xxx MCUs.

The new peripherals of the STM32WBA6xxx MCUs have been added to the memory map. For more details on the memory mapping, refer to [1].

5 Migrating the security peripherals

5.1 TAMP

The antitamper detection circuit (TAMP) of the STM32WBA6xxx MCUs is used to protect sensitive data from external attacks. Thirty-two 32-bit backup registers are retained in all low-power modes. There is no difference between the STM32WBA5xxx and STM32WBA6xxx MCUs.

5.1.1 Tamper pins and internal events

The tamper pins and internal events are the same between the STM32WBA5xxx and STM32WBA6xxx MCUs.

5.1.2 Boot hardware key

The first eight backup registers can be used to store a boot master key, programmed during boot for the SAES (secure AES). Once locked, the software cannot access the eight backup registers anymore: they are read as 0 and write operations to these registers are ignored.

The software cannot clear the BHKLOCK locking bit. The hardware clears it following a tamper event. Disabling the readout protection (RDP) also clears this bit. In both cases, the backup registers are also erased. Refer to [1], section "Boot hardware key" for more details.

5.2 HASH (hash processor)

The STM32WBA5xxx and STM32WBA6xxx MCUs embed the same HASH hardware accelerator with the same features.

5.3 RNG (true random number generator)

The STM32WBA5xxx and STM32WBA6xxx MCUs embed an RNG hardware accelerator with the same features. The RNG embedded in the STM32WBA6xxx MCUs is however an improved version with additional health test configuration registers and fewer noise sources.

Table 9. RNG features in the STM32WBA5xxx and STM32WBA6xxx MCUs

Features	STM32WBA5xxx	STM32WBA6xxx
Noise source	6	3
Health test configuration	HTCR	HTCR0
	N/A	HTCR1
	N/A	HTCR2
	N/A	HTCR3

5.4 PKA (public key accelerator)

The STM32WBA5xxx and STM32WBA6xxx MCUs embed the same PKA hardware accelerator with the same features.

5.5 AES and SAES hardware accelerators

The STM32WBA5xxx and STM32WBA6xxx MCUs embed two AES accelerators, both with the same features:

- A secure AES (SAES)
- A faster AES

5.6 GTZC (global TrustZone® controller)

The security architecture of the STM32WBA5xxx and STM32WBA6xxx MCUs is based on the Arm® TrustZone® technology with the Armv8-M mainline extension. Each GPIO or peripheral, DMA channel, clock configuration register, ICACHE, or a small part of flash memory or SRAM can be configured as trusted or untrusted.

The GTZC embedded in the STM32WBA5xxx and STM32WBA6xxx MCUs is used to configure secure-TrustZone® and privileged attributes within the full system. It contains the following subblocks:

- TZSC: the TrustZone® security controller
  This subblock defines the secure/privileged state of subordinate peripherals. The TZSC informs some peripherals (such as the RCC or GPIOs) about the secure status of each securable peripheral by sharing with the RCC and I/O logic.
- MPCBB: the block-based memory protection controller
  This subblock configures the internal RAM in a TrustZone®-system product that features a segmented SRAM (pages of 512 bytes) with programmable-security and privileged attributes.
- TZIC: the TrustZone® illegal access controller
  This subblock gathers all illegal access events in the system and generates a secure interrupt towards the NVIC.

The GTZC registers of the STM32WBA5xxx and STM32WBA6xxx MCUs for the same peripheral are the same. The new peripherals of the STM32WBA6xxx secure MCUs were added to the register map.

5.6.1 GTZC implementation and resource assignments

The STM32WBA5xxx and STM32WBA6xxx MCUs implement the same GTZC peripherals, except for MPCBB1 (see the table below).

Table 10. MPCBB resources in the STM32WBA5xxx and STM32WBA6xxx MCUs

MPC	Resource	Block size (bytes)	Memory size (Kbytes)	STM32WBA5xxx	STM32WBA6xxx
MPCBB1	SRAM1	512	Memory size (Kbytes)	Up to 64	Up to 448
			Number of blocks	Up to 128	Up to 896
			Number of super-blocks	Up to 4	Up to 28
MPCBB2	SRAM2		Memory size (Kbytes)	64	
			Number of blocks	128	
			Number of super-blocks	4	
MPCBB5	RXTXSRAM		Memory size (Kbytes)	16	
			Number of blocks	32	
			Number of super-blocks	1	

5.6.2 TrustZone® security architecture

When TrustZone® security is enabled, the Armv8-M attributes define the access permissions based on the secure or nonsecure state:

- SAU (security attribution unit): up to eight SAU-configurable regions are available for security attribution.
- IDAU (implementation-defined attribution unit): it provides a first memory partition as nonsecure or nonsecure callable attributes. This partition is then combined with the results from the SAU security attribution, and the higher-security state is selected.

Based on IDAU security attribution, the flash memory, system SRAMs, and peripheral memory space are aliased twice for the secure and nonsecure states. However, the external memory space is not aliased.

The datasheets ([2] and [3]) of the STM32WBA5xxx and STM32WBA6xxx MCUs give the same example of memory map security attribution versus SAU configuration regions.

5.6.3 TrustZone® peripheral classification

When TrustZone® security is active, a peripheral can be either securable or TrustZone®-aware as follows:

- Securable: a peripheral protected by an AHB/APB firewall gate that is controlled from the TZSC to define security properties.
- TrustZone®-aware: a peripheral connected directly to the AHB or APB bus and implementing a specific TrustZone® behavior such as a subset of secure registers.

The default system security state is the same for the STM32WBA5xxx and STM32WBA6xxx MCUs.

6 Migrating the 2.4 GHz RADIO

This section analyzes the differences and similarities between the 2.4 GHz RADIO implemented in the STM32WBA5xxx and STM32WBA6xxx MCUs.

6.1 2.4 GHz RADIO

The table below shows the differences between the 2.4 GHz RADIO in the STM32WBA5xxx and STM32WBA6xxx MCUs.

Table 11. 2.4 GHz RADIO features in the STM32WBA5xxx and STM32WBA6xxx MCUs

Features		STM32WBA5xxx	STM32WBA63/64/65	STM32WBA62
Bluetooth® Low Energy	2 Mbit/s	X		
	1 Mbit/s	X		
	500 kbit/s coded	X		
	125 kbit/s coded	X		
	Audio	X		
	Angle of arrival (AoA)/ angle of departure (AoD)	X		N/A
	Thread	X		N/A
Zigbee®	Beacon management	X		N/A
	Nonbeaconed personal area network (PAN)	X		N/A
Thread®		X		N/A
Matter		With an external host		N/A
IEEE 802.15.4	Proprietary	X		N/A
Concurrent modes	Bluetooth® – Thread®	X		N/A
	Bluetooth® – Zigbee®	X		N/A
	Zigbee® – Thread®	X		N/A
	Bluetooth® – Thread® – Zigbee®	X		N/A
Packet traffic arbitration (PTA)		X		
Output power		+ 10 dBm		
External power amplifier (PA)		X		N/A

7 Migrating the system peripherals

This section analyzes the differences and similarities between the system peripherals implemented in the STM32WBA5xxx and STM32WBA6xxx MCUs.

7.1 SYSCFG (system configuration controller)

The table below shows the differences between the SYSCFG in the STM32WBA5xxx and STM32WBA6xxx MCUs.

Table 12. SYSCFG features in the STM32WBA5xxx and STM32WBA6xxx MCUs

Features	STM32WBA5xxx	STM32WBA6xxx
Common features	Managing the robustness feature	
	Configuring TrustZone® security register access	
	Configuring FPU interrupts	
	Driving capability on some I/Os and voltage booster for I/O analog switches	
Managing I/O compensation cells	Compensation cells on VDD: process/voltage/ temperature (PVT) conditions to control the current slew-rate and output impedance in the I/O buffer	Compensation cells on VDD/VDDIO2(1): PVT conditions to control the current slew-rate and output impedance in the I/O buffer.
I²C Fast-mode Plus	The I²C I/O Fast-mode Plus drive is controlled from the I²C peripheral. This mode can still be enabled/disabled in SYSCFG for four I/Os when not used by the I²C peripheral.	
OTG_HS PHY(2)	N/A	Configuring the OTG_HS PHY

1. *Only available on the STM32WBA62/65.*
2. *Only available on the STM32WBA62/64/65.*

7.2 Flash memory

Compared to the STM32WBA5xxx, the flash memory of the STM32WBA6xxx MCUs includes bigger memory space and advanced features (see the table below).

Table 13. Flash memory features in STM32WBA5xxx and STM32WBA6xxx MCUs

Feature	STM32WBA5xxx	STM32WBA6xxx
Size	Up to 1-Mbyte single bank (128 × 8-Kbyte pages)	Up to 2-Mbyte dual bank (128 × 8 Kbyte pages per bank)
	OTP area: 512 bytes, base address 0x0BF9 0000	OTP area: 512 bytes, base address 0x0BFA 0000
	RSS + RSS lib, base address 0x0BF8 0000	
	Bootloader, base address 0x0BF8 8000	Bootloader, base address 0x0BF9 0000
Access modes	Read (R) and write (W)	Read (R), write (W) and read-while-write (RWW)
	Single bank, 128-bit read/write access	Dual bank, 128-bit read/write access
ECC	9 bits per 128-bit quad word. The ECC mechanism supports: • One-bit error detection and correction • Two-bit error detection	
Read-access latency	Up to 3 wait states (WS) depending on the supply voltage and the frequency	
	The flash memory supports a low-power read mode (LPM). The number of WSs depends on the supply voltage and the frequency.	
	Instruction prefetch through ICACHE can be enabled by setting the PRFTEN bit to increase the code execution speed.	

Feature	STM32WBA5xxx	STM32WBA6xxx
Power-down mode per bank	After reset, the bank is in normal mode. The bank can be put in power-down mode.	After reset, both banks are in normal mode. Each bank can be independently put in power-down mode.
Endurance capability	10 kilo cycles (written and erased) on the entire flash memory 100 kilo cycles (written and erased) on 256 Kbytes (32 pages)	10 kilo cycles (written and erased) on the entire flash memory 100 kilo cycles (written and erased) on 512 Kbytes (256 Kbytes, 32 pages per bank)
Flash memory program and erase operations	Page/mass erase	Page/bank/mass erase (both banks)
	128-bit (quad word) programming	
Flash memory protection	Write protection (WRP)	
	Readout protection (RPD)	
	One secure watermark-based area	Two secure watermark-based areas (one per bank)
	One secure watermark-based hide protection area	Two secure watermark-based hide protection areas (one per bank)
	On-the-fly programmable secure block-based areas with page granularity	
	On-the-fly programmable privileged block-based areas with page granularity	
Privileged register protection	For secure (SPRIV) and nonsecure (NSPRIV) accesses	
Locking keys for RDP	OEM key protection for RDP regression between levels: • Possible RDP regression from L1 to L0 with the OEM1 key • Possible RDP regression from L1 to L0.5 with the OEM2 key • Possible RDP regression from L2 to L1 with the OEM2 key	

The end user configures the option bytes depending on the application requirements. The address mapping of the option bytes register is the same in the STM32WBA6xxx MCUs compared to the STM32WBA5xxx MCUs. The new option bytes of the STM32WBA6xxx were added to the register map. (See the table below and refer to [1], section "Flash memory option bytes" for more details).

Table 14. Main option bytes in the STM32WBA5xxx and STM32WBA6xxx MCUs

Option bit/byte	STM32WBA5xxx	STM32WBA6xxx
Global TrustZone® activation	TZEN: global TrustZone® security enable	
Readout protection	RDP levels: level 0, level 0.5, level 1, and level 2	
Reset	BOR_LEV[2:0]: BOR reset level.	
	NRST_STOP: reset generation in Stop mode	
	NRST_STDBY: reset generation in Standby mode	
	SRAM_RST: SRAM1 erased when a system reset occurs	
	SRAM2_RST: SRAM2 erased when a system reset occurs	
Watchdog	WWDG_SW: window watchdog selection	
	IWDG_SW: hardware or software independent watchdog selection	
	IWDG_STOP: independent watchdog counter freeze in Stop mode	
	IWDG_STDBY: independent watchdog counter freeze in Standby mode	
Secure and nonsecure boot	NSWBOOT0: software BOOT0	
	NBOOT0 option bit	
	NSBOOTADD0[24:0]: nonsecure boot base-address 0	
	NSBOOTADD1[24:0]: nonsecure boot base-address 1	

Option bit/byte	STM32WBA5xxx	STM32WBA6xxx
Secure and nonsecure boot	SECBOOTADD0[24:0]: secure boot base-address 0	
	BOOT_LOCK: boot lock	
Flash memory secure watermark	SECWM_PSTRT[6:0]: first page of the secure area	SECWM1_PSTRT[6:0]: first page of the secure area in bank 1
	SECWM_PEND[6:0]: last page of the secure area	SECWM1_PEND[6:0]: last page of the secure area in bank 1
	N/A	SECWM2_PSTRT[6:0]: first page of the secure area in bank 2
	N/A	SECWM2_PEND[6:0]: last page of the secure area in bank 2
	HDP_PEND[6:0]: last page of the HDP area	HDP1_PEND[6:0]: last page of the HDP area in bank 1
	HDPEN: hide protection area bank 1 enable	HDP1EN: hide protection area enable bank 1
	N/A	HDP2_PEND[6:0]: last page of the HDP area in bank 2
	N/A	HDP2EN: hide protection area enable bank 2
Flash memory write protection (WRP) areas	WRPA_PSTRT[6:0]: first page of the WPR area A	WRP1A_PSTRT[6:0]: first page of the WPR area A in bank 1
	WRPA_PEND[6:0]: last page of the WPR area A	WRP1A_PEND[6:0]: last page of the WPR area A in bank 1
	UNLOCK WRP area A	UNLOCK WRP area A in bank 1
	WRPB_PSTRT[6:0]: first page of the WPR area B	WRP1B_PSTRT[6:0]: first page of the WPR area B in bank 1
	WRPB_PEND[6:0]: last page of the WPR area B	WRP1B_PEND[6:0]: last page of the WPR area B in bank 1
	UNLOCK WRP area B	UNLOCK WRP area B in bank 1
	N/A	WRP2A_PSTRT[6:0]: first page of the WPR area A in bank 1
	N/A	WRP2A_PEND[6:0]: last page of the WPR area A in bank 2
	N/A	UNLOCK WRP area A in bank 2
	N/A	WRP2B_PSTRT[6:0]: first page of the WPR area B in bank 2
	N/A	WRP2B_PEND[6:0]: last page of the WPR area B in bank 2
	N/A	UNLOCK WRP area B in bank 2
Flash memory locking keys for RDP level regression	OEM1KEY[63:0]: OEM1 key	
	OEM2KEY[63:0]: OEM2 key	
RAM parity	SRAM2_PE: SRAM2 parity check enable option bit	
Flash memory banking	N/A	SWAP_BANK: used to swap banks
		DUALBANK: dual-bank configuration
I/O speed selection(1)	N/A	IO_VDD_HSLV: high-speed I/O configuration bit at a low VDD voltage
		IO_VDDIO2_HSLV: high-speed I/O configuration bit at a low VDDIO2 voltage

1. *Only available on the STM32WBA62/65.*

7.3 SRAMs

In the STM32WBA5xxx and STM32WBA6xxx MCUs, SRAM control is implemented in the RAMCFG controller (refer to [1], section "RAM configuration controller" for more details).

The table below compares the embedded SRAM features in the STM32WBA5xxx and STM32WBA6xxx MCUs.

Table 15. SRAMs in the STM32WBA5xxx and STM32WBA6xxx MCUs

Feature		STM32WBA5xxx	STM32WBA6xxx
Size (Kbytes)		SRAM1: up to 64 Kbytes	SRAM1: up to 448 Kbytes
		SRAM2: 64 Kbytes	SRAM2: 64 Kbytes
Access by DMA and CPU		SRAM1, SRAM2: byte, half-word (16-bit), or full word (32-bit) possible access	
CPU access bus	System bus	SRAM1, SRAM2	
	C-bus access	SRAM1, SRAM2	
Retention in Stop and Standby modes		SRAM1 up to 64 Kbytes	SRAM1 page 1: 64 Kbytes
		N/A	SRAM1 page 2: 64 Kbytes
		N/A	SRAM1 page 3: 64 Kbytes
		N/A	SRAM1 page 4: 64 Kbytes (1)
		N/A	SRAM1 page 5: 192 Kbytes (1)
		SRAM2: 64 Kbytes	SRAM2: 64 Kbytes
Security		When the TrustZone® security is enabled, all SRAMs are secure after reset.	
Security		The SRAMs can be programmed as nonsecure using the MPCBB with a block granularity of 512 bytes.	
Hardware erase conditions		The hardware erases all SRAMs in the case of RDP level regression to Level 0.5 or 0.	
		The tamper detection circuit protects SRAM2. The hardware erases SRAM2 in the case of a tamper detection.	
Software erase conditions		A request to erase each SRAM can be made by executing a specific software sequence, detailed in the product reference manuals, in the "RAMCFG" section.	
System reset erase		SRAM2 is erased when a system reset occurs if the SRAM2_RST option is selected.	
		SRAM1 is erased when a system reset occurs if the SRAM1_RST option is selected.	
WRP		SRAM2 can be write-protected with a page granularity of 1 Kbyte.	
Error detection		AN SRAM2 parity error can be detected if the SRAM2_PE option is selected.	
		Interrupts are generated when an SRAM2 parity error is detected: NVIC parity interrupt or NMI parity interrupt. Interrupts allow the device to exit Sleep, Stop 0, or Stop 1 mode.	
		AN SRAM2 parity error event can be linked to the BRK_IN break input of TIM1, TIM16, or TIM17.	
Read access latency		Up to 1 wait state (WS) depending on the voltage range 2 and the AHB clock frequency (HCLK)	

1. *Only available on devices with 2-Mbyte flash memory.*

7.4 Caches

The STM32WBA5xxx and STM32WBA6xxx MCUs embed the same ICACHE, which allows for a more efficient use of the internal flash memory.

7.5 DMA

The STM32WBA5xxx and STM32WBA6xxx MCUs have the same DMA architectures and features.

The DMA module of the STM32WBA MCUs is named GPDMA (general-purpose DMA). The DMA request and trigger mapping is the same in the STM32WBA6xxx MCUs compared to the STM32WBA5xxx. The new peripherals of the STM32WBA6xxx MCUs were added to the DMA request and trigger map. (See the table below and refer to [1], section "GPDMA" for more details.)

Table 16. DMA features in the STM32WBA5xxx and STM32WBA6xxx MCUs

Features	STM32WBA5xxx	STM32WBA6xxx
Number of managers	Dual bidirectional AHB manager	
Linked list	Separately programmed source and destination transfers	
	Programmable data handling between source and destination	
	Block-level (programmable number of data bytes)	
	Linear source and destination addressing: programmable signed address offsets between successive burst transfers	
Linked-list 2D addressing	2D source and destination addressing	
	Scatter-gather (multibuffer transfers), data interleaving, and deinterleaving via 2D addressing	
Data transfers from source to destination	Peripheral-to-memory, memory-to-peripheral, memory-to-peripheral, and peripheral-to-peripheral	
Number of channels	8	
Number of requests/ triggers	52 DMA requests	67 DMA requests
	30 triggers	32 triggers
Autonomous data transfer in Sleep and Stop modes	Autonomous data transfers and wake-up during Stop 0 and Stop 1 low-power modes	
TrustZone® privileged/ unprivileged	Same features	
Retention	Down to Stop 1 mode	Down to Stop 1 mode

7.6 NVIC

The STM32WBA5xxx and STM32WBA6xxx MCUs have the same NVIC mapping. The new peripherals of the STM32WBA6xxx were added to the NVIC map.

Table 17. NVIC mapping in the STM32WBA5xxx and STM32WBA6xxx MCUs

IRQ	Position	
	STM32WBA5xxx	STM32WBA6xxx
WWDG	0	
PVD	1	
RTC	2 to 3	
TAMP	4	
RAMCFG	5	
FLASH	6 to 7	
GTZC_TZIC	8	
RCC	9 to 10	
EXTI0 to EXTI15	11 to 26	
IWDG	27	

IRQ	Position	
	STM32WBA5xxx	STM32WBA6xxx
SEAS	28	
GPDMA1_CH0 to GPDMA1_CH7	29 to 36	
TIM1	37 to 40	
TIM2	41	
TIM3	42	
I2C1	43 to 44	
SPI1	45	
USART1	46	
USART2	47	
LPUART1	48	
LPTIM1	49	
LPTIM2	50	
TIM16	51	
TIM17	52	
COMP	53	
I2C3	54 to 55	
SAI	56	
TSC	57	
AES	58	
RNG	59	
FPU	60	
HASH	61	
PKA	62	
SPI3	63	
ICACHE	64	
ADC4	65	
RADIO	66	
	N/A	80 to 81
WKUP	67 and 70	
HSEM	68 to 69	
RCC_AUDIO	71	
TIM4[1]	N/A	72
I2C2[1]		73 to 74
SPI2[1]		75
OTG[1]		76
I2C4[1]		77 to 78
USART3[1]		79

1. *Only available on the STM32WBA62/64/65.*

7.7 EXTI

The STM32WBA5xxx and STM32WBA6xxx MCUs have the same external interrupt/event controller (EXTI) mapping. The new events of the STM32WBA6xxx have been added to the EXTI map.

Table 18. EXTI mapping in the STM32WBA5xxx and STM32WBA6xxx MCUs

Event	Position	
	STM32WBA5xxx	STM32WBA6xxx
GPIO	0 to 15	
PVD	16	
COMP	17 to 18	
RADIO	N/A	19 to 20

7.8 RCC (reset and clock control)

The RCC module of the STM32WBA6xxx MCUs manages the clocks and resets of the system and peripherals. It has the same features as the RCC module of the STM32WBA5xxx MCUs. The RCC register mapping is the same in the STM32WBA6xxx and STM32WBA5xxx MCUs. The new peripherals of the STM32WBA6xxx were added to the RCC register map. (See the table below and refer to[1], section "GPDMA" for more details.)

Table 19. RCC features in the STM32WBA5xxx and STM32WBA6xxx MCUs

Feature	STM32WBA5xxx	STM32WBA6xxx
Safe and flexible reset management without external components	System reset, power reset, and backup domain reset	
Internal clock sources	HSI16 with trimming	
	LSI1 32 kHz 1%	
	LSI2 32 kHz 500 ppm/°C	
External clock sources	HSE32 32 kHz with trimming	
	LSE 32.768 kHz	
PLLs	PLL1 (main PLL)	

Note: HSI16: 16 MHz high-speed internal RC oscillator.
LSI1: 32 kHz low-speed internal RC oscillator.
LSI2: 32 kHz high-stability, low-speed internal RC oscillator.
HSE32: 32 MHz high-speed external crystal oscillator.
LSE: 32.000 kHz or 32.768 kHz low-speed external crystal oscillator.

The table below lists the RCC input/output signals and their mapping on the STM32WBA5xxx and STM32WBA6xxx MCUs.

Table 20. RCC pin names in the STM32WBA5xxx and STM32WBA6xxx MCUs

Alternate function	Pin name	
	STM32WBA5xxx	STM32WBA6xxx
NRST	NRST	
OSC32_IN	PC14	
OSC32_OUT	PC15	
OSC_IN	OSC_IN	
OSC_OUT	OSC_OUT	
MCO	PA8	
LSCO	PA2	
AUDIO_CLK	PA4/PA5	

The table below details the RCC clock sources for the STM32WBA5xxx compared to the STM32WBA6xxx MCUs.

Table 21. Clock sources in the STM32WBA5xxx and STM32WBA6xxx MCUs

Clock source	STM32WBA5xxx	STM32WBA6xxx
System clock	100 MHz maximum frequency	
	16 MHz after reset, Stop, and Standby modes using HSI16	
	HSI16, HSE32, or PLL	
HSE	32 MHz user trimmed	
HSI16	Generated from an internal 16 MHz RC oscillator 16 MHz RC factory- and user-trimmed Can be used as a backup clock source (auxiliary clock) if the HSE crystal oscillator fails. It is the system clock after wake-up from Stop and Standby modes.	
LSE	32.768 kHz or 32.000 kHz configurable drive/consumption, available in the V_{DD} domain.	
LSI	LSI1 32 kHz low consumption (refer to the electrical characteristics sections of ([2] and [3]), available in the V_{DD} domain.	
	LSI2 24 kHz – 49 kHz high accuracy (refer to the electrical characteristics sections of the ([2] and [3]), available in the V_{DD} domain.	
Clock-out capabilities of the MCO and LSCO	One of the following clock signals can be selected as the microcontroller clock output (MCO): LSI, LSE, HSI16, HSE32, SYSCLKpre, pll1pclk, pll1qclk, pll1rclk, or hclk5	
	One of the following clock signals can be selected as the low-speed clock output (LSCO): LSI or LSE. This output remains available in Stop and Standby modes.	
Clock measurement and calibration using timers	LSI calibration using TIM16/TIM17/LPTIM1	
	HSI16 calibration using TIM16/TIM17/LPTIM2	
Interrupts	HSECSS (linked to NMI IRQ)	
	An interrupt vector equivalent to the one below is available for secure events, only when TrustZone® is enabled.	
	LSECSS	
	PLL1RDY	
	LSI1RDY, LSI2RDY, LSERDY, HSIRDY, and HSERDY	
	Audio synchronization CAF, COF, and CAEF	

7.8.1 PLL

The STM32WBA5xxx and STM32WBA6xxx MCUs embed the same fractional PLL, allows for 100 MHz clock generation.

7.8.2 Bus frequencies versus voltage scaling

The STM32WBA5xxx and STM32WBA6xxx MCUs embed the same voltage scaling. The table below lists the maximum frequencies of the internal bus in the STM32WBA5xxx and STM32WBA6xxx MCUs, depending on the voltage range of the product.

Table 22. Maximum bus frequency versus voltage scaling in the STM32WBA5xxx and STM32WBA6xxx MCUs

Product voltage range	STM32WBA5xxx	STM32WBA6xxx
Range 1	AHB1, AHB2, AHB4: maximum 100 MHz	
	AHB5: maximum 32 MHz	
Range 2	AHB1, AHB2, AHB4, AHB5: maximum 16 MHz	

7.8.3 CSS (clock security system)

The STM32WBA5xxx and STM32WBA6xxx MCUs embed the same CSS.

Table 23. CSS in the STM32WBA5xxx and STM32WBA6xxx MCUs

CSS clock source	STM32WBA5xxx	STM32WBA6xxx
CSS on HSE	Same features	
CSS on LSE modes	Same features	

7.8.4 Specific features of the ADC clock

The STM32WBA5xxx and STM32WBA6xxx MCUs embed the same ADC clocks and features, in particular:

- If a TIMx timer triggers the ADC precisely and with no any uncertainty, the HCLK must be selected as the ADC kernel clock source. The other clock sources are asynchronous to the TIMx timers. The LPTIMx timers are also asynchronous.

7.8.5 RTC and TAMP clocks

The STM32WBA5xxx and STM32WBA6xxx MCUs embed the same RTC and TAMP clocks. The table below lists the features of the RTC and TAMP clock sources for these two MCU.

Table 24. RTC and TAMP clocks in the STM32WBA5xxx and STM32WBA6xxx MCUs

Feature	STM32WBA5xxx	STM32WBA6xxx
Clock source for the RTC and TAMP	HSE32/32, LSE, or LSI	
Only the backup registers used in TAMP with tampers in edge-detection mode	No kernel clock required	
Active clocks of the backup domain	LSE and LSI	

7.8.6 Timer and watchdog clock sources

The hardware automatically defines the timer clock frequencies, with the following cases:

- If the APB prescaler equals one, the hardware sets the timer clock frequencies to the APB domain frequency.
- Otherwise, the hardware sets them to twice (× 2) the APB domain frequency.

If the hardware option or a software access starts the independent watchdog (IWDG), the LSI oscillator is forced on and cannot be disabled. After the LSI oscillator temporization, the 32 kHz LSI clock is provided to the IWDG.

7.8.7 Peripheral clock gating and reset

The peripheral clock gating and reset of the STM32WBA6xxx MCUs provide the same features as the STM32WBA5xxx MCUs. The RCC register mapping remains the same in the STM32WBA6xxx MCUs compared to the STM32WBA5xxx MCUs. The new peripherals of the STM32WBA6xxx MCUs were added to the RCC register map.

The table below shows the RCC registers used for peripheral access configuration in the STM32WBA5xxx and STM32WBA6xxx MCUs.

Table 25. RCC clock and reset registers in the STM32WBA5xxx and STM32WBA6xxx MCUs

Register	STM32WBA5xxx	STM32WBA6xxx
AHB: the AHB peripherals [enter/exit] reset	RCC_AHB1RSTR RCC_AHB2RSTR RCC_AHB4RSTR RCC_AHB5RSTR	
APB: the APB peripherals [enter/exit] reset	RCC_APB1RSTR1 RCC_APB1RSTR2 RCC_APB2RSTR RCC_APB7RSTR	
AHB: [enable/disable] the AHB peripheral clock	RCC_AHB1ENR RCC_AHB2ENR RCC_AHB4ENR RCC_AHB5ENR	
APB: [enable/disable] the APB peripheral clock	RCC_APB1ENR1 RCC_APB1ENR2 RCC_APB2ENR RCC_APB7ENR	
AHB: [enable/disable] the AHB peripheral clock in Sleep mode	RCC_AHB1SMENR RCC_AHB2SMENR RCC_AHB4SMENR RCC_AHB5SMENR	
APB: [enable/disable] the APB peripheral clock in Sleep mode	RCC_APB1SMENR1 RCC_APB1SMENR2 RCC_APB2SMENR RCC_APB7SMENR	

7.8.8 Peripheral clock source migration

The peripheral clock gating and reset of the STM32WBA6xxx MCUs provide the same features as the STM32WBA5xxx MCUs. The RCC register mapping remains the same in the STM32WBA6xxx MCUs compared to the STM32WBA5xxx MCUs. The new peripherals of the STM32WBA6xxx MCUs were added to the RCC register map.

Table 26. Peripheral clock sources in the STM32WBA5xxx and STM32WBA6xxx MCUs

Peripheral	STM32WBA5xxx	STM32WBA6xxx
IWDG	LSI	
WWDG	PCLK1	
RTC	LSE, LSI, or HSE/32	
LPTIMx (x = 1, 2)	HSI16, lsesys, LSI	

Peripheral	STM32WBA5xxx	STM32WBA6xxx
TIMx (x = 2, 3)	PCLK1	
TIM4(1)	N/A	PCLK1
TIMx (x = 1, 16, 17)	PCLK2	
USART2	HSI16, lsesys, PCLK1, SYSCLK	
USART3(1)	N/A	HSI16, lsesys, PCLK1, SYSCLK
USART1	HSI16, lsesys, PCLK2, SYSCLK	
LPUART1	HSI16, lsesys, PCLK7, SYSCLK	
SPI1	HSI16, PCLK2, SYSCLK	
SPI2(1)	N/A	HSI16, PCLK1, SYSCLK
SPI3	HSI16, PCLK7, SYSCLK	
I2C1	HSI16, PCLK1, SYSCLK	
I2Cx (x = 2, 4)(1)	N/A	HSI16, PCLK1, SYSCLK
I2C3	HSI16, PCLK7, SYSCLK	
SAI1	HSI16, SYSCLK, pll1pclk, pll1qclk, AUDIOCLK (external)	
OTG(1)	N/A	HSE, HSE/2, pll1pclk, pll1pclk/2
RNG	HSI16, lsesys, LSI, pll1qclk/2	
ADC4	HSI16, HCLK1, SYSCLK, HSE, pll1pclk	
CPU system timer	lsesys, LSI, HCLK1/8	HSI16/4, lsesys, LSI, HCLK1/8
GPIOx (x = A, B, C, H)	HCLK2	
GPIOx (x = D, E, G)(1)	N/A	HCLK2
VREFBUF(2)	N/A	PCLK7
COMP	PCLK7	
PKA	HCLK2	
AES	HCLK2	
TSC	HCLK1	
CRC	HCLK1	
RCC AUDIO synchronization	pll1pclk, pll1qclk	

1. *Only available on the STM32WBA62/64/65.*
2. *Only available on the STM32WBA62/65.*

7.8.9 System clock after wake-up

The system clock used after wake-up in the STM32WBA5xxx and STM32WBA6xxx MCUs is the same. The STM32WBA6xxx features some additional low-power modes.

Table 27. System source after wake-up in the STM32WBA5xxx and STM32WBA6xxx MCUs

Power mode	STM32WBA5xxx	STM32WBA6xxx
Sleep	Same clock as before entering Sleep mode	
Stop 0, Stop 1	HSI16 at 16 MHz	
Stop 2	N/A	HSI16 at 16 MHz
Standby	HSI16 at 16 MHz	

7.8.10 Autonomous peripheral mode

The STM32WBA5xxx and STM32WBA6xxx MCUs embed the same autonomous peripheral modes. The STM32WBA6xxx features some additional autonomous peripherals.

For the STM32WBA6xxx MCUs, some peripherals support an autonomous mode also in Stop 2 mode.

- The autonomous peripherals can generate a kernel clock request and a bus clock request when needed, even in Stop mode.
- The selected oscillator is woken up.
- In autonomous mode with DMA, the bus clocks and the oscillator (HSI16) are automatically switched off when the transfer completes. The device automatically goes back to the selected low-power mode.
- If the autonomous peripheral is configured with the interrupts enabled, the interrupts wake up the device into Run mode.

Furthermore, the following capabilities exist in Stop mode when needed:

- If USARTs, LPUARTs, and I2C select HSI16 as the kernel clock source, these peripherals can enable it in Stop 0, Stop 1, or Stop 2 mode.
- The LSE can remain always on in Stop mode, with no on-the-fly activation capability, when it drives the USARTs, LPUARTs, and LPTIMs.

The table below lists the main features of the autonomous mode supported by the STM32WBA5xxx and STM32WBA6xxx MCUs.

Table 28. Autonomous peripherals in the STM32WBA5xxx and STM32WBA6xxx MCUs

Feature	STM32WBA5xxx	STM32WBA6xxx
Stop 0 and Stop 1 retained peripherals	Autonomous peripherals in Stop 0 and Stop 1 modes only. Enabled if both the xxEN and xxSMEN bits of the peripheral are set (xx = instance name) GPDMA1 is associated. SRAM1 and SRAM2 are associated.	
Stop 2 retained peripherals	N/A	Autonomous peripherals in Stop 0, Stop 1 and Stop 2 modes. Enabled if both the xxEN and xxSMEN bits of the peripheral are set (xx = instance name). Autonomous peripherals mapped on AHB4 or APB7. No DMA association.
Autonomous peripherals in Stop 0 and Stop 1	USARTx (x = 1, 2)	
	N/A	USART3(1)
	LPUART1	
	SPIx (x = 1, 3)	
	N/A	SPI2(1)
	I2Cx (x = 1, 3)	
	N/A	I2Cx (x = 2, 4)(1)
	LPTIMx (x = 1 ,2)	
	ADC4	
	GPDMA1	
Autonomous peripherals in Stop 2 mode	N/A	LPUART1
		SPI3
		I2C3
		LPTIM1
Autonomous peripheral requesting its kernel clock in Stop mode	If the peripheral kernel clock request selects HSI16, the internal oscillator (HSI16) is woken up when off. The kernel clock is propagated only to the peripherals requesting it. When all peripheral kernel clock requests selecting HSI16 are released, the HSI16 is switched off.	

Feature	STM32WBA5xxx	STM32WBA6xxx
Autonomous peripheral requesting its bus clock in Stop 0 or Stop 1 mode	Stop 0 mode is entered. The internal oscillator (HSI16) is woken up when off. The system clock is propagated to all peripherals configured with both the xxEN and xxSMEN bits set. When all peripherals release their bus clock request, the system clock is stopped. Then, if all peripheral kernel clock requests selecting HSI16 are released, the HSI16 is switched off.	
Forcing HSI16 on in Stop mode	Can be done by configuring HSIKERON. The oscillator is propagated only to the kernel clock of the enabled autonomous peripherals with this oscillator selected as the kernel clock. This allows the peripheral baud rates or conversion rates to increase, as there is no need to wait the oscillator wake-up time when the peripheral requests its kernel clock.	
LSE or LSI as the kernel clock	The LSE or LSI selected as the peripheral kernel clock remains always on in Stop mode.	

1. *Only available on the STM32WBA62/64/65.*

7.8.11 Operating modes

The table below lists the main operating modes and main clock sources of the STM32WBA5xxx and STM32WBA6xxx MCUs.

Table 29. Operating modes in the STM32WBA5xxx and STM32WBA6xxx MCUs

Feature	STM32WBA5xxx	STM32WBA6xxx
Run	CPU running System clock active on PLL, HSI16, or HSE. The software can disable the peripheral bus and kernel clocks.	
Sleep mode	Stops the CPU HCLK clock. The software can stop the memory interface clocks during Sleep mode. The hardware disables the AHB-to-APB bridge clocks during Sleep mode, when all the clocks of the peripherals connected to them are disabled.	
Stop 0 mode	Stop the system clock when there is no autonomous peripheral bus clock request. Disable the PLL. Disable the HSI16 and HSE oscillators when no autonomous peripheral requests them.	
Stop 1 mode	Stop the system clock. Disable the PLL and the HSE oscillator. Disable HSI16 when no autonomous peripheral requests it.	
Stop 2 mode	N/A	Stop the system clock. Disable the PLL and the HSE oscillator. Disable HSI16 when no autonomous peripheral requests it.
Standby modes	Stop the system clock. Disable the PLLs, and HSI16 and HSE oscillators.	
LSE or LSI	Remain active in Stop mode and Standby mode.	
Low-power modes and memory/bus operation	If a programming operation is ongoing in the flash memory, Stop or Standby mode entry is delayed until the access to the flash memory interface is finished. If access to the APB domain is ongoing, Stop or Standby mode entry is delayed until the APB access is finished.	

7.8.12 RCC security and privilege, functional description

When TrustZone® security is activated, the RCC can ensure that no nonsecure access can modify the RCC configuration and status bits. The RCC_SECCFGR register is used in both the STM32WBA5xxx and STM32WBA6xxx MCUs to prevent nonsecure access from reading or modifying the items listed in the table below.

The security configuration bits in RCC_SECCFGR are the same for the STM32WBA5xxx and STM32WBA6xxx MCUs.

Table 30. Secured RCC items in the STM32WBA5xxx and STM32WBA6xxx MCUs

Feature	STM32WBA5xxx	STM32WBA6xxx
Configuration and status bits of the clock sources	HSE, HSECSS, HSI16, LSI, LSE, and LSECSS	
Configuration and status bits of the PLL, AHB, and APB prescaler	PLL1, AHB, and APB	
System and independent clocks	SYSCLK, SysTick	
Clockout capability	MCO and LSCO	
Remove reset flag settings	RMVF	

7.8.13 RCC privilege protection modes

In the STM32WBA5xxx and STM32WBA6xxx MCUs, there are the same dedicated register bits for privileged and unprivileged access: RCC_PRIVCFGR (SPRIV and NSPRIV bits).

By default, after a reset, all RCC registers can be read or written with privileged and unprivileged access, except RCC_PRIVCFGR that can be written with privileged access only.

7.9 Power (PWR)

The STM32WBA5xxx and STM32WBA6xxx MCUs have the same PWR features, except:

- The following STM32WBA6xxx features, not available in the STM32WBA5xxx MCUs:
  - Stop 2 mode
  - OTG (only available on the STM32WBA62/64/65 devices)
  - V_{DDIO2} and V_{REF+} power supplies (only available on the STM32WBA62/65 devices)

7.9.1 Power-supply pins

The STM32WBA5xxx and STM32WBA6xxx MCUs have the same power supplies. The STM32WBA6xxx MCUs support additional supply pins. The table below lists the differences between the STM32WBA5xxx and STM32WBA6xxx supply pins.

Table 31. Power-supply pins in the STM32WBA5xxx and STM32WBA6xxx MCUs

Pin name	
STM32WBA5xxx	**STM32WBA6xxx**
VDD	
N/A	VDDIO2(1)
N/A	VDDUSB(2)
VDDA	
N/A	VREF+(1)
VDDSMPS(3)	
VLXSMPS(3)	
VSSSMPS(3)	
VDD11(3), VCAP(4)	
VDDRF	
VDDRFPA	
VDDANA(3)	
VDDHPA	
VSSRF	
VSSA	
VSS	

1. *Only available on the STM32WBA62/65 devices.*
2. *Only available on the STM32WBA62/64/65 devices.*
3. *Only available on the STM32WBA63/65 devices.*
4. *Only available on the STM32WBA62/64 devices.*

The table below details pins that are specific to low-power modes.

Table 32. Specific pins in the STM32WBA5xxx and STM32WBA6xxx MCUs

Pin name	STM32WBA5xxx	STM32WBA6xxx
WKUPx	WKUPx (x = 1 to 8) input interrupt and wake-up pins Up to 16 multiplexed interrupt and wake-up pins from Run, Sleep, Stop, and Standby modes	
CSLEEP	CSLEEP output MCU in Sleep mode	
CSTOP	CDSTOP output CPU domain in Stop mode	

7.9.2 Power modes

The STM32WBA5xxx and STM32WBA6xxx MCUs support the same low-power modes. The STM32WBA6xxx MCUs additionally support Stop 2 mode. The table below shows the power modes of the STM32WBA6xxx MCUs compared to those of the STM32WBA5xxx.

Table 33. Power modes in the STM32WBA5xxx and STM32WBA6xxx MCUs

Power mode	STM32WBA5xxx	STM32WBA6xxx
Run mode	Run voltage scaling range 1	
	Run voltage scaling range 2	
Sleep mode	Sleep voltage scaling range 1 (entered from Run voltage range 1)	
	Sleep voltage scaling range 2 (entered from Run voltage range 2)	
Stop mode	SRAM pages can be powered down in Stop modes	
	Stop 0 voltage scaling range 1 (entered from Run voltage range 1)	
	Stop 0 voltage scaling range 2 (entered from Run voltage range 2)	
	Stop 1	
	N/A	Stop 2
Standby retention mode	SRAM pages, 2.4 GHz RADIO RAMs, and the sleep timer can be retained in Standby mode.	

7.9.3 Migrating the power management of peripherals

The power management of the peripherals of the STM32WBA6xxx MCUs provides the same features as the STM32WBA5xxx. The PWR register mapping remains the same in the STM32WBA6xxx MCUs compared to the STM32WBA5xxx. The power management of the new peripherals of the STM32WBA6xxx was added to the PWR register map.

Table 34. Peripheral power in the STM32WBA5xxx and STM32WBA6xxx MCUs

Peripheral	STM32WBA5xxx	STM32WBA6xxx
Low-power flags	STOPF	
	N/A	STOP2F
	SBF	
OTG supply(1)	N/A	USV, VDD11USBSWDLY, VDD11USBDIS, USBBOOSTEN, USBPWREN, USBBOOSTRDY, VDD11USBRDY
V_{DDIO2} supply(2)	N/A	IO2SV
SRAM1 retention	R1RSB1, SRAM1PDS1	
	N/A	R1RSB[4:2], R1RSB567, SRAM1PDS[4:2], SRAM1PDS567
SRAM2 retention	R2RSB1, SRAM2PDS	
ICACHE RAM retention	ICRAMPDS	N/A
PKA RAM retention	N/A	PKARAMPDS
OTG RAM retention(1)	N/A	PRAMPDS
2.4 GHz RADIO retention	RADIORSB	
State retention of the PTA signals in Stop 2 mode	N/A	PTASREN, PTASR
State retention of the GPIOs in Standby mode	GPIO PA[15:5, 2:1]: IORETEN, IORET	
	GPIO PA[4]: IORETEN, IORET(2)	

Peripheral	STM32WBA5xxx	STM32WBA6xxx
State retention of the GPIOs in Standby mode	GPIO PA[3]: IORETEN, IORET(1)	
	GPIO PA[0]: IORETEN, IORET(3)	
	GPIO PB[15:14, 12, 8, 4:0]: IORETEN, IORET	
	GPIO PB[13, 11:10]: IORETEN, IORET(1)	
	GPIO PB[9, 7:5]: IORETEN, IORET(3)	
	GPIO PC[15:13]: IORETEN, IORET	
	N/A	GPIO PC[12:0]: IORETEN, IORET(2)
	N/A	GPIO PD[15:10, 4:0]: IORETEN, IORET(2)
		GPIO PD[9:5]: IORETEN, IORET(1)
	N/A	GPIO PE[6:0]: IORETEN, IORET(2)
	N/A	GPIO PG[15:2]: IORETEN, IORET(2)
	GPIO PH[3]: IORETEN, IORET	

1. *These pins are only available on the STM32WBA62/64/65 devices.*
2. *These pins are only available on the STM32WBA62/65 devices.*
3. *These pins are only available on the STM32WBA62/63/65 devices.*

7.9.4 PWR security and privilege, functional description

When TrustZone® security is activated, the PWR can ensure that no nonsecure access can modify the PWR configuration and status bits. The PWR_SECCFGR register is used in both the STM32WBA5xxx and STM32WBA6xxx MCUs to prevent nonsecure access from reading or modifying the items listed in the table below.

The security configuration bits in PWR_SECCFGR are the same in the STM32WBA5xxx and STM32WBA6xxx MCUs.

Table 35. Secured RCC items in the STM32WBA5xxx and STM32WBA6xxx MCUs

Feature	STM32WBA5xxx	STM32WBA6xxx
Low-power mode configuration and status bits	SRAM RSB and DS bits, RADIORSB, LPMS, FLASHFWU, CSSF	
Voltage detection	PVDLS, PVDE, FSTEN, REGSEL	
Backup domain	DBP	
Wake-up pin	WKUP[8:1]	

7.9.5 PWR security and privilege

In the STM32WBA5xxx and STM32WBA6xxx MCUs, there are the same dedicated register bits for privileged and unprivileged access: PWR_PRIVCFGR (SPRIV and NSPRIV bits).

By default, after a reset, all PWR registers can be read or written with privileged and unprivileged access, except PWR_PRIVCFGR that can be written with privileged access only.

7.9.6 PWR interrupts

The table below lists the power interrupts sources of the STM32WBA5xxx and STM32WBA6xxx MCUs.

Table 36. PWR interrupt sources of the STM32WBA5xxx and STM32WBA6xxx MCUs

Interrupt vector	Description	Event flag	STM32WBA5xxx	STM32WBA6xxx
PWR_WKUP	Wake-up pin interrupt	WUFx(x = 1 to 8)	12 pins	
PWR_WKUPS	Secure interrupt of the wake-up pin			
PVD_PVM	Programmable voltage detector	PVDO	EXTI line 16	

7.10 CRC

The CRC architecture is the same in the STM32WBA5xxx and STM32WBA6xxx MCUs, with the same features.

8 Migrating the timer peripherals

The STM32WBA5xxx and STM32WBA6xxx MCUs embed the same timers with the same features. The STM32WBA6xxx MCUs have new timers and features.

8.1 Advanced-control timers (TIM1)

The STM32WBA5xxx and STM32WBA6xxx MCUs embed the same advanced-control timer, TIM1, with identical features.

The alternate function (AF) pins of the advanced timer TIM1 are mapped as described in the table below.

Table 37. TIM1 AF pins on the STM32WBA5xxx and STM32WBA6xxx MCUs

AF pin function	STM32WBA5xxx	STM32WBA63	STM32WBA64	STM32WBA62/65
TIM1_BKIN	PA2			
TIM1_BKIN2	PB15, PC13			
TIM1_ETR	PA15			
TIM1_CH1	PA11, PB8			
TIM1_CH1N	PA1, PB2			
TIM1_CH2	PA12			
TIM1_CH2N	PB1			
	PA0		N/A	PA0
TIM1_CH3	PB4			
TIM1_CH3N	PB0			
	PB9		N/A	PB9
TIM1_CH4	PB3			
TIM1_CH4N	PB7		N/A	PB7
	N/A	N/A	N/A	PC5

8.2 GP timers with up, down, and up-down auto-reload counters (TIM2/3/4)

The general-purpose timers consist of a 16-bit or 32-bit auto-reload counter driven by a programmable prescaler. The STM32WBA5xxx and STM32WBA6xxx MCUs embed the same general-purpose timers, TIM2 and TIM3, with identical features. The STM32WBA6xxx MCUs feature an additional timer, TIM4.

The AF pins of the general-purpose timers TIM2/3/4 are mapped as described in the table below.

Table 38. TIM2/3/4 AF pins on the STM32WBA5xxx and STM32WBA6xxx MCUs

AF pin	STM32WBA5xxx	STM32WBA63	STM32WBA64	STM32WBA62/65
TIM2_ETR	PA5			
	PB6		N/A	PB6
TIM2_CH1	PA5			
	PB6		N/A	PB6
TIM2_CH2	PA8			
TIM2_CH3	PA7			
TIM2_CH4	PA6			
TIM3_ETR	PB8, PB12			
	PA0		N/A	PA0

AF pin	STM32WBA5xxx	STM32WBA63	STM32WBA64	STM32WBA62/65
TIM3_ETR	N/A	N/A	N/A	PD2, PE2
TIM3_CH1	PA2, PA10			
	PB5		N/A	PB5
	N/A	N/A	N/A	PC3, PC6, PE3
TIM3_CH2	PA1, PA9			
	N/A	N/A	N/A	PC4, PC7, PE4
TIM3_CH3	PB14			
	PA0		N/A	PA0
	N/A	N/A	N/A	PC8, PE5
TIM3_CH4	PB9		N/A	PB9
	PB13	N/A	PB13	
	N/A	N/A	N/A	PC9, PE6
TIM4_ETR	N/A	N/A	N/A	PE0
TIM4_CH1		PB6	N/A	PB6
		N/A	N/A	PD12
TIM4_CH2		PB7	N/A	PB7
		N/A	N/A	PD13
TIM4_CH3		PB8		
		PB9	N/A	PB9
		N/A	N/A	PD14
TIM4_CH4		N/A	N/A	PD15

8.3 GP timers with an auto-reload upcounter (TIM16/17)

The STM32WBA5xxx and STM32WBA6xxx MCUs embed the same two 16-bit resolution general-purpose timers with a 16-bit auto-reload upcounter (TIM16 and TIM17) with identical features.

The AF pins of the GP timers TIM16/17 are mapped as described in the table below.

Table 39. TIM16/17 AF pins on the STM32WBA5xxx and STM32WBA6xxx MCUs

AF pin	STM32WBA5xxx	STM32WBA63	STM32WBA64	STM32WBA62/65
TIM16_BKIN	PB15			
	PB10	N/A	PB10	
TIM16_CH1	PA2			
	PB9		N/A	PB9
	PA4	N/A	N/A	PA4
	N/A	N/A	N/A	PE0
TIM16_CH1N	PB8			
	PA3	N/A	PA3	
TIM17_BKIN	PA15			
TIM17_CH1	PA1, PB4			
	N/A	N/A	N/A	PE1
TIM17_CH1N	PB3			

8.4 Low-power timers (LPTIM1/2)

The STM32WBA5xxx and STM32WBA6xxx MCUs embed the same two 16-bit resolution low-power timers with a 16-bit auto-reload upcounter (LPTIM1 and LPTIM2) with identical features.

The AF pins of the LP timers LPTIM1/2 are mapped as described in the table below.

Table 40. LPTIM1/2 AF pins on the STM32WBA5xxx and STM32WBA6xxx MCUs

AF pin function	STM32WBA5xxx	STM32WBA63	STM32WBA64	STM32WBA62/65
LPTIM1_ETR	PB8			
	PB11	N/A	PB11	
	N/A	N/A	N/A	PC3, PG12
LPTIM1_CH1	PB11	N/A	PB11	
	N/A	N/A	N/A	PC1, PG15
LPTIM1_CH2	PA8, PA15			
	N/A	N/A	N/A	PG14
LPTIM1_IN1	PA0		N/A	PA0
	N/A	N/A	N/A	PC0, PG10
LPTIM1_IN2	PB3			
	N/A	N/A	N/A	PC2, PG11
LPTIM2_ETR	PA5			
	N/A	N/A	N/A	PC3, PD11
LPTIM2_CH1	PA11			
	N/A	N/A	N/A	PD13
LPTIM2_CH2	PA1			
	N/A	N/A	N/A	PC4, PC7, PD10
LPTIM2_IN1	PB9		N/A	PB9
	N/A	N/A	N/A	PC0, PD12
LPTIM2_IN2	PB0, PB4			
	N/A	N/A	N/A	PD4

8.4.1 LPTIM autonomous mode

The STM32WBA5xxx and STM32WBA6xxx MCUs support LPTIM autonomous operation as described in the table below.

Table 41. SPI autonomous operation in the STM32WBA5xxx and STM32WBA6xxx MCUs

AF pin function	STM32WBA5xxx	STM32WBA6xxx
LPTIM1	Down to Stop 1 mode	Down to Stop 2 mode
LPTIM2	Down to Stop 1 mode	

8.5 Watchdogs

The STM32WBA5xxx and STM32WBA6xxx MCUs embed the same two watchdogs:

- A system window watchdog (WWDG) with the same features
- An independent watchdog (IWDG) with the same features

8.6 Real-time clock (RTC)

The STM32WBA5xxx and STM32WBA6xxx MCUs embed the same RTC with the same features.
The AF pins of RTC are mapped as described in the table below.

Table 42. RTC AF pins in the STM32WBA5xxx and STM32WBA6xxx MCUs

AF pin	STM32WBA5xxx	STM32WBA6xxx
RTC_REFIN	PB14	
RTC_TS	PC13	
RTC_OUT1	PC13	
RTC_OUT2	PB2	

8.7 SysTick timer

The Arm® Cortex®-M33 with TrustZone® technology of the STM32WBA5xxx and STM32WBA6xxx MCUs embed:

- Two SysTick timers when TrustZone® technology is activated
- Only one SysTick when TrustZone® technology is disabled

The STM32WBA6xxx supports an additional SysTick timer clock source.

Table 43. SysTick in the STM32WBA5xxx and STM32WBA6xxx MCUs

Feature	STM32WBA5xxx	STM32WBA6xxx
SysTick clock source	HCLK1 / 8	
	LSI	
	lsesys	
	N/A	HSI16 / 4

9 Migrating the communication peripherals

9.1 Serial peripheral interface (SPI)

The STM32WBA5xxx and STM32WBA6xxx MCUs embed the same SPI1 and SPI3 with identical features. The STM32WBA6xxx MCUs feature an additional SPI, SPI2.

The AF pins of SPI1/2/3 are mapped as described in the table below.

Table 44. SPI AF pins in STM32WBA5xxx and STM32WBA6xxx MCUs

AF pin function	STM32WBA5xxx	STM32WBA63	STM32WBA64	STM32WBA62/65
SPI1_MOSI	PA15			
	N/A	N/A	N/A	PG4
SPI1_MISO	PB3			
	N/A	N/A	N/A	PG3
SPI1_SCK	PB4			
	N/A	N/A	N/A	PG2
SPI1_NSS	PA12			
	N/A	N/A	N/A	PG5
SPI1_RDY	PA1, PB12			
	N/A	N/A	N/A	PG6
SPI2_MOSI	N/A	N/A	PB0	
			N/A	PC1, PC3
SPI2_MISO			PA9, PB14	
			N/A	PC2, PD3
SPI2_SCK			PA9, PB10, PB13	
			N/A	PD1, PD3
SPI2_NSS			PA10, PB9, PB12	
			N/A	PD0
SPI2_RDY			PB11	
			N/A	PC0
SPI3_MOSI	PB8			
	N/A	N/A	N/A	PC3, PC12, PD5, PG11
SPI3_MISO	PB9		N/A	PB9
	N/A	PA1		
	N/A	N/A	N/A	PC4, PC11, PG10
SPI3_SCK	PA0		N/A	PA0
	N/A	PA7		
	N/A	N/A	N/A	PC10, PG9
SPI3_NSS	PA5			
	N/A	N/A	N/A	PG12
SPI3_RDY	PA6, PA8			
	N/A	N/A	N/A	PG13

9.2 Inter-integrated circuit interface (I²C)

The STM32WBA5xxx and STM32WBA6xxx MCUs embed the same I2C1 and I2C3 with identical features. The STM32WBA6xxx MCUs features additional I² interfaces, I2C2 and I2C4.

The AF pins of I2CI1/2/3/4 are mapped as described in the table below.

Table 45. I2C AF pins in the STM32WBA5xxx and STM32WBA6xxx MCUs

AF pin function	STM32WBA5xxx	STM32WBA63	STM32WBA64	STM32WBA62/65
I2C1_SCL	PA15, PB2			
	N/A	N/A	N/A	PG14
I2C1_SDA	PB1, PB3			
	N/A	N/A	N/A	PG13
I2C1_SMBA	PB15			
	N/A	N/A	N/A	PG15
I2C2_SCL	N/A	N/A	PB10, PB13	
I2C2_SDA			PB11, PB14	
I2C2_SMBA			PB12	
I2C3_SCL	PA6, PB2			
	N/A	N/A	N/A	PC0, PG7
I2C3_SDA	PA7, PB1			
	N/A	N/A	N/A	PC1, PG8
I2C3_SMBA	PB15			
	N/A	N/A	N/A	PG6
I2C4_SCL	N/A	N/A	PB10	
			N/A	PD12
I2C4_SDA			PB11	
			N/A	PD13
I2C4_SMBA			PA14	
			N/A	PD11

9.2.1 Autonomous I²C mode

The STM32WBA5xxx and STM32WBA6xxx MCUs support autonomous I²C operation as described in the table below.

Table 46. Autonomous I²C operation in the STM32WBA5xxx and STM32WBA6xxx MCUs

AF pin function	STM32WBA5xxx	STM32WBA6xxx
I2C1	Down to Stop 1	
I2C2	N/A	Down to Stop 1
I2C3	Down to Stop 1	Down to Stop 2
I2C4	N/A	Down to Stop 1

9.3 U(S)ART and LPUART

The STM32WBA5xxx and STM32WBA6xxx MCUs embed the same USART1, USART2, and LPUART1 with identical features. The STM32WBA6xxx features an additional USART3.

The AF pins of USART1/2/3 and LPUART1 are mapped as described in the table below.

Table 47. U(S)ART/LPUART AF pins in the STM32WBA5xxx and STM32WBA6xxx MCUs

AF pin function	STM32WBA5xxx	STM32WBA63	STM32WBA64	STM32WBA62/65
USART1_TX	PB12, PB14			
	N/A	N/A	N/A	PG9
USART1_RX	PA8			
	N/A	N/A	N/A	PG10
USART1_CK	PA1, PA5			
	PB10	N/A	PB10	
	N/A	N/A	N/A	PG13
USART1_CTS	PA4	N/A	N/A	PA4
	PA7			
	N/A	N/A	N/A	PG11
USART1_RTS_DE	PA2, PA6			
	PA3	N/A	PA3	
	N/A	N/A	N/A	PG12
USART2_TX	PA12, PA14, PB0			
	N/A	N/A	N/A	PC9
	N/A	N/A	PD9	
USART2_RX	PA11, PB4			
	PB8		N/A	PB8
	N/A	N/A	N/A	PC8, PD5
USART2_CK	PB3			
	N/A	N/A	PD8	
USART2_CTS	PB2, PB15			
	N/A	N/A	N/A	PD3
USART2_RTS_DE	PA15, PB1			
	N/A	N/A	N/A	PC7
USART3_TX	N/A	N/A	PA7, PB10, PD9	
			N/A	PC4, PC10
USART3_RX			PA5, PB11	
			N/A	PC5, PC11, PD4
USART3_CK			PB0, PB12	
			N/A	PC12, PD10
USART3_CTS			PA6, PB13	
			N/A	PD11
USART3_RTS_DE			PA15, PB1, PB14	
			N/A	PD2, PD12
LPUART1_TX	PA2			

AF pin function	STM32WBA5xxx	STM32WBA63	STM32WBA64	STM32WBA62/65
LPUART1_TX	PB5		N/A	PB5
	PB11	N/A	PB11	
	N/A	N/A	N/A	PC1, PG7
LPUART1_RX	PA1, PA10			
	N/A	N/A	N/A	PC0, PG8
LPUART1_CTS	PA0		N/A	PA0
	PB15			
	N/A	N/A	N/A	PG5
LPUART1_RTS_DE	PA9			
	PB9		N/A	PB9
	N/A	N/A	N/A	PG6

9.3.1 Autonomous U(S)ART and LPUART mode

The STM32WBA5xxx and STM32WBA6xxx MCUs support autonomous U(S)ART and LPUART operation as described in the table below.

Table 48. Autonomous U(S)ART and LPUART operation in the STM32WBA5xxx and STM32WBA6xxx MCUs

AF pin function	STM32WBA5xxx	STM32WBA6xxx
USART1	Down to Stop 1	
USART2	Down to Stop 1	
USART3	N/A	Down to Stop 1
LPUART1	Down to Stop 1	Down to Stop 2

9.4 Serial audio interface (SAI)

The STM32WBA5xxx and STM32WBA6xxx MCUs embed the same SAI1 with identical features.
The AF pins of SAI1 are mapped as described in the table below.

Table 49. SAI AF pins in the STM32WBA5xxx and STM32WBA6xxx MCUs

AF pin function	STM32WBA5xxx	STM32WBA63	STM32WBA64	STM32WBA62/65
SAI1_SD_A	PB12, PB14			
	N/A	N/A	N/A	PC1, PC3, PD5, PE6, PG12
SAI1_FS_A	PA8			
	N/A	N/A	N/A	PC4, PE4, PG10
SAI1_SCK_A	PA7			
	N/A	N/A	N/A	PE5, PG9
SAI1_MCLK_A	PA6			
	N/A	N/A	N/A	PE2, PG7, PG11
SAI1_SD_B	PB7		N/A	PB7
	N/A	N/A	N/A	PC5, PE3, PG5
SAI1_FS_B	PB5		N/A	PB5
	N/A	N/A	N/A	PG3
SAI1_SCK_B	PB6		N/A	PB6
	N/A	N/A	N/A	PG2
SAI1_MCLK_B	PB4			
	N/A	N/A	N/A	PG4
SAI1_D1	PA2, PA10			
	N/A	N/A	PD5	
	N/A	N/A	N/A	PC3, PE6
SAI1_D2	PA5, PB5		N/A	PA5, PB5
	N/A	N/A	N/A	PC4, PE4
SAI1_D3	N/A	N/A	N/A	PC5
SAI1_CK1	PA1, PA9			
	N/A	N/A	N/A	PE2, PG7
SAI1_CK2	PA6			
	N/A	N/A	N/A	PE5

9.5 USB on-the-go high-speed interface (OTG)

In the STM32WBA6xxx MCUs, the USB on-the-go high-speed interface (OTG) was added.

The table below describes the mapping of the AF pins of OTG.

Note: OTG is only available on the STM32WBA62/64/65 devices.

Table 50. OTG pins in the STM32WBA5xxx and STM32WBA6xxx MCUs

Pin name	STM32WBA5xxx	STM32WBA63	STM32WBA62/64/65
OTG_SOF	N/A	N/A	PA8, PA14
OTG_ID			PD8
OTG_HSDM			PD7
OTG_HSDP			PD6
OTG_VBUS			PD9

10 Migrating the analog peripherals

10.1 Analog-to-digital converter (ADC)

The STM32WBA5xxx and STM32WBA6xxx MCUs embed the same 12-bit ADC4 with identical features.

The AF pins of ADC4 are mapped as described in the table below.

Table 51. ADC implementation in the STM32WBA5xxx and STM32WBA6xxx MCUs

AF pin function	STM32WBA5xxx	STM32WBA63	STM32WBA64	STM32WBA62/65
ADC4_IN1	PA8			
ADC4_IN2	PA7			
ADC4_IN3	PA6			
ADC4_IN4	PA5			
ADC4_IN5	PA4	N/A	N/A	PA4
ADC4_IN6	PA3	N/A	PA3	PA3
ADC4_IN7	PA2			
ADC4_IN8	PA1			
ADC4_IN9	PA0		N/A	PA0
ADC4_IN10	PB9		N/A	PB9

10.2 Comparator (COMP)

The STM32WBA5xxx and STM32WBA6xxx MCUs embed the same comparators, COMP1 and COMP2, with identical features.

The AF pins of COMP are mapped as described in the table below.

Note: COMP2 is only available on the STM32WBA62/63/65.

Table 52. COMP pins in the STM32WBA5xxx and STM32WBA6xxx MCUs

AF pin function	STM32WBA5xxx	STM32WBA62/63/65	STM32WBA64
COMP1_INP1	PA2		
COMP1_INM1	PA1		
COMP1_OUT	PA7, PB8		
COMP2_INP1	PA0		N/A
COMP2_INM1	PB9		
COMP2_OUT	PA12, PA14		

10.3 Voltage reference buffer (VREFBUF)

In the STM32WBA6xxx MCUs, a voltage reference buffer VREFBUF was added.

Note: VREFBUF is only available on the STM32WBA62/65.

11 Migrating the signal processing accelerators

11.1 Touch sensing controller (TSC)

The STM32WBA5xxx and STM32WBA6xxx MCUs embed the same touch sensing controller, TSC, with identical features. The STM32WBA6xxx MCUs feature additional groups: group 7 and group 8.

The AF pins of the TSC are mapped as described in the table below.

Table 53. TSC AF pins in the STM32WBA5xxx and STM32WBA6xxx MCUs

AF pin function	STM32WBA5xxx	STM32WBA63	STM32WBA64	STM32WBA62/65
TSC_SYNC	PB12			
	N/A	N/A	N/A	PD2
TSC_G1_IO1	PA8			
TSC_G1_IO2	PA7			
TSC_G1_IO3	PA6			
TSC_G1_IO4	PA5			
TSC_G2_IO1	PA1			
TSC_G2_IO2	PA0		N/A	PA0
TSC_G2_IO3	PB9		N/A	PB9
TSC_G2_IO4	PB8			
TSC_G3_IO1	PB4			
TSC_G3_IO2	PB3			
TSC_G3_IO3	PA15			
TSC_G3_IO4	PA12			
TSC_G4_IO1	PA4	N/A	N/A	PA4
TSC_G4_IO2	PA3	N/A	PA3	
TSC_G4_IO3	PB10	N/A	PB10	
TSC_G4_IO4	PA2			
TSC_G5_IO1	PC13			
TSC_G5_IO2	PB7		N/A	PB7
TSC_G5_IO3	PB6		N/A	PB6
TSC_G5_IO4	PB5		N/A	PB5
TSC_G6_IO1	PB14			
TSC_G6_IO2	PB13	N/A	PB13	
TSC_G6_IO3	N/A	N/A	N/A	PD12
TSC_G6_IO4				PD13
TSC_G7_IO1				PE3
TSC_G7_IO2				PE2
TSC_G7_IO3				PE1
TSC_G7_IO4				PE0
TSC_G8_IO1				PD3
TSC_G8_IO2				PD1
TSC_G8_IO3				PD0
TSC_G8_IO4				PD15

12 Migrating the software

For further details on the information provided in this chapter, refer to [5] and [6].

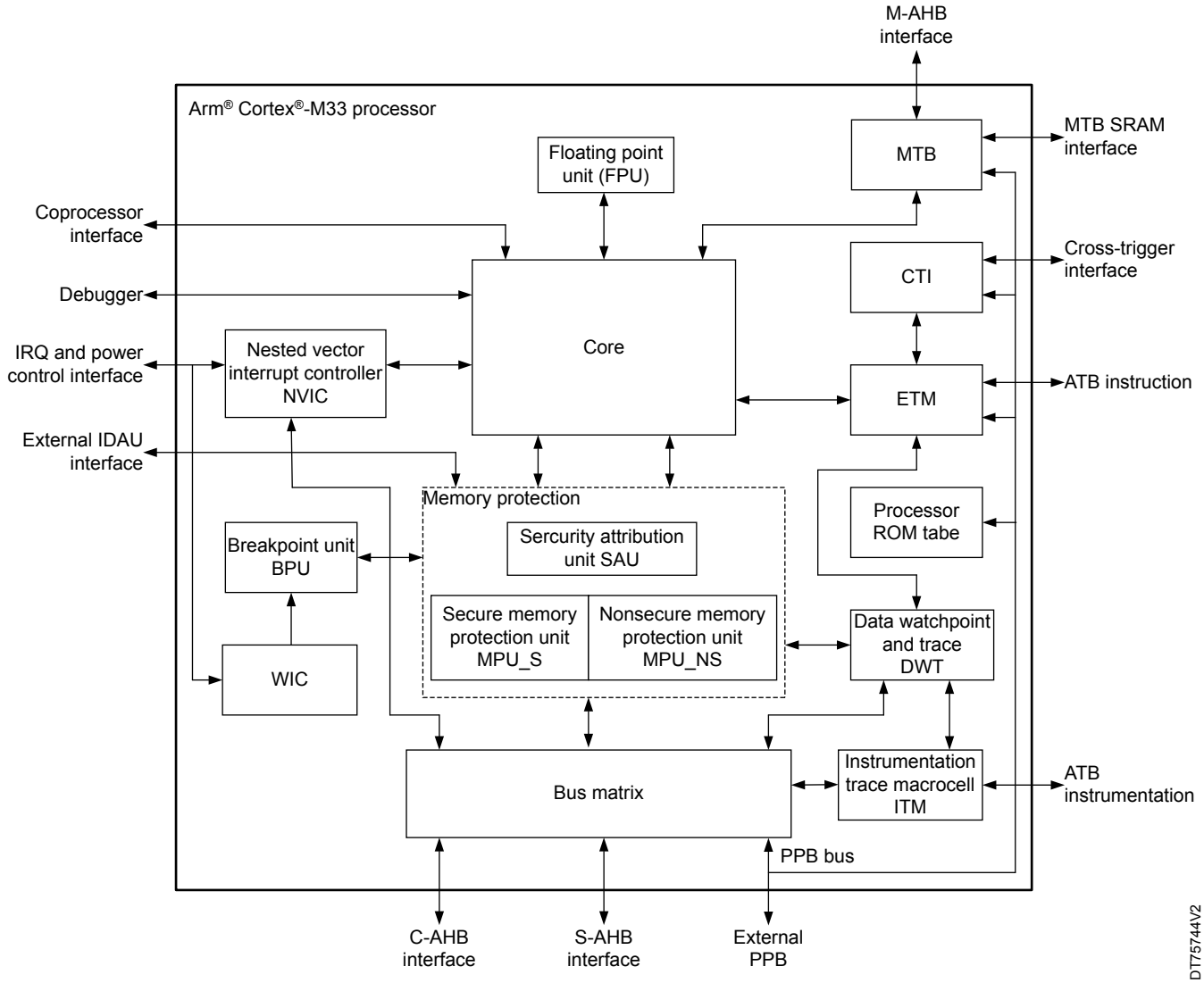
12.1 Arm® Cortex®-M33 overview

The Arm® Cortex®-M33 processor provides excellent ultra-low-power, performance, and security features. This processor is based on the Armv8-M architecture for use in environments that require more security implementation. The Arm® Cortex®-M33 core implements:

- A full set of DSP (digital signal processing) instructions
- TrustZone® aware support
- A memory protection unit (MPU) that enhances application security

The Arm® Cortex®-M33 core also features a single-precision floating-point unit (FPU), which supports all the Arm® single-precision data-processing instructions and all the data types. The figure below illustrates the STM32 Arm® Cortex®-M33 implementation.

Figure 3. STM32 Arm® Cortex®-M33 implementation



The Arm® Cortex®-M33 core has the key features listed below:

- Arm-v8M architecture with a 2- or 3-stage pipeline, Harvard, 1.5 DMIPS/MHz
- Single-cycle branch, no branch prediction
- Hardware divide instruction
- Debug (CoreSight™-compliant)
- Memory-exclusive instructions
- NVIC without interrupts increased to up to 82 (16 priority levels)
- Enhanced MPU, more flexible (32 bytes) up to 8 regions (for each of the secure and nonsecure states)
- New AMBA®5 AHB interface, which supports security state extension to the system
- Support for an external implementation-defined attribution unit
- Fully compatible with the TrustZone® system

12.2 Arm® Cortex®-M33 software point of view

The Arm® Cortex®-M33 includes the following features:

- It implements the Armv8-M architecture.
- It implements the latest FPU specification (based on the Arm® FPv5 architecture).
- It uses the AHB5 specification for the system and memory interface to extend security across the whole system.
- It uses the latest version of the MPU specification for the setup of regions.
- It provides optional execution trace using MTB or ETM.
- It integrates enhanced debug components to simplify debugging.
- It implements hardware stack limit checking.
- It has TrustZone® security features, which deliver efficient security.

12.3 Arm® Cortex®-M33 mapping overview

The table below illustrates the mapping on the Arm® Cortex®-M33 core.

Table 54. Arm® Cortex®-M33 overview mapping for the STM32WBA5xxx and STM32WBA6xxx MCUs

Architecture		STM32WBA5xxx	STM32WBA6xxx
Core	NVIC (nested vectored interrupt controller), not including the 16 interrupt lines of the Arm® Cortex®-M33 with FPU)	72	82
	EXTI (extended interrupt and event controller)	19	21
Mapping (base address)	Instrumentation trace macrocell (ITM)	0xE000 0000	
	Data watchpoint and trace unit (DWT)	0xE000 1000	
	Breakpoint unit (BPU)	0xE000 2000	
	System control space (SCS)	0xE000 E000	
	System timer	0xE000E010	
	Nested vectored interrupt controller (NVIC)	0xE000E100	
	MPU	0xE000ED90	
	Floating-point unit (FPU)	0xE000EF30	
	Trace port interface unit (TPIU)	0xE004 0000	
	ETM (1)	N/A	0xE004 1000
	Cross-trigger interface (CTI)	0xE004 2000	
	Debug MCU controller (DBGMCU)	0xE004 4000	
	Processor ROM table	0xE00F F000	

1. *Only available on the STM32WBA62/65 devices.*

13 Conclusion

This application note is a complement to the datasheets and reference manuals of the STM32WBA5xxx and STM32WBA6xxx MCUs (refer to Reference documents). This document provides a simple guideline to migrate an existing product based on the STM32WBA5xxx to the STM32WBA6xxx MCUs.

Revision history

Table 55. **Document revision history**

Date	Revision	Changes
19-Feb-2025	1	Initial release.

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