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Application note

Guidelines for crystal oscillator design on ST25 NFC readers

Introduction

This document applies to products belonging to the ST25 NFC Readers series. It describes how to select and design an oscillator circuit to achieve optimum crystal performance.

The need for reliable and accurate data transmission is greater than ever. One of the key components in achieving this is the quartz crystal, a passive component used as a resonator to generate a stable and accurate frequency for data transmission.

In NFC devices, the crystal is used as a resonator to generate a carrier frequency for data transmission. The crystal is connected to an oscillator circuit that adjusts the frequency of the AC signal until it matches the natural frequency of the crystal. To ensure a fast start of the oscillation and to obtain the required stable and precise oscillation frequency, it is essential to ensure optimum oscillation circuit conditions.

1 Terms and acronyms

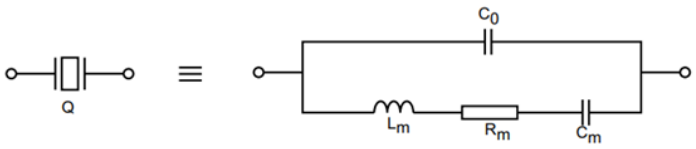
Table 1. Terms and acronyms

Acronym	Description
ESR	Equivalent series resistance
MCU	Microcontroller unit
PCB	Printed circuit board
NFC	Near field communication
ppm	Parts per million

2 Quartz crystal properties and model

A quartz crystal is a piezoelectric device that converts electrical energy into mechanical energy and vice versa. The conversion takes place at the mechanical resonant frequency. The simplified model in Figure 1 includes only the fundamental frequency of oscillation.

Figure 1. Quartz crystal model



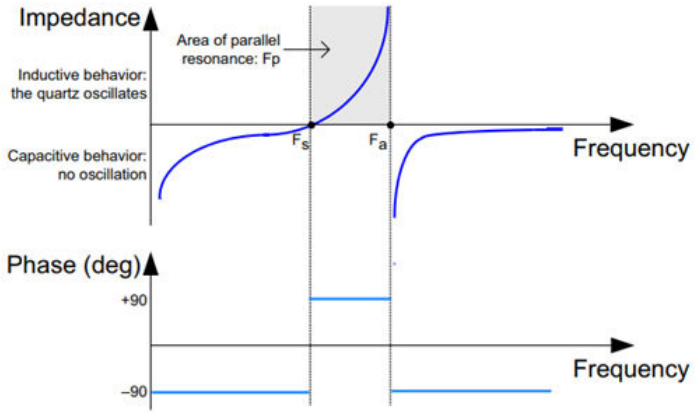
- C_0 (parallel capacitance) is the shunt capacitance resulting from the capacitor formed by the electrodes.
- L_m (motional inductance/equivalent series inductance) is the vibrating mass of the crystal.
- C_m (motional capacitance/equivalent series capacitance) is the elasticity of the crystal.
- R_m (motional resistance/equivalent series resistance) accounts for the circuit losses.

The impedance of the crystal (assuming that the R_m is negligible) is:

$$Z = \frac{j}{w} \times \frac{w \times L_m \times C_m - 1}{(C_0 + C_m) - w^2 \times L_m \times C_m \times C_0} \quad (1)$$

Figure 2 shows the impedance in the frequency domain.

Figure 2. Impedance in the frequency domain



F_s is the series resonant frequency when Z = 0. Its expression can be deduced from equation 1 as follows:

(2)

$$F_s = \frac{1}{2\pi\sqrt{L_m C_m}}$$

F_a is the antiresonant frequency when Z tends to infinity. Using equation 1, it is expressed as follows:

(3)

$$F_a = F_s\sqrt{1 + \frac{C_m}{C_0}} = \frac{1}{2\pi\sqrt{L_m \times \frac{C_m \times C_0}{C_m + C_0}}}$$

As specified in the datasheet of the crystal, the frequency of oscillation is between the resonance frequencies:

(4)

$$F_s < f < F_a$$

The region between F_s and F_a (shaded in Figure 2) is the parallel resonance region. The crystal acts as a parallel resonant inductor, adding 180 degrees to the phase of the loop. Its frequency F_p (or F_L: load frequency) has the following expression:

(5)

$$F_p = F_s\left(1 + \frac{C_m}{2(C_0 + C_L)}\right)$$

In accordance with this equation, the oscillation frequency of the crystal can be tuned by the variation of the load capacitance C_L. For this reason, crystal manufacturers specify in their datasheets the exact C_L required to make the crystal oscillate at the nominal frequency.

3 Crystal parameters

ESR (equivalent series resistance)

ESR is the total resistance of all components in the oscillator circuit. It affects the stability and frequency accuracy of the oscillator. A higher ESR can cause the oscillator to drift more and be less accurate. The ESR includes the resistive components within the crystal, and affects the overall quality factor (Q) of the crystal resonance.

$$ESR = R_M \left(1 + \frac{C_0}{C_L}\right)^2 \quad (6)$$

As C_0 is typically of the order of 1 pF and C_L is 5-9 pF, the ESR for many crystals is approximately R_M. Sometimes the ESR is approximated as the motional resistance.

Low ESR is essential to minimize losses and maintain a stable clock signal, so these crystals are preferred due to their effect on signal quality. Note that the choice of low ESR crystal may be limited by the requirements of the specific device. Higher ESR can lead to signal degradation, affecting the communication range and reliability of the device. It is therefore important to carefully consider the device specifications and limitations when selecting a crystal for NFC applications.

Drive level

This is the amount of power required to drive the oscillator, it is usually measured in mW or decibels (dBm). The drive level must be within the specified range for the oscillator to work properly. If the drive level is too low, the oscillator may not start or be unstable. Exceeding this value may damage the crystal or shorten the life of the device

The formula DL = ESR x I_Q^2 gives the drive level, where I_Q is the RMS current flowing through the crystal. This current can be displayed as a sine wave on an oscilloscope. The current value can be read as the peak-to-peak value (I_{PP}).

Load capacitance

This parameter determines the frequency and stability of the oscillator. It is specified in picofarads (pF), and is the capacitance that must be connected to the oscillator for it to operate correctly. The load capacitance is determined by the external capacitors C_{L1} and C_{L2}, the stray capacitance (C_S) of the PCB and connectors, and the input/output capacitance (C_{IC}) of the IC. The stray capacitance can be assumed to be in the range of 1 to 5 pF. The C_L value is specified by the crystal manufacturer and must be within the specified range for the oscillator to operate at the desired frequency. External capacitors C_{L1} and C_{L2} are used to adjust the desired value of C_L to match the specified value. It is important to maintain a constant load capacitance for frequency stability as any deviation from the specified value may cause the oscillator to become unstable or operate at an incorrect frequency. The load capacitance is required for parallel resonant crystals, not required for series resonant crystals.

The following equation gives the expression of C_L:

$$C_L = \frac{C_{L1} \times C_{L2}}{C_{L1} + C_{L2}} + C_S + C_{IC} \quad (7)$$

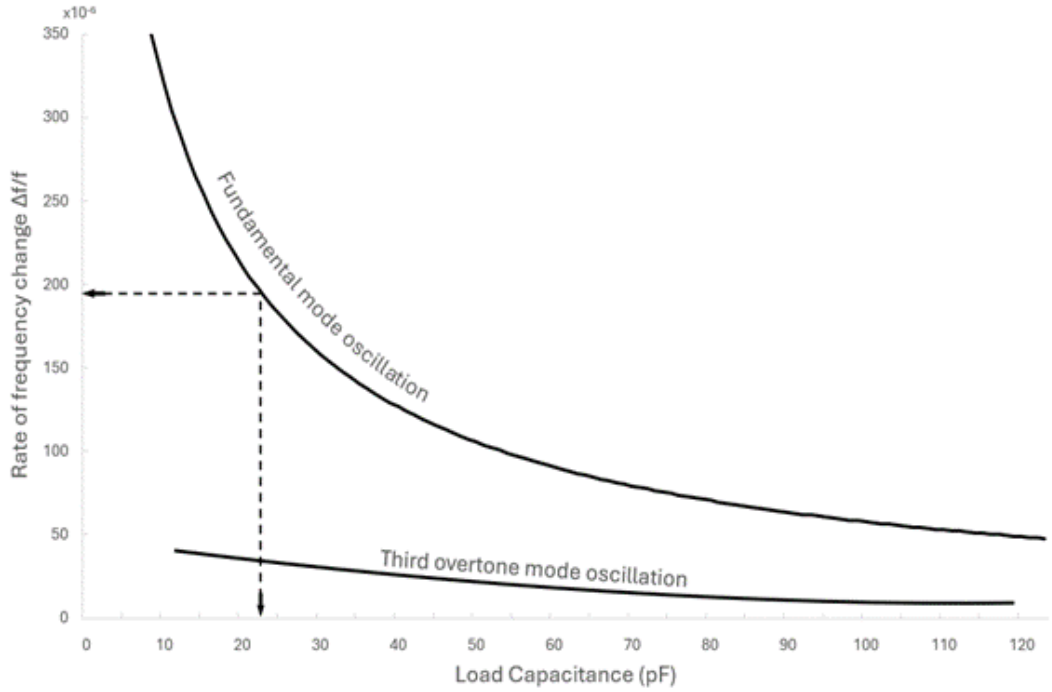
If C_L = 10 pF, C_s = 4 pF and C_{IC} = 1 pF:

$$C_L - C_S - C_{IC} = \frac{C_{L1} \times C_{L2}}{C_{L1} + C_{L2}} = 5pF \quad (8)$$

Then C_{L1} = C_{L2} = 10 pF

As already mentioned in equation 5, Figure 3 shows this relation.

Figure 3. Load capacitance vs frequency change



Because the motional (series) capacitance C_m values of the overtoned mode oscillation are smaller, the rate of frequency change for an overtone mode oscillation is lower than for a fundamental mode oscillation. Comparing crystals of the same frequency, smaller crystals have smaller C_m values. This means that smaller crystals have less rate of frequency change due to the load capacitance. The shape and cut of the crystal can also affect the rate of frequency change, with crystals with a higher overtone mode having a larger C_m value and therefore a higher rate of frequency change.

4 Negative resistance (oscillation allowance)

Negative resistance is a parameter in quartz oscillator circuits. It encompasses all the components of the oscillator circuit, including capacitor values, crystal parameters and on-chip circuitry. It plays a key role in ensuring stable oscillations, particularly during startup and steady-state operation, while also influencing power consumption.

The oscillation margin is a fundamental indicator of a circuit's amplification capability. It is expressed as a ratio based on the crystal resistance. It acts as a crucial buffer against oscillation arrest, representing the circuit's ability to sustain oscillations under varying conditions.

In theory, a resonant circuit can operate with an absolute margin of 1 or more. However, approaching this threshold carries a risk of operational failure. Problems such as excessive startup time and other instabilities can occur as the margin approaches 1. To mitigate such risks, a larger oscillation margin is advisable.

In summary, negative resistance and oscillation margin are of paramount importance in crystal oscillator circuits to ensure reliable operation, stability, and optimum performance over a range of conditions. Understanding and managing these parameters is essential to the design of robust and efficient oscillator systems.

Calculation of negative resistance

The values of the additional resistor indicate the oscillation allowance, as shown in Figure 4.

$$Oscillation\ margin[times] = \frac{|-R|}{R_{ESRmax}} \quad (9)$$

Where:

- |-R| is the negative resistance

and

- R_{ESRmax} is the maximum value of equivalent series resistance of crystal unit specified.

A variable resistor is temporarily placed in series with the crystal unit to evaluate the negative resistance in a circuit. This resistor is initially set to its lowest possible value, ideally close to zero ohms, to begin the measurement process.

Once the variable resistor is in place, the oscillator is activated and its output is closely monitored on an oscilloscope.

Note: The oscilloscope probe has a parasitic capacitance of about 9.5 pF, whereas an active probe has about 1 pF

However, this does change the load capacitance. This means that attaching the probe changes the initial behavior of the crystal. The next step is to carefully adjust the variable resistor to gradually increase its resistance value. Throughout this adjustment phase, the output must be continuously monitored on the oscilloscope to detect any changes in the oscillation behavior of the circuit.

As the resistance is increased, a point is reached where the oscillation stops. This resistance value is critical as it indicates the threshold at which the circuit stops oscillating. At this point, the resistance value of the variable resistor (R_{s_max}) is measured to determine the ohmic value at which the oscillation stopped.

The effective resistance R_L is calculated by the formula:

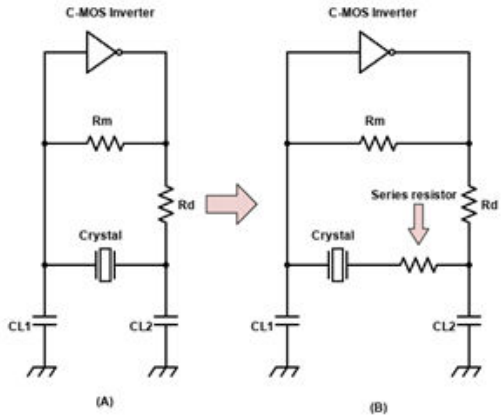
$$R_L \approx R_m \left(1 + \frac{C_0}{C_m}\right)^2 \quad (10)$$

$$C_s = \frac{C_m}{2} \frac{1}{\left(\frac{f_{osc}}{f_s}\right) - 1} - C_0 \quad (11)$$

$$f_s \approx \frac{1}{2\pi\sqrt{L_m C_m}} \quad (12)$$

Figure 4 shows on (A) general oscillation circuit is shown, with R_d as damping resistor C-MOS invertor (which are both included in MCU), and on (B) the series resistor is added to crystal for measuring the negative resistance.

Figure 4. (A) General oscillation circuit – (B) circuit for measuring negative resistance



To calculate negative resistance |-R|, needs to add the effective resistance R_L to the maximum of variable resistor R_{s_max}:

(13)

$$|-R| = Rs\_max + R_L$$

This negative resistance should be at least five times the specified maximum equivalent series resistance of the crystal unit for the circuit to operate reliably and effectively. In fact, values greater than five times are considered even more beneficial to circuit performance.

Performing this test at the highest temperature in the circuit's operating range is also recommended. This comes from observing that negative resistance tends to decrease as the temperature rises. By testing under these conditions, the user can ensure that the oscillator maintains stable performance even at elevated temperatures, thus guaranteeing its reliability over the entire operating range.

5 Stability assessment

Selecting a quartz oscillator for NFC applications requires a comprehensive stability evaluation to ensure reliable and accurate performance. The frequency stability, temperature sensitivity and aging characteristics of the oscillator are fundamental considerations.

One such parameter is the resonator ESR, which is a function of environmental factors such as humidity and temperature. Supply voltage and temperature also affect the transconductance of the oscillator.

When evaluating the aging rate and design for aging compensation features, alongside frequency tolerance, one can ensure that reliability and maintenance needs are met. Considering these aspects can help make an informed decision when selecting a quartz oscillator that meets application requirements for accurate, reliable performance.

5.1 Temperature influence

The frequency stability of an NFC crystal oscillator can be significantly influenced by temperature variations. The inherent properties of the crystal material cause its physical dimensions and resonance characteristics to shift as temperature changes, which can cause the output frequency of the oscillator to drift. To minimize this effect, manufacturers often employ temperature compensation techniques, such as adding temperature-sensitive components or employing digitally controlled oscillators.

If it is not possible to meet the temperature stability requirements due to cost, limited board space or other reasons, manufacturers often provide information on the frequency shift with temperature and the operating temperature range (for example, -30 °C to +85 °C) in the datasheet. To ensure optimum performance. It is recommended to select an NFC crystal oscillator with the lowest possible ppm value for frequency shift with temperature (for example, ± 20 ppm max).

5.2 Crystal pullability

Pullability, denoting the frequency change near parallel resonance, becomes crucial when tuning a crystal within a specific range. It depends on shunt capacitance C_s and motional capacitance C_m. If pullability is not specified, tuning hazards may arise, risking frequencies outside the operational range.

Crystal pullability, synonymous with crystal sensitivity, measures the effect of small variations in load capacitance C_L on the frequency shift, which is particularly important in low-speed oscillators for time-keeping functions such as real-time clocks.

Changes in the capacitance load C_L directly shift the vibration frequency. In production, accurate control of these capacitances is a challenge. Choosing a crystal with low pullability minimizes the influence of manufacturing uncertainties on the final frequency accuracy. In general, a higher load capacitance corresponds to a lower pullability. For example, a crystal with a pullability of 45 ppm/pF loaded with two ±5% tolerant 7 pF C0G ceramic capacitors (C_{L1} and C_{L2}) shows the effect on load capacitance.

Considering $C_{L1} = C_{L2}$ mounted in series, their contribution to C_L is ($C_{L1} = C_{L2}$)/2, with a ±5% tolerance. If other contributors to CL maintain nominal values, load capacitance can decrease or increase by 0.175 pF, inducing an oscillation shift of:

0.175 pF × 45 ppm/pF ~ 7.8 ppm (~0.7 s/day for timekeeping function as real-time clock).

This example illustrates that lower pullability reduces the impact of small load capacitance deviation on frequency shifting.

$$\text{Pullability}_{(\text{PPM/pF})} = \frac{C_m \times 10^6}{2 \times (C_s + C_L)^2} \quad (14)$$

Crystal pullability has a significant influence on the final ppm budget of the application, which includes crystal motion capacitance (C_m), shunt capacitance (C_s) and nominal load capacitance (C_L). The following sections provide a detailed insight into the calibration of the oscillation frequency and the estimation of the final ppm budget.

6 Tolerance and NFC standard compliance

The NFC ISO/IEC 14443 compliant devices operate at a base frequency of 13.56 MHz with an allowed tolerance of ±7 kHz. This means that the quartz oscillator used in NFC applications can have a frequency tolerance of up to 14 kHz to remain within the specifications of the ISO 14443 standard. It is important to select a quartz oscillator with a tolerance able to meet this requirement. Typical values for 27.12 MHz crystal oscillators range from ±10 to ±50 ppm.

6.1 Crystal requirements

The quartz oscillator is a critical component in an NFC system and must meet several requirements to ensure reliable and accurate communication between devices. The main requirements for the quartz oscillator used in an NFC application are summarized in the table below, along with recommended limits.

Table 2. Crystal parameters for ISO/IEC14443 compatibility

Parameter	Min.	Typ.	Max.	Unit
Crystal frequency	-	27.12	-	MHz
Crystal frequency accuracy preference	-50	-	+50	ppm
Load capacitance C_L	4	8	10	pF
Equivalent series resistance ESR	10	30	100	Ω
Frequency shift by temperature	-20	-	20	ppm
Aging	-	-	5	ppm/year

Note: Most datasheets do not give a value for the parallel capacitance, so it is necessary to request the data from the manufacturer or make a measurement with a network analyzer.

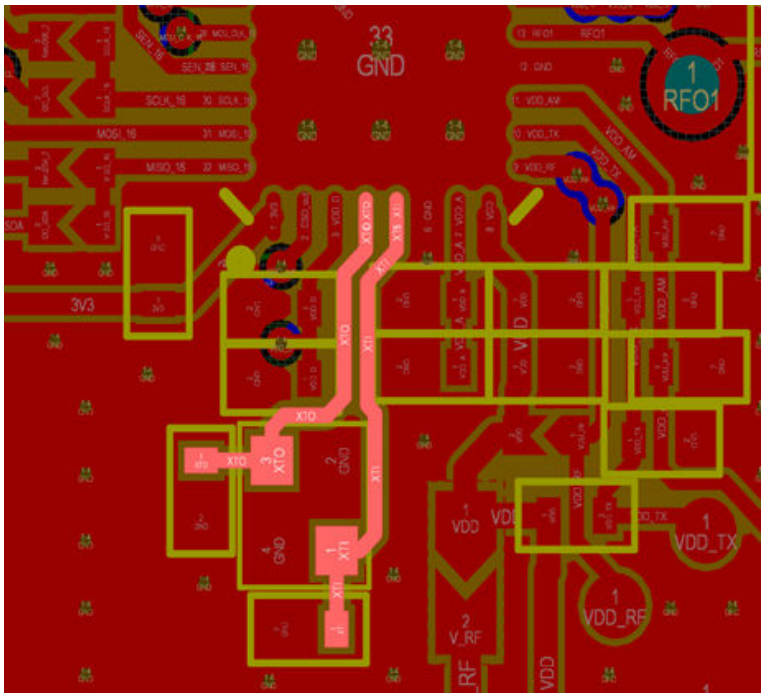
Working temperature according to the NFC IC operating temperature range.

7 Crystal placement and PCB design guidelines

When designing a printed circuit board (PCB), the correct placement and routing of the crystal oscillator is critical to the stability and performance of the oscillator circuit. Consider the following guidelines/suggestions when placing a crystal on a PCB:

- The crystal oscillator must be placed as close as possible to the XTI/XTO pins, to minimize trace lengths
- To avoid crosstalk from other signals (for example XTO <-> RESET), these PCB tracks must be separated by a GND area.
- The GND plane must be around the oscillator
- Ensure that the crystal and its load capacitors are away from high-speed signals, power supplies and other sources of noise
- The ideal routing from IC to crystal must be direct, with no vias or sharp bends to maintain signal integrity
- Place the load capacitors as close as possible to the crystal pins with a direct path to the ground. Ideally there should be symmetry between the capacitors
- Avoid or minimize test points

Figure 5. Example of board placement and routing for the crystal for the ST25R100



8 Conclusion

This application note provides an overview of the fundamentals of quartz oscillators for NFC applications. However, it is important for product design engineers to conduct further research and consult with crystal manufacturers to ensure the selection of the appropriate crystal for their specific needs. During the experimentation phase, it is recommended to use components with the same characteristics as those that will be used in production to avoid unexpected behavior.

A full understanding of the crystal requirements for ISO/IEC14443 compliance is a key factor in successful product design and operation.

Revision history

Table 3. **Document revision history**

Date	Version	Changes
28-Jun-2024	1	Initial release.

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