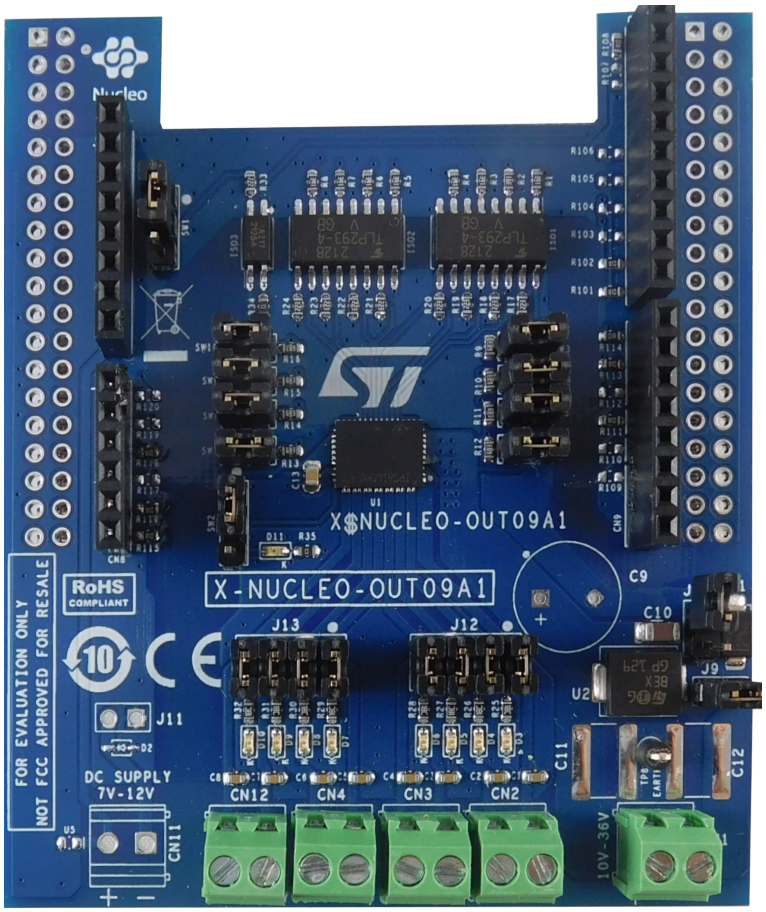
Designing industrial applications with IPS8160HQ/IPS8160HQ-1 high-side drivers

Introduction

This application note describes the functions of IPS8160HQ/IPS8160HQ-1 high-side drivers in industrial applications and covers the various tests used to ensure compliance with international electromagnetic compatibility (EMC) specifications as well as other requirements.

IPS8160HQ/IPS8160HQ-1 high-side drivers are mounted on their respective reference design boards, the X-NUCLEO-OUT09A1 and X-NUCLEO-OUT19A1 respectively.

Figure 1. IPS8160HQ (IPS8160HQ-1) reference design board



1 Device description

Monolithic devices built with ST's robust VIPower technology, the IPS8160HQ and IPS8160HQ-1 high-side switches are designed to drive any type of capacitive, resistive, or inductive industrial load with one side connected to ground.

The ICs can be driven by using 3.3 V logic signals, and they differ for the internal current limitations, 0.7 A per channel for the IPS8160HQ and 1.0 A for the IPS8160HQ-1; all other electrical parameters are the same.

Each of the eight output stages is a fully protected N-channel power MOSFET with a maximum RDS(on) of 160 mΩ @ 25 °C.

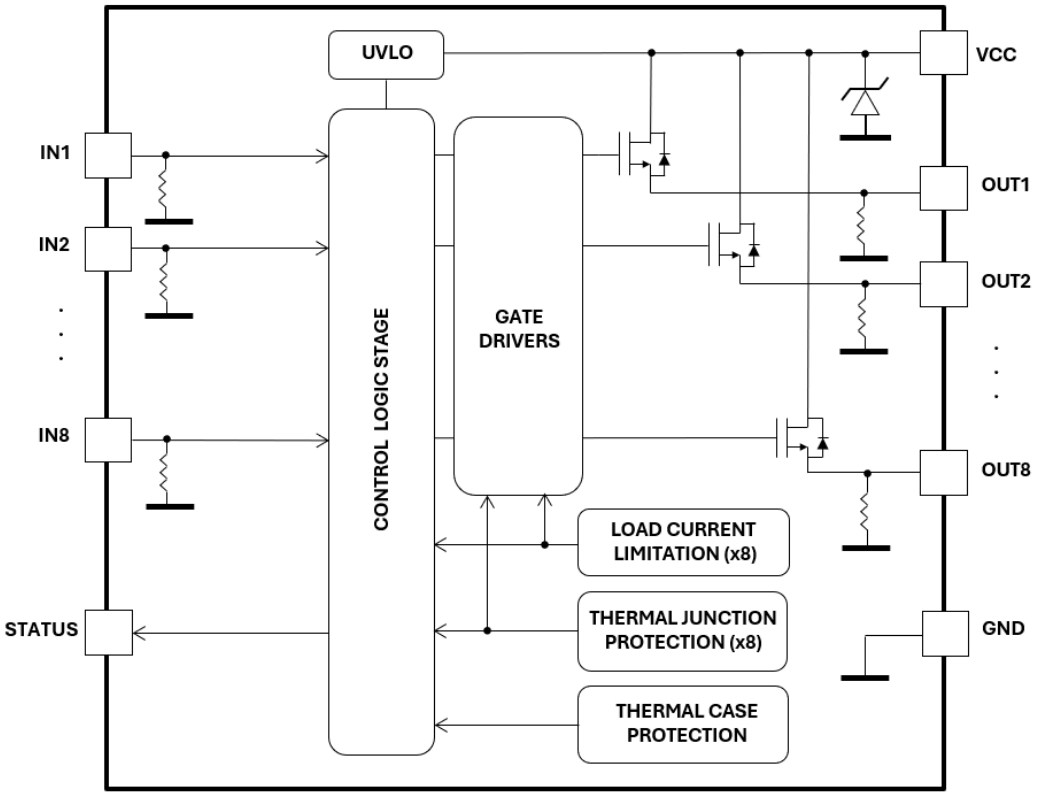
Active current limitation, combined with thermal shutdown and automatic restart, protects the devices against overload.

Available in a compact 48-pin QFN (8 x 6 mm) package, these intelligent power switches are ideal for space constrained industrial applications in compliance with IEC 61000-4-2 (ESD), IEC 61000-4-4 (EFT/Burst), and IEC 61000-4-5 (Surge) immunity standards.

Main characteristics

- Operating output current: 0.7 A (IPS8160HQ) or 1.0 A (IPS8160HQ-1) per channel
- CMOS compatible input
- Very low standby current
- Undervoltage shutdown
- Overload and short-circuit protection with output current limitation
- Junction overtemperature protection
- Case overtemperature protection for thermal independence of the channels
- Protection against loss of ground
- Thermal shutdown diagnostic pin
- Designed to meet IEC 61000-4-2, IEC 61000-4-4, IEC 61000-4-5
- UL 2367 certified
- Package: QFN48L 8x6x0.9 mm

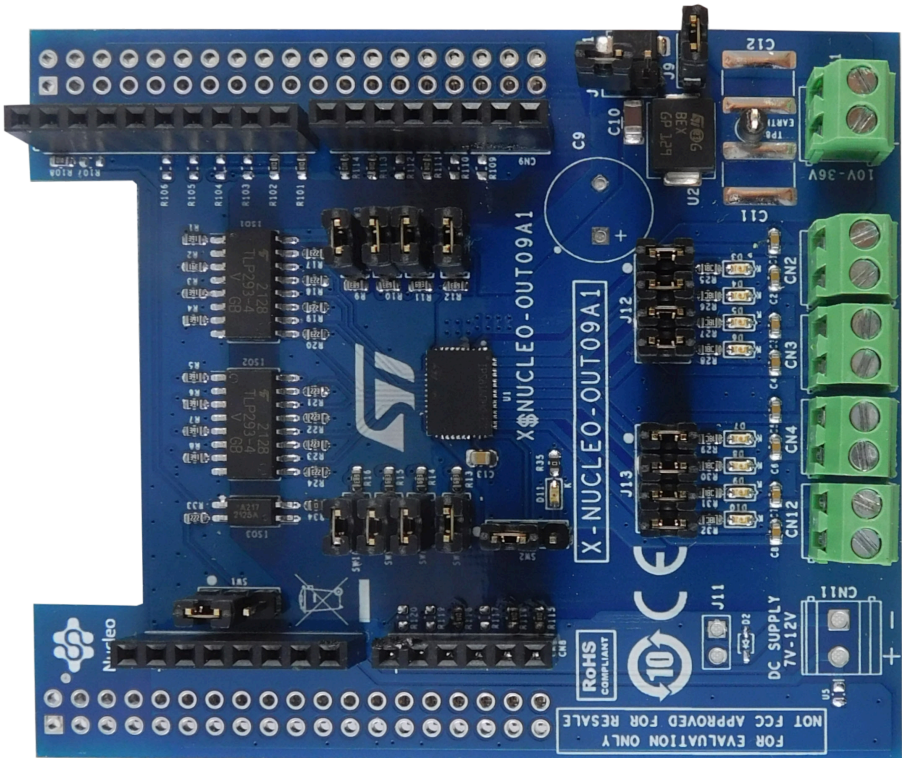
Figure 2. **IPS8160HQ/IPS8160HQ-1 block diagram**



2 IPS8160HQ/IPS8160HQ-1 reference design boards

This is a practical example of how the IPS8160HQ/IPS8160HQ-1 high-side driver (HSD) can be used in applications for an industrial environment.

Figure 3. X-NUCLEO-OUT09A1



2.1 Circuit description

The industrial environment is usually electrically harsh: optocouplers and TRANSIL diodes (TVS) are usually mounted on the application to protect the whole application.

The goal of the TVS is to filter the high-voltage spikes on the 24 V rails coming from the switching of reactive loads and from external electromagnetic events.

The purpose of optocouplers (or digital isolators) is to protect the control system side of the applications from the injected electrical noises on the 24 V rated rails.

Figure 9 and Figure 10 show a complete schematic diagram of the IPS8160HQ/IPS8160HQ-1 reference design boards, named X-NUCLEO-OUT09A1 and X-NUCLEO-OUT19A1 respectively.

X-NUCLEO-OUT09A1 and X-NUCLEO-OUT19A1 use surface-mounted optocouplers that consist of a photo transistor optically coupled to an infrared emitting diode.

The clamping function of TRANSIL diodes protects the device against transient overvoltages. The reference design board is assembled with the SM15T39CA TRANSIL diode.

Refer to Section Appendix A.2 for more information about designing boards to improve EMC immunity and performance in industrial environments.

2.2 Surge suppression

When designing your application, VCC and ground lines should lay on top of each other, minimizing the closed loop area and increasing the ability of the application to reject environmental noise.

Figure 4 shows a surge suppression block using an SM15T39CA TRANSIL diode (TVS).

It provides overvoltage protection for the HSD.

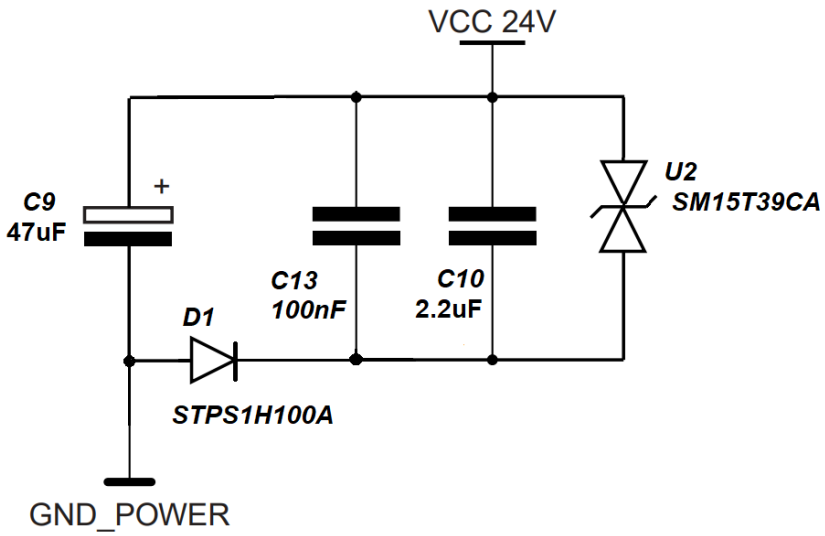
The SM15T39CA has a peak-pulse-power dissipation of 1500 W, standoff voltage of 39 V, and breakdown voltage of 41 V.

A typical protection schematic is composed by a TVS, a couple of MLCC capacitors, and an optional electrolytic capacitor with a reverse polarity protection Schottky.

The TVS acts as a surge suppressor on the supply line and is placed as close as possible to the supply connector of the module. The first 2.2 uF MLCC capacitor is placed parallel to the TVS; the second 100 nF MLCC capacitor must be placed as close as possible to the IPS, and its ESR lower than the ESR of the 2.2 uF allows to reduce any undesired ripple on the supply rail.

An electrolytic capacitor can be placed immediately after the surge suppression block: in this case it is preferable to add a reverse polarity protection Schottky. The size of the electrolytic capacitor is typically 47 uF and it fits most of the applicative conditions. The high ESR of the electrolytic capacitor is already balanced by the two MLCC capacitors.

Figure 4. Surge protection scheme



2.3 Isolation recommendations

Industrial environments require good electrical isolation between digital and power supply parts. Optocouplers are widely used and multichannel optocouplers represent a very attractive solution. Figure 5 shows a schematic diagram with optocouplers connected to ground. Although optocouplers are good isolators, they may lower the category of the Electrical Fast Transients (EFT) immunity tests.

EFT can result in switching shortly on one or more of the optocoupler's channels, and the corresponding output signal is consequently altered.

The phenomenon can be described in this way: the primary and secondary sides of the optocouplers are isolated but they still have parasitic capacitance "bonding" one to each other.

This parasitic capacitance may inject a current through the base emitter junction of the phototransistor when one half of the optocoupler is "tight" due to fast voltage transients with respect to the other side, as shown in Figure 6.

If an optocoupler is used in an emitter-follower configuration, as in most industrial applications, a high emitter voltage signal may be induced by applying EFTs even after opening the collector termination.

An efficient way to prevent this high emitter voltage signal is to provide a conducting plane connected to ground on both the top and bottom layers of the PCB (under the optocouplers) as shown in Figure 30.

Figure 5. **Typical input/status isolation by optocouplers**

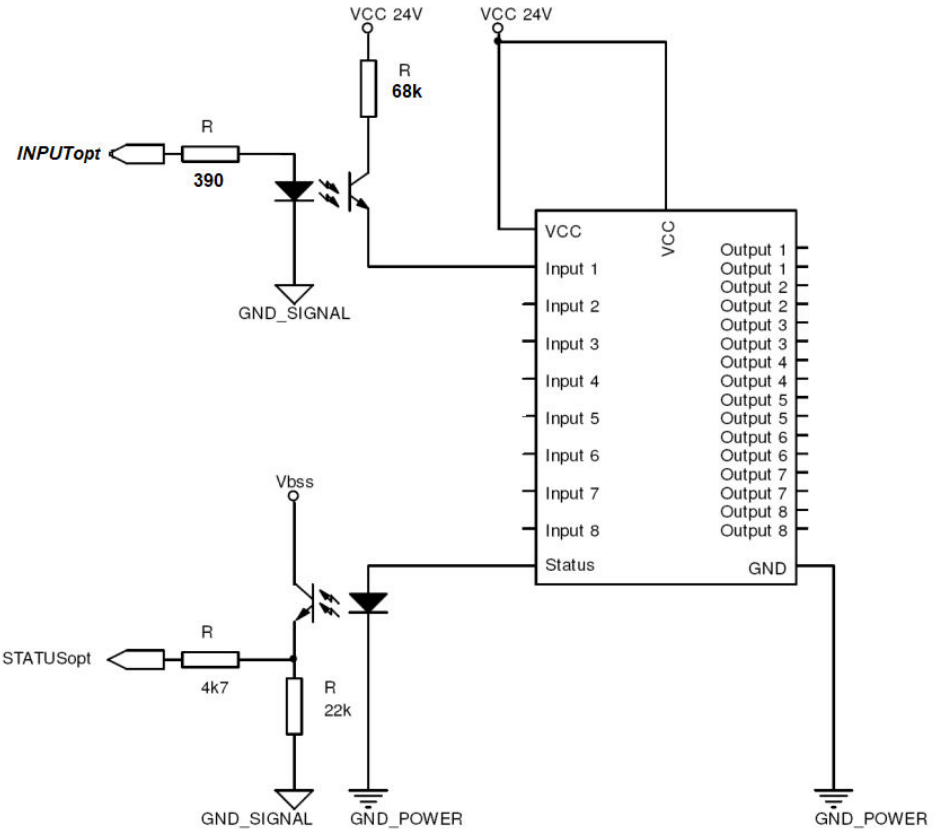
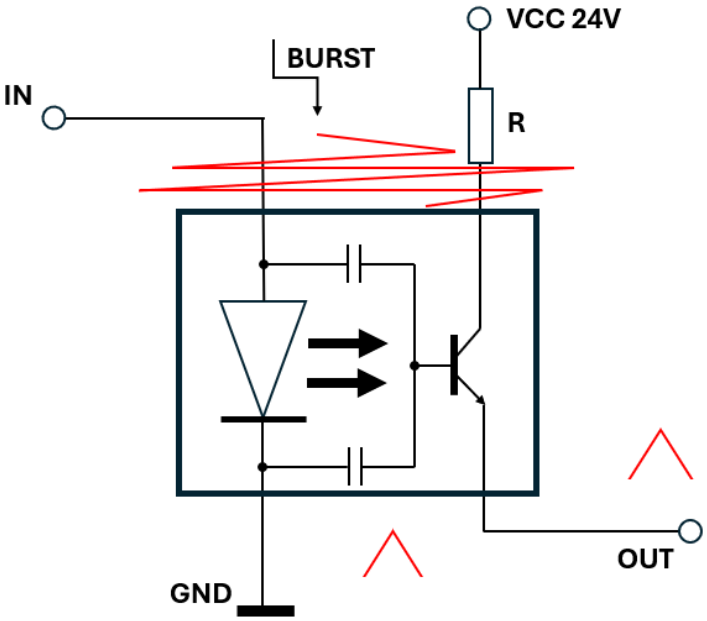


Figure 6. **Burst pulse affecting one input**

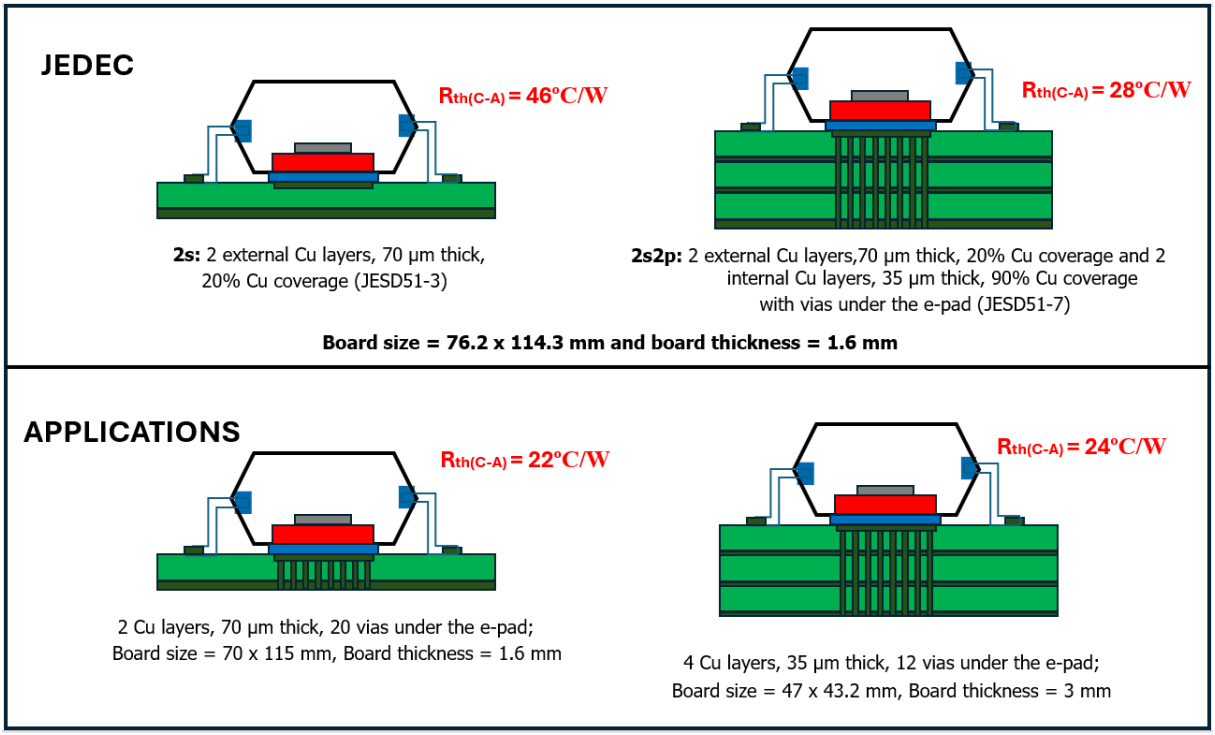


2.4 Heatsink recommendations

Depending on ambient thermal conditions, HSD's with a QFN package require external cooling as the copper bottom plate of the QFN-Package, used to maintain the junction temperature during inductive switching, acts as a thermal capacitor.

The IPS8160HQ/IPS8160HQ-1 reference boards are designed with an onboard heatsink capability (minimum heat sink area is 0.5 cm²). The recommended layout for QFN48L 8x6x0.9 mm packages is shown in Figure 7.

Figure 7. Recommended layout for high power dissipation capability



2.5 Schematic diagrams

Figure 8. Current and voltage conventions

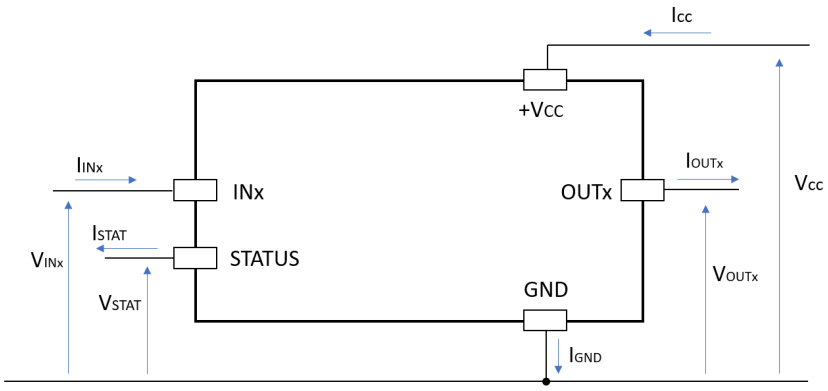


Figure 9. **X-NUCLEO-OUT09A1 and X-NUCLEO-OUT19A1 schematics (1/2)**

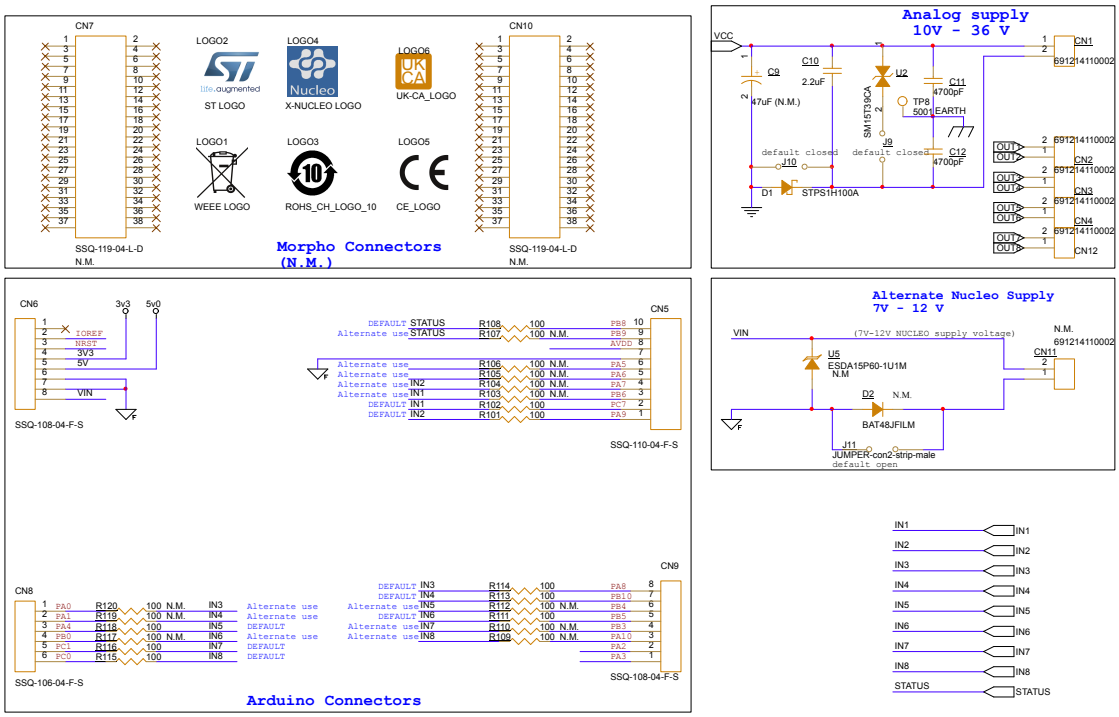
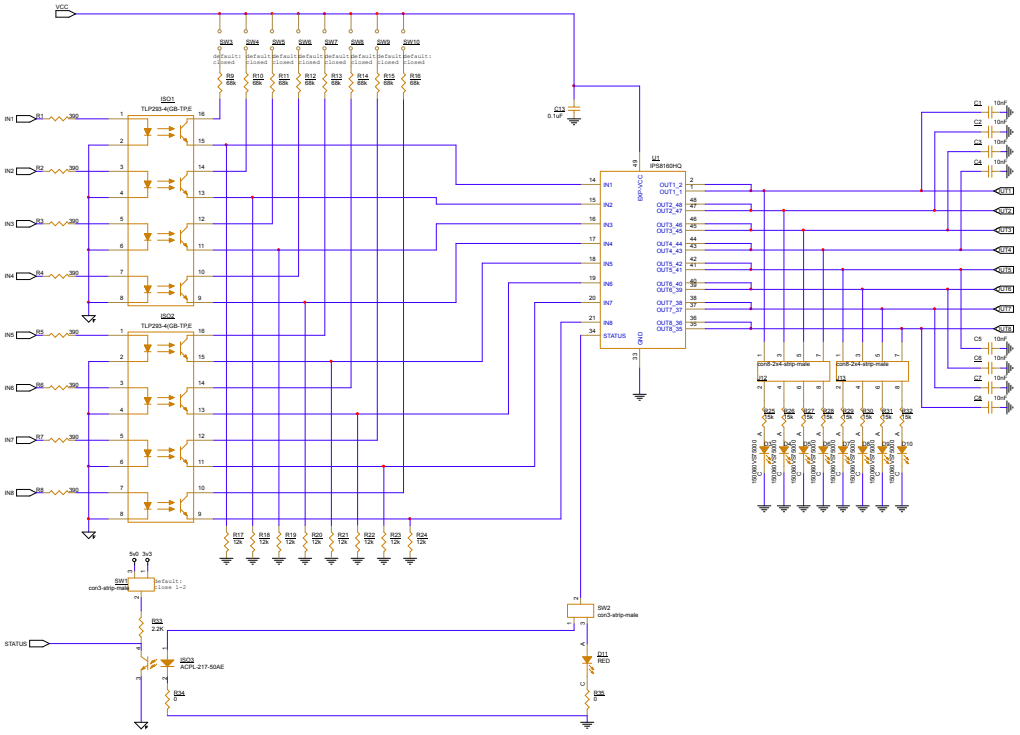


Figure 10. **X-NUCLEO-OUT09A1 and X-NUCLEO-OUT19A1 schematics (2/2)**

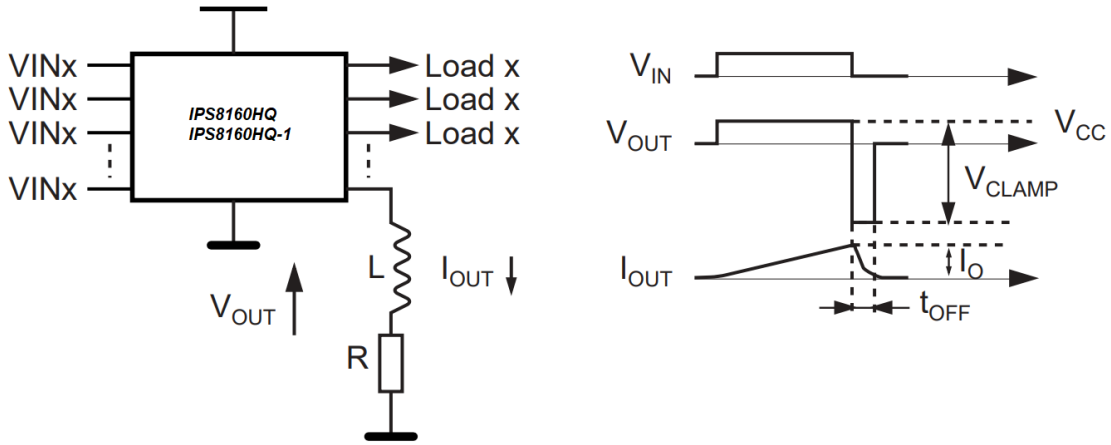


3 Load switching tests

Many different types of loads can be found in an industrial environment. Typical loads have inductive or resistive characteristics. Applications compliant with IEC 60947-5-1 DC13 (48 Ω and 1.15 H) specifications are generally considered as the worst case.

A basic description of typical switching inductor loads is given in Figure 11. In the industrial environment the supply voltage is typically 24 V and it is used to consider a +/-20% variation (19.2 to 28.8 V). The V_{CLAMP} voltage value decides the t_{OFF} demagnetization duration: the faster you want to switch off the circuit, the bigger the $|V_{CLAMP}|$ compared with |VCC| has to be.

Figure 11. Description of the switching inductor loads



Note: Typical V_{CLAMP} value for IPS8160HQ/IPS8160HQ-1 is 50 V.

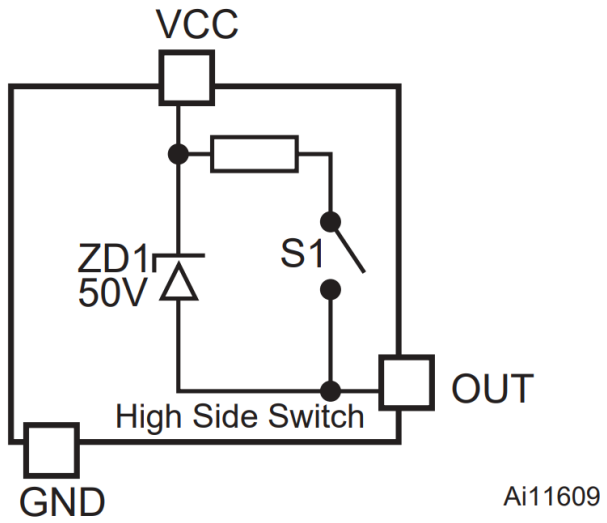
STMicroelectronics' Intelligent Power Switches (IPSs) provide a "fast demagnetization" output structure, an integrated solution for fast switch-off of inductive loads.

Figure 12 shows an equivalent circuit of the fast demagnetization block. In most applications, the output voltage is then clamped at $V_{OUT} = V_{CC} - 50$ V and is therefore dependent on the supply voltage. The integrated clamping structure saves on components and space.

Internal demagnetization can be used only if thermal behavior and load conditions are well known to designers.

Therefore, a detailed analysis of thermal behavior related to inductive load switching is mandatory to prevent improper utilization of the IPSs.

Figure 12. **IPS simplified structure**



The parameters are given by the following formulas:

$$t_{OFF} = \frac{L}{R_{LOAD}} \times ln\left(1 + \frac{V_{CC}}{V_{CLAMP} - V_{CC}}\right) \quad (1)$$

$$E_{OFF} = \frac{V_{CLAMP}}{R_{LOAD}} \times \left\{\frac{L \times V_{CC}}{R_{LOAD}} - [(V_{CLAMP} - V_{CC}) \times t_{OFF}]\right\}$$

$$P_{t_{OFF}} = \frac{E_{OFF}}{t_{OFF}}$$

Example, for IPS8160HQ and IPS8160HQ-1:

for I_{OUT} = 0.5 A, L = 1.15 H, f = 0.5 Hz, VCC = 24 V, and V_{CLAMP} = 50 V

V_{CLAMP} - VCC = 26 V and R_{LOAD} = 48 Ω

t_{OFF} = 15.7 ms

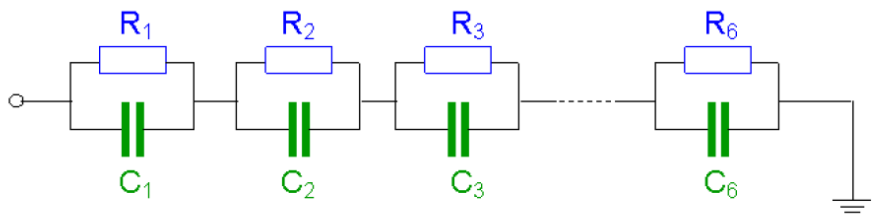
E_{OFF} = 175 mJ per channel

Pt_{OFF} = 8 x (175 / 15.7) = 89 W

4 Thermal stress tests

The thermal model of a generic Intelligent Power Switch (IPS) can be exemplified as shown in Figure 13.
In the same figure the thermal parameter values for the IPS8160HQ/IPS8160HQ-1 mounted on a 2s2p Jedec board are also indicated.

Figure 13. RC ladder on IPS8160HQ thermal impedance / 2s2p Jedec board



R (°C/W)	R1	R2	R3	R4	R5	R6
	1.000E-03	1.152	3.439	5.08	7.25	10.849
C (Ws/°C)	C1	C2	C3	C4	C5	C6
	4.446E-01	4.07E-03	1.85E-02	1.68E-01	4.94E-01	7.73
τ (s)	4.4464E-04	4.69E-03	6.345E-02	0.85496	3.58368	83.8628

The aim of the designer is to provide the lowest possible junction-ambient thermal impedance, in order to minimize the chip temperature jump-up.

Example IPS8160HQ:

I = 0.5 A, L = 1.15 H, f = 0.5 Hz, T_A = 60 °C, Duty Cycle (DC) = 50%, VCC = 24 V, 8 channels active at the same time.

Conduction losses:

Losses due to I_{SON} (supply current): VCC * I_{SON} (max) * DC = 24 * 0.012 * 0.5 = 144 mW

PowerMOS losses at ON-state: R_{ON} (max) * I^2 * DC * 8 = 0,28 * (0.5)^2 * 0.5 * 8 = 280 mW

Switching losses:

Switching losses are due to inductance discharge: P_{DOFF} = 8 * E_{OFF} * f = 8 * 0.175 * 0.5 = 700 mW

Total losses and junction temperature:

Total power losses = 1.12 W

Considering a 2s2p JESD51-7 board, for the QFN48L 8x6x0.9 mm results:

R_{thJA} = 28.3 °C/W and T_J = T_A + P_D * R_{thJA} = 60 + 1.12 * 28.3 = 91.7 °C.

Note: According to the JESD51-7 standard, a 2s2p board has: 2 external Cu layers, 70 µm thick, 20% Cu coverage and 2 internal Cu layers, 35 µm thick, 90% Cu coverage with vias under the e-pad.

5 Electromagnetic compatibility (EMC) tests

The IPS8160HQ and IPS8160HQ-1 reference design boards pass the following industrial tests.

Table 1. EMC industrial compliance

IEC specification	Description
61000-4-2	Electrostatic Discharge (ESD)
61000-4-4	Electric Fast Transients (EFT)
61000-4-5	Surge protection
61000-4-6	Immunity to conducted disturbances

Table 2. Abbreviations

Abbreviations	Description
CC	Current Clamp(EFT)
CCC	Capacitive Coupling Clamp
CDN	Coupling/Decoupling Network
DN	Electric Fast Transients
EFT	Generator with CDN according to IEC 61000-4-4
ESD	Electrostatic Discharge
EUT	Equipment Under Test
HSD	High-Side Driver
IPS	Intelligent Power Switch
PE	Protected Earth (metal plane)
Signal Generator	Wave generator with power amplifier according to IEC 61000-4-6
Surge Generator	Generator with CDN according to IEC 61000-4-5

Performance criteria for immunity tests

- Performance criteria A – ‘Performance within specification limits’
- Performance criteria B – ‘Temporary degradation which is self-recoverable’
- Performance criteria C – ‘Temporary degradation which requires operator intervention’
- Performance criteria D – ‘Loss of function which is not recoverable’

5.1 Requested test levels

IEC 61000-4-2

- Polarity: positive/negative
- Test voltage:
  - Contact: level 2 (4 kV)
  - Air: level 3 (8 kV)
- Stress sequence: 10 positive / 10 negative
- Rate discharge = 1 Hz
- Outputs: always OFF and floating

IEC 61000-4-4

- Polarity: positive/negative
- Test voltage: level 4 (4 kV)
- Burst duration: 15 ms±20% at 5 or 100 kHz
- Burst period: 300 ms±20%
- Duration time: 60 seconds (min.)
- Applied to: input/output ports and supply lines

IEC 61000-4-5

- Polarity: positive/negative
- Test voltage: level 3 (2 kV)
- Number of discharges: 5
- Repetition rate: 1 per min.
- Applied to: output ports and supply lines (all combinations)

IEC 61000-4-6

- Test voltage: level 3 (10 V)
- Frequency range: 150 kHz to 80 MHz
- Modulation: 80% depth by AM 1 kHz
- Frequency step: 1%
- Dwell time 100 ms
- Applied to: input/output ports and supply lines

5.2 IEC 61000-4-2 ESD test description

The test is intended to demonstrate the immunity of equipment subjected to static electricity discharges from operators directly and to adjacent objects.

The table-top equipment under test is placed on a wooden table, 0.8 m high, standing on the ground reference plane. A horizontal coupling plane (HCP) is placed on the table.

The EUT and the cables are isolated from the coupling plane by an insulating support, 0.5 mm thick. The floor-standing equipment is isolated from the ground reference plane by an insulating support about 0.1 m thick.

The vertical coupling plane (VCP) of dimensions 0.5 m x 0.5 m is placed parallel to, and positioned at a distance of 0.1 m from, the EUT.

Air discharges are applied to non-metallic parts of the system. Contact discharges are applied to all accessible metallic parts. Discharges are also applied to the horizontal and vertical coupling planes.

Types of discharges:

- In contact: the conductive surface (head pointed gun)
- In air: on insulating surfaces (gun head rounded)

5.2.1 ESD tests setup

Figure 14 illustrates the ESD test setup while Figure 15 a typical calibration waveform.

- Positive and negative discharges;
- 10 discharges, one per second;
- The discharge return cable of the ESD generator is connected to the ground reference plane. The total length of this cable is 2 m.

Figure 14. **ESD test setup**

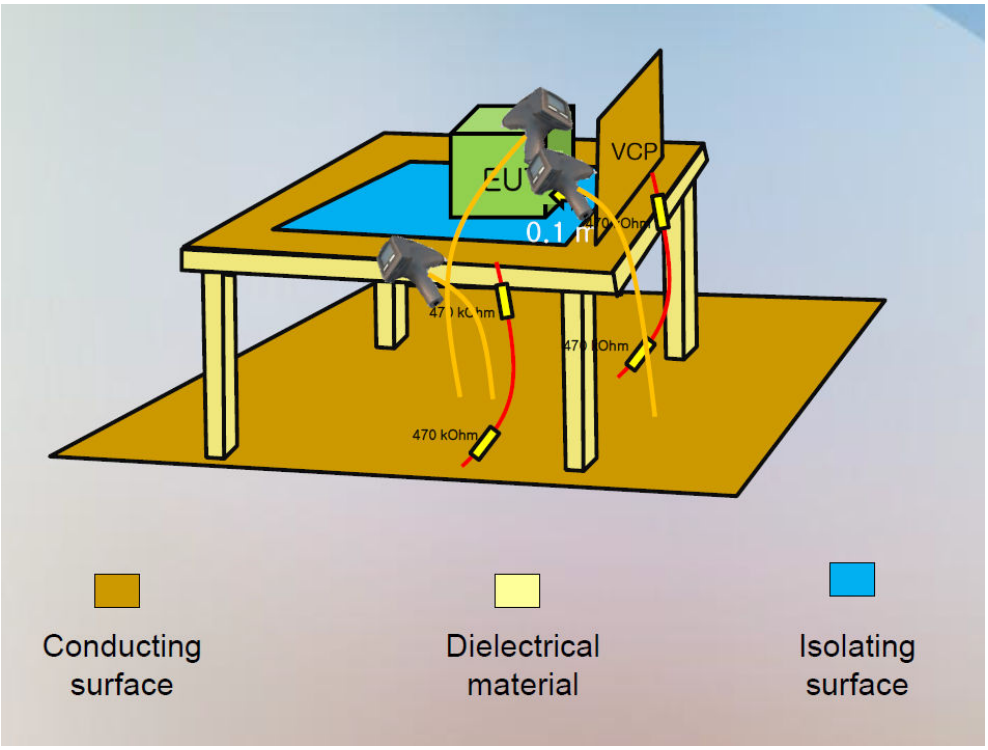
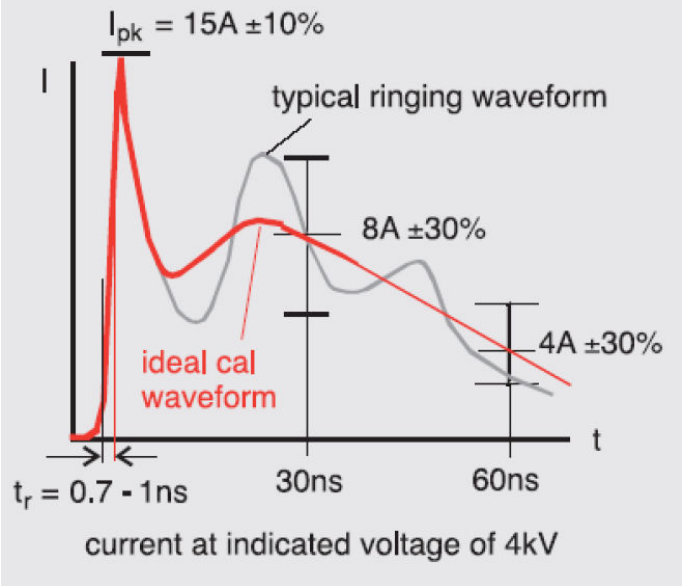


Figure 15. **ESD calibration waveform**



5.3 IEC 61000-4-4 EFT test setup

The reference design boards are tested on input/output ports and power supply lines.

The test voltage is applied from the EFT generator to the EUT via a capacitive coupling clamp.

The test setup and test voltage waveform comply with IEC 61000-4-4 specifications.

The capacitive coupling clamp is connected by a high-voltage coaxial cable to the generator as close as possible to the EUT.

5.3.1 Power supply tests

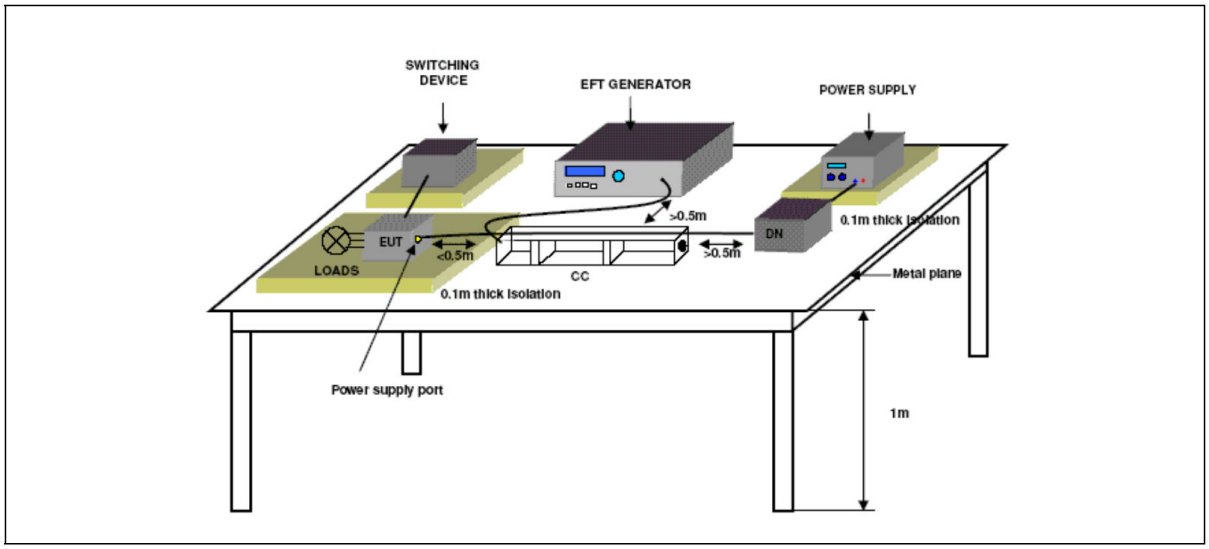
Figure 16 illustrates the power supply test setup. A capacitive coupling clamp applies the test voltage (max. 4 kV) to the power supply lines. A decoupling network (DN) protects the power supply against the test voltage.

EUT test conditions:

Input port ON/OFF and f_{OPER} = 1 Hz

Input port wave form: Square 0/5 V; f = 1 Hz

Figure 16. Power supply tests (IEC 61000-4-4)



5.3.2 Input port tests

Figure 17 illustrates the input port test setup. The RDB input ports are tested by first switching them to ground and then to the 5 V supply using the battery-powered switch shown in Figure 18 to increase protection. The maximum test voltage must not exceed 4 kV.

Figure 17. Test on input ports (IEC 61000-4-4)

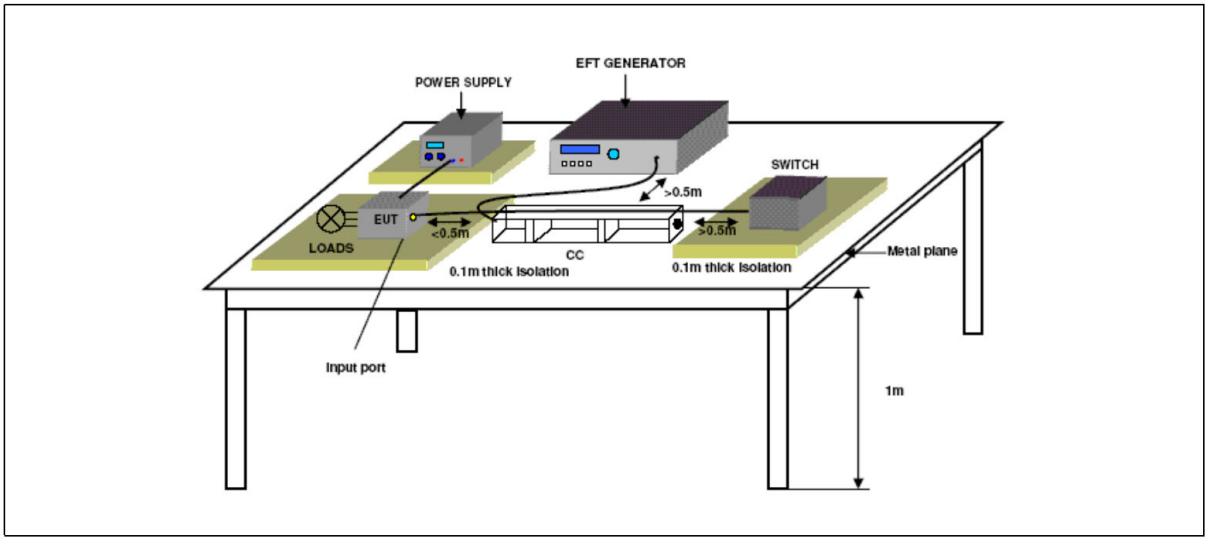
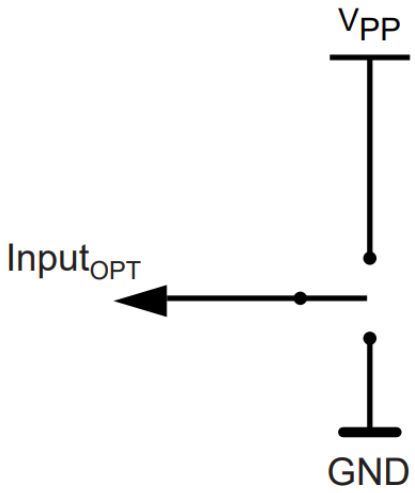


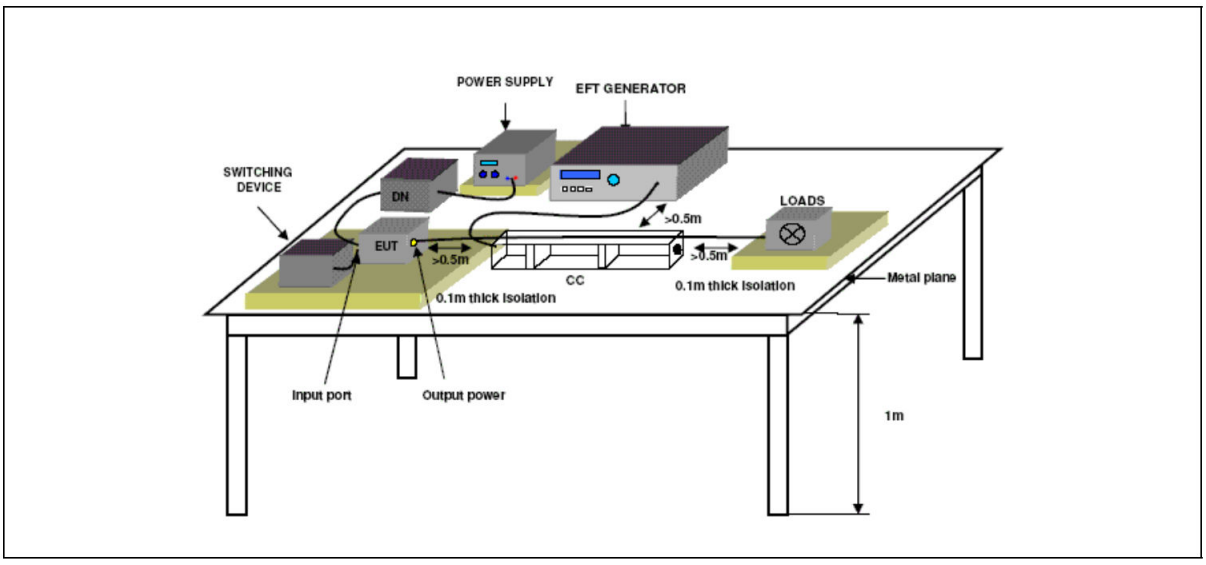
Figure 18. **Switch diagram**



5.3.3 Output port tests

Figure 19 illustrates the output port test setup. The capacitive coupling clamp is the recommended method for coupling the generator source voltage into the output ports. All auxiliary devices are placed on the wood isolation board (0.1-meter thick). The test is performed while the HSD output port is switched On/Off at 1 Hz. The maximum test voltage must not exceed 4 kV.

Figure 19. **Output port tests (IEC 61000-4-4)**



5.4 IEC 61000-4-5 surge test setup

Section 5 of the IEC 61000-4 specification concerns the immunity requirements, test methods, and range of recommended test levels for equipment to unidirectional surges caused by overvoltages from switching and lightning transients. The reference design boards are tested on the power supply lines and output port.

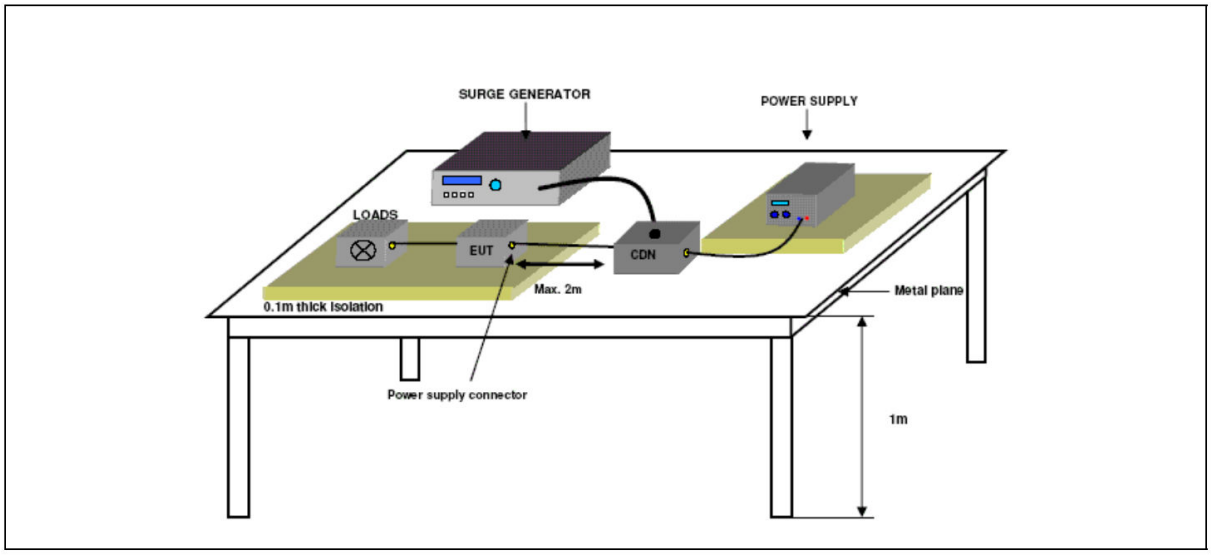
5.4.1 Power supply tests

Figure 20 illustrates the power supply test setup. The reference design boards are tested with different coupling modes:

- Line-to-line coupling mode with source impedance 42 Ω (meaning VCC 24 V and GND_Power on the board, both polarities)
- Line-to-PE coupling mode with source impedance 42 Ω (meaning VCC 24 V/GND_Power to GND_earth on the board, both polarities)
- Output to GND_Power with source impedance 2 Ω (requested test level: level 1 (+/- 500 V))
- Output to VCC 24 V with source impedance 2 Ω (requested test level: level 1 (+/- 500 V))
- Output to Protect Earth with source impedance 42 Ω.

The maximum surge voltage may not exceed 2 kV for line-to-line coupling mode and 2 kV for line-to-PE coupling mode. The test is performed while the HSD output port is switched On/Off at 1 Hz. The maximum length of the cables between the EUT and CDN is 2 meters.

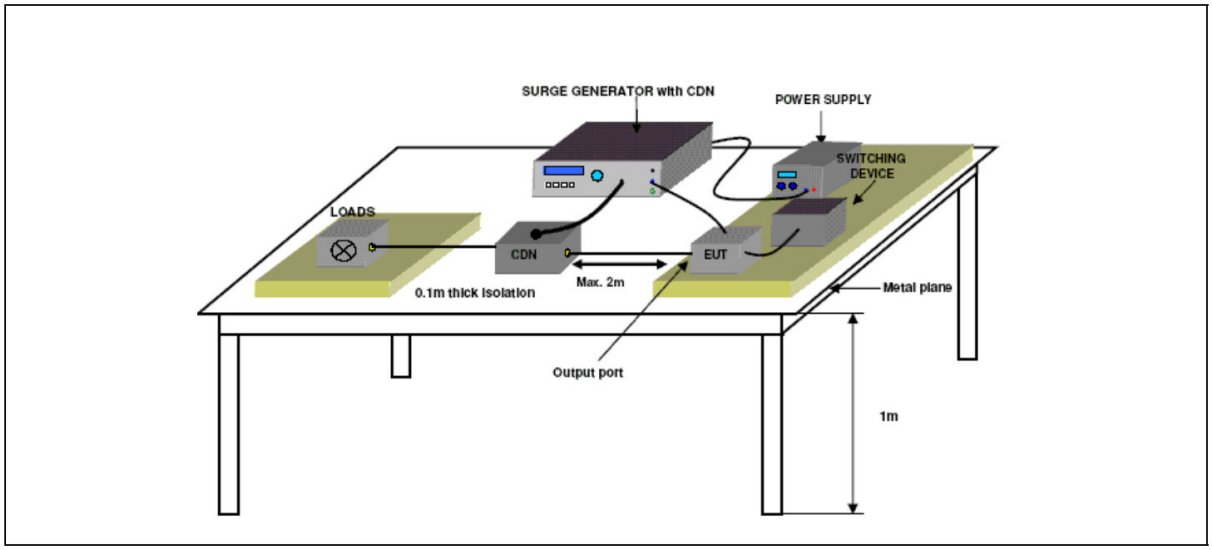
Figure 20. Power supply tests (IEC 61000-4-5)



5.4.2 Output port tests

Figure 21 illustrates the output port test setup. The maximum surge voltage and coupling mode are the same as with the power supply tests. The test is performed while the HSD output port is switched On/Off with both polarities. The output lines are tested between VCC/GND and PE.

Figure 21. Test on output ports (IEC 61000-4-5)



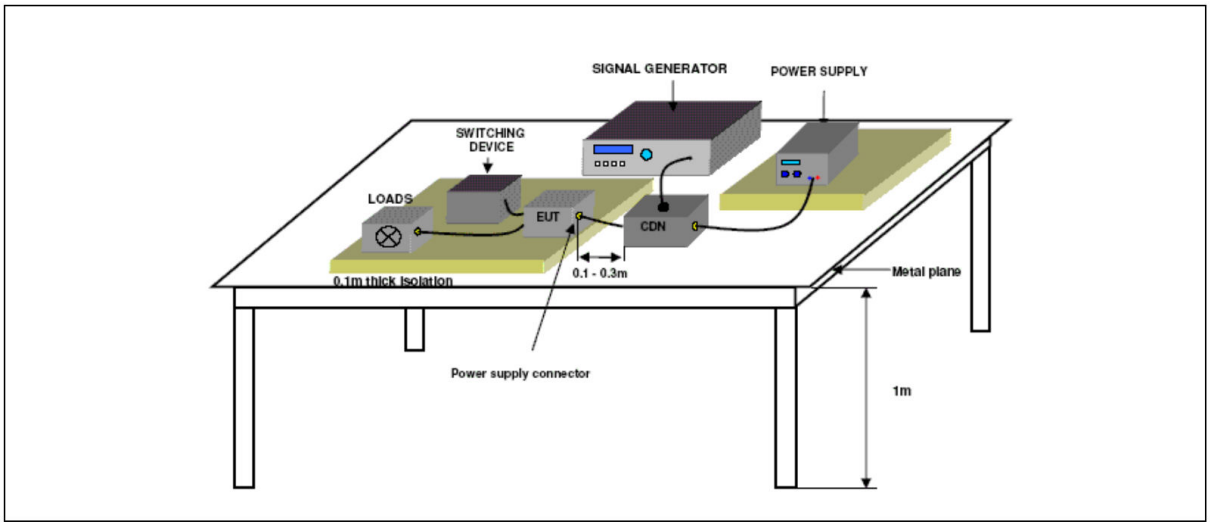
5.5 IEC 61000-4-6 conducted immunity

The reference design boards are tested on the input/output ports and power supply lines with a maximum voltage of 10 VRMS. The test signal is basically a sinusoidal waveform, whose frequency sweeps from 150 kHz up to 80 MHz with an 80% amplitude modulation at 1 kHz of the same signal. The EUT clearance from all metallic objects must be at least 0.5 meters.

5.5.1 Power supply tests

Figure 22 illustrates the power supply test setup. The test voltage is applied by coupling the decoupling networks CDN. The maximum voltage is 10 VRMS. The maximum distance between EUT and CDN is 0.3 meters. All Auxiliary Units (AU) such as power supply switching devices must be placed on the wood isolation.

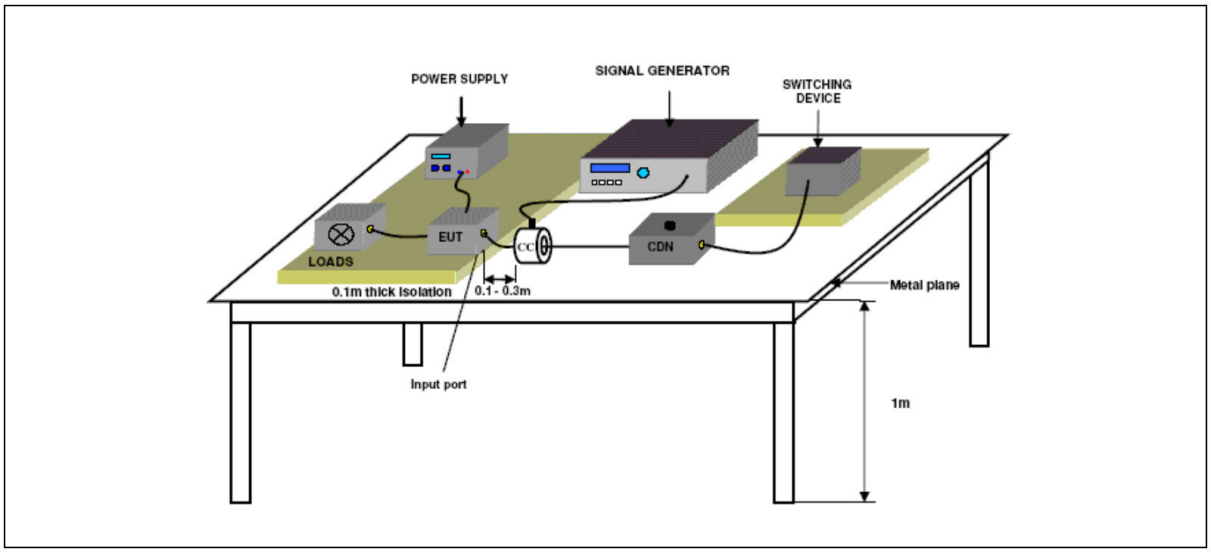
Figure 22. Power supply tests (IEC 61000-4-6)



5.5.2 Input port tests

Figure 23 illustrates the input port test setup. The test voltage from the signal generator to the EUT is applied by the current clamp. This device establishes inductive coupling to the cable connected to the EUT. The maximum distance between the EUT and the CC is 0.3 meters. The test is performed while the HSD input port is switched on/off at 1 Hz.

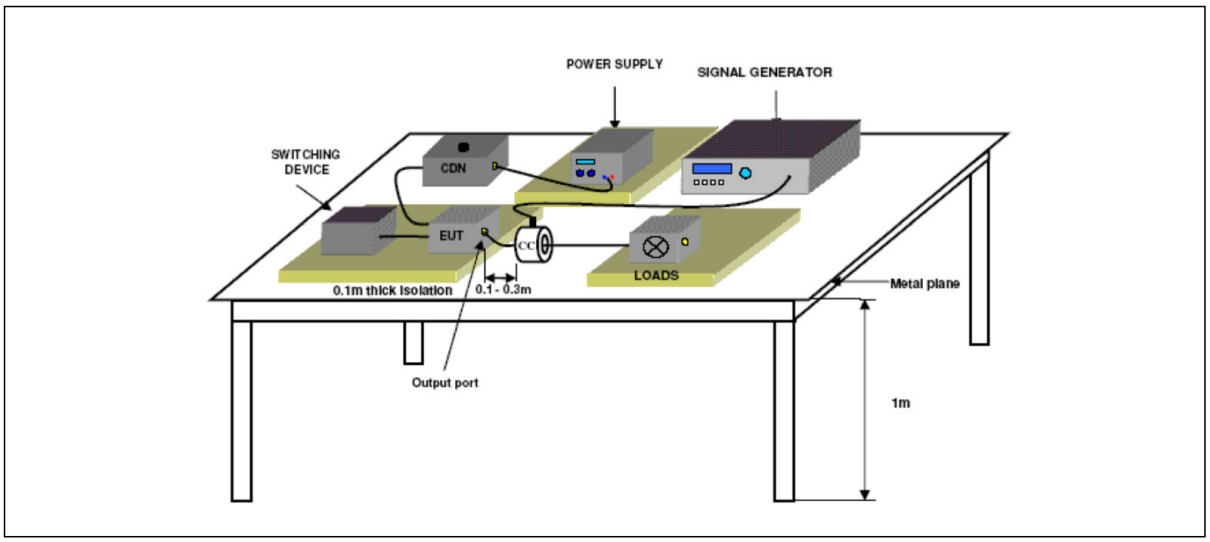
Figure 23. Input port tests (IEC 61000-4-6)



5.5.3 Output port tests

Figure 24 illustrates the output port test setup. The power supply must be protected from the disturbance signal by a decoupling network. The current clamp is used as the coupling device for the signal generator. The test is performed while the HSD output port is switched on/off at 1 Hz.

Figure 24. Output port tests (IEC 61000-4-6)



6 EMC test results

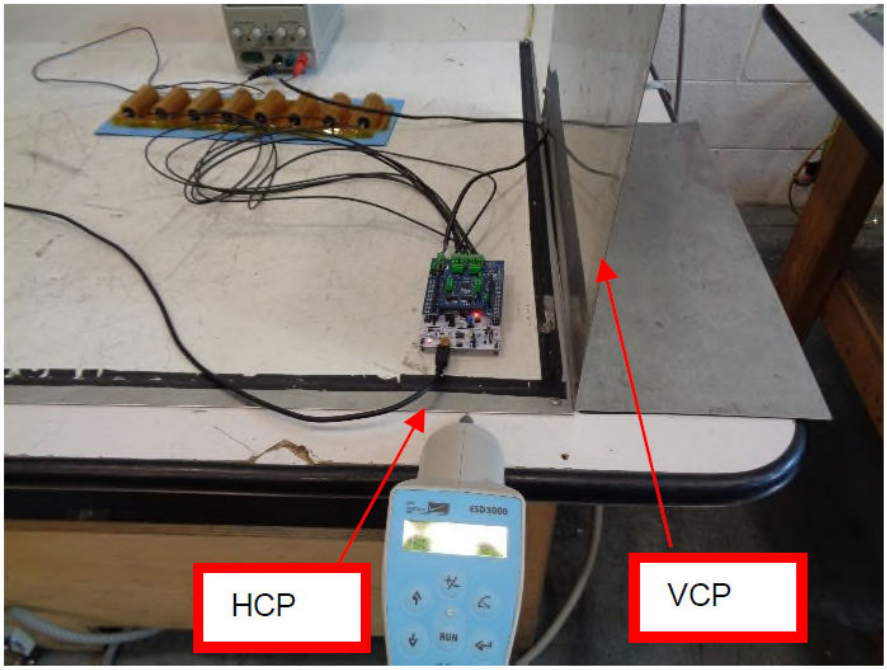
6.1 IEC 61000-4-2 ESD test

The IPS8160HQ/IPS8160HQ-1 reference design boards are tested according to IEC 61000-4-2 for ±4 kV level (contact) and for ±8 kV level (air).

These tests have been conducted by third parties.

Test result: The X-NUCLEO-OUT09A1 and X-NUCLEO-OUT19A1 worked properly during and after the tests up to ±4 kV (criteria “A”) and ±8 kV (criteria “A”); test **passed**.

Figure 25. Photo documentation of the test setup



Note: Horizontal coupling plane (HCP) - Vertical coupling plane (VCP)

C = Contact discharge / A = Air discharge

6.2 IEC 61000-4-4 EFT test

The IPS8160HQ/IPS8160HQ-1 reference design boards are tested according to IEC 61000-4-4 for ±4 kV level.

Test result: The X-NUCLEO-OUT09A1 and X-NUCLEO-OUT19A1 worked properly during the test up to ±4.4 kV (criteria “A”); test **passed**.

6.3 IEC 61000-4-5 surge test

The IPS8160HQ/IPS8160HQ-1 reference design boards are tested according to IEC 61000-4-5 for ±2 kV level.

The following figures (R_{GND} = 27 Ω) show the application diagram in case of surge to OUTx and surge to VCC with related signal scope acquisitions.

Figure 26. **Surge to OUT - application diagram**

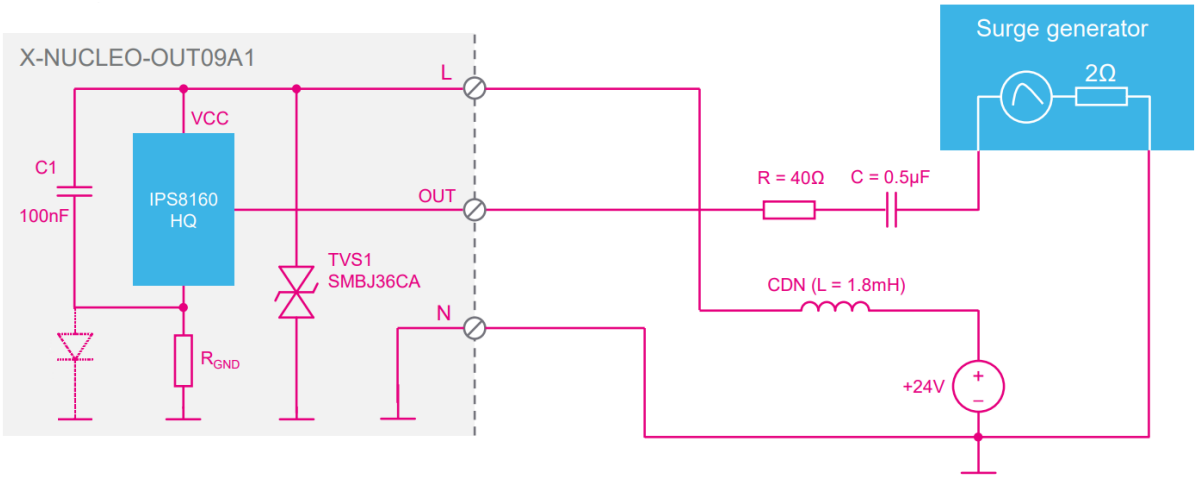


Figure 27. **Surge to OUT - scope acquisitions example**

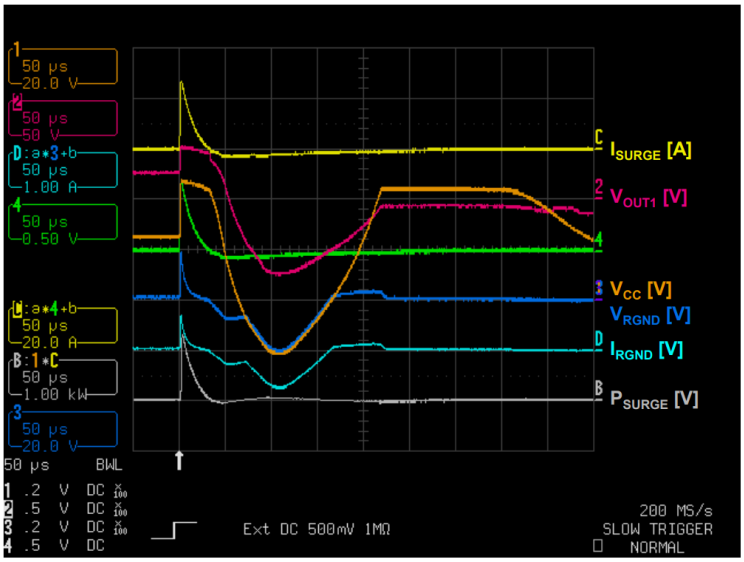


Figure 28. **Surge to VCC - application diagram**

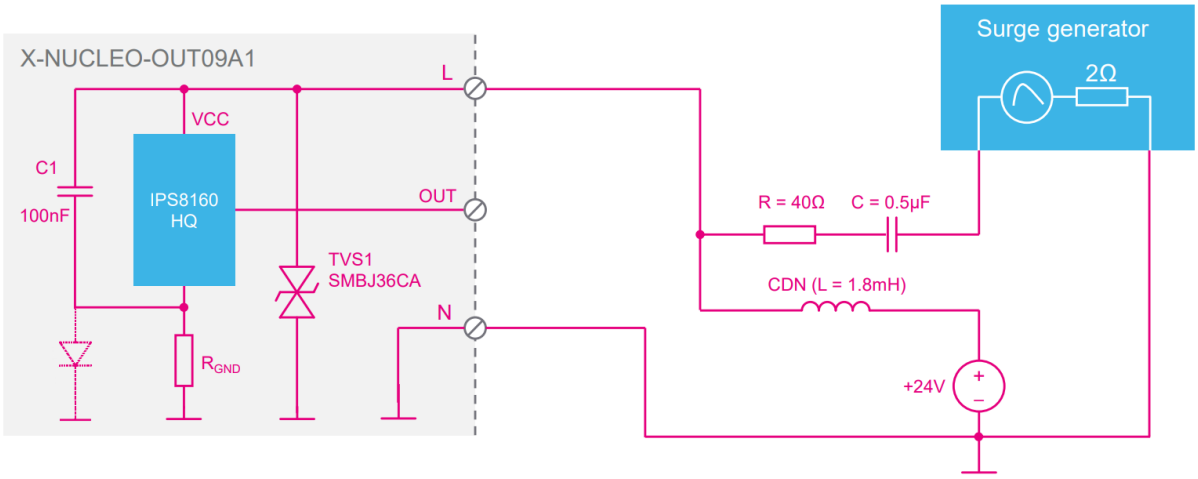
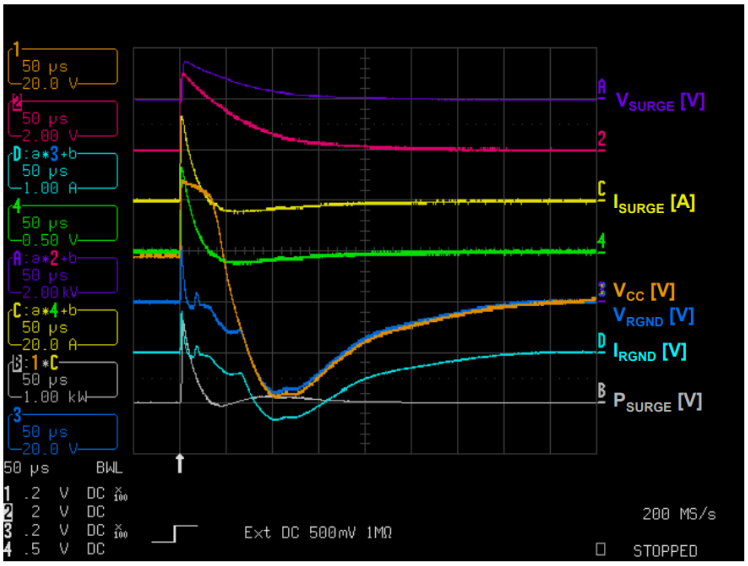


Figure 29. **Surge to VCC - scope acquisitions example**



Test results:

- ±2.8 kV (criteria “A”)

Test **passed**.

6.4 IEC 61000-4-6 conducted immunity tests

These tests have been conducted by third parties.

In particular, compliance has been verified with:

EN IEC 61000-6-1:2019

Electromagnetic compatibility (EMC) Part 6-1: Generic standards - Immunity standard for residential, commercial, and light industrial environments.

EN IEC 61000-6-3:2021

Electromagnetic compatibility (EMC) - Part 6-3: Generic standards - Emission standard for equipment in residential environments.

Tests **passed**.

6.5 EMC tests summary

Table 3 summarizes the EMC test results obtained and the corresponding requested levels.

Table 3. **EMC tests summary**

Test	Requested level	Checked level
61000-4-2 (ESD Contact)	± 4 kV	± 4 kV
61000-4-2 (ESD Air)	± 8 kV	± 8 kV
61000-4-4 (EFT)	± 4 kV	± 4.4 kV
61000-4-5 (Surge)	± 2 kV	± 2.8 kV
61000-4-6 (Conducted immunity)	10 V	10 V

Appendix A IPS8160HQ and IPS8160HQ-1 reference design boards (RDB)

A.1 X-NUCLEO-OUT09A1 and X-NUCLEO-OUT19A1 bill of materials

The list of parts for the IPS8160HQ (IPS8160HQ-1) reference design board is provided in the following table

Table 4. X-NUCLEO-OUT09A1 and X-NUCLEO-OUT19A1 BOM

Item	Quantity	Reference	Value
1	8	C1 C2 C3 C4 C5 C6 C7 C8	10nF
2	0	C9	47uF (N.M.)
3	1	C10	2.2uF
4	0	C11 C12	4700pF
5	1	C13	0.1uF
6	5	CN1 CN2 CN3 CN4 CN12	691214110002
7	1	CN5	10 ways, 1 row
8	2	CN6 CN9	8 ways, 1row
9	0	CN7 CN10	
10	1	CN8	6 ways, 1 row
11	0	CN11	691214110002
12	1	D1	STPS1H100
13	0	D2	BAT48JFILM
14	8	D3 D4 D5 D6 D7 D8 D9 D10	150060VS75000
15	1	D11	RED
16	2	ISO1 ISO2	TLP293-4 TLP293-4
17	1	ISO3	ACPL-217-50AE
18	10	J9 J10 SW3 SW4 SW5 SW6 SW7 SW8 SW9 SW10	JUMPER-con2-strip-male
19	0	J11	JUMPER-con2-strip-male
20	2	J12 J13	con8-2x4-strip-male
21	8	R1 R2 R3 R4 R5 R6 R7 R8	390
22	8	R9 R10 R11 R12 R13 R14 R15 R16	68k
23	8	R17 R18 R19 R20 R21 R22 R23 R24	12k
24	8	R25 R26 R27 R28 R29 R30 R31 R32	15k
25	1	R33	2.2K
26	2	R34 R35	0
27	9	R101 R102 R108 R111 R113 R114 R115 R116 R118	100
28	0	R103 R104 R105 R106 R107 R109 R110 R112 R117 R119 R120	100
29	2	SW1 SW2	con3-strip-male
30	1	TP8	5001

Item	Quantity	Reference	Value
31	1	U2	SM15T39CA
32	0	U5	ESDA15P60-1U1M
33	1	U1 (U1)	IPS8160HQ (IPS8160HQ-1)

A.2 Recommended X-NUCLEO-OUT09A1 and X-NUCLEO-OUT19A1 layout

The PCB layout is very important in order to operate the devices in the worst condition and under EMC immunity.

Figure 30. X-NUCLEO-OUT09A1 PCB layout (top and bottom)

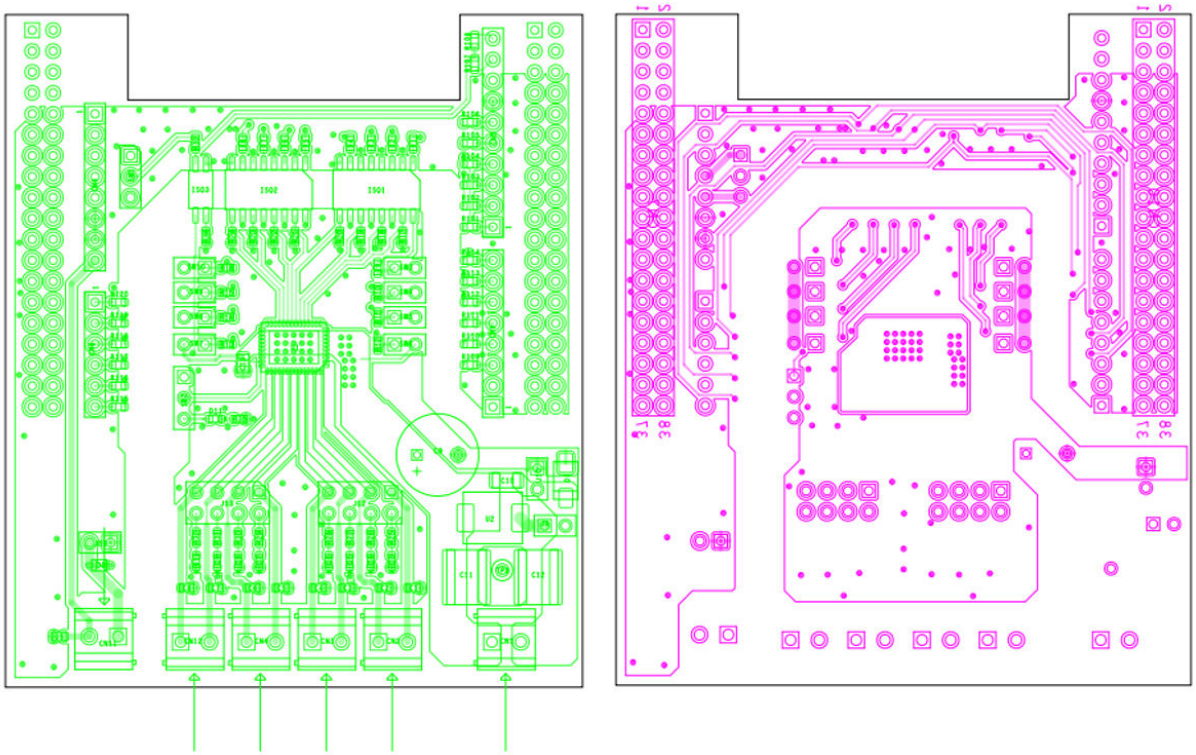
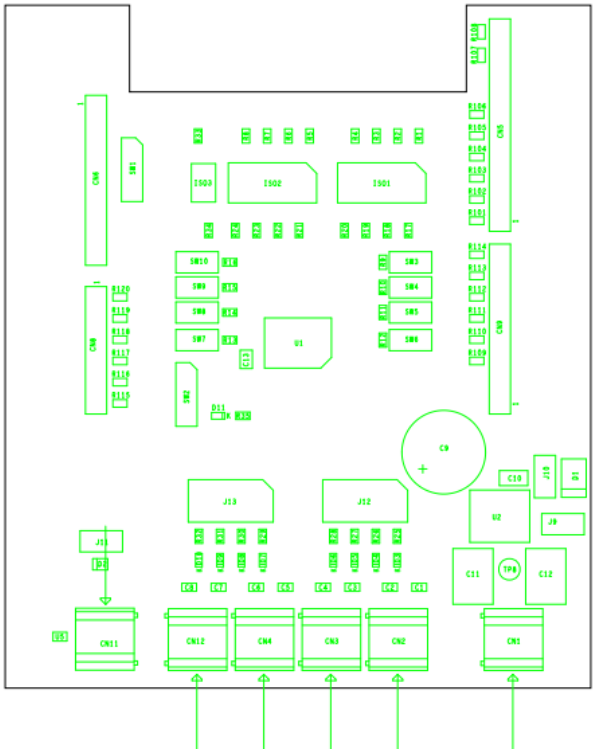


Figure 31. **X-NUCLEO-OUT09A1 PCB layout (component side)**



Revision history

Table 5. **Document revision history**

Date	Version	Changes
08-Aug-2024	1	Initial release.
15-Oct-2024	2	Corrected typo in Section 3; corrected some typos in Section 4; changed Figure 26 and Figure 28; some minor changes.

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