Antenna design for ST25R500 and ST25R300 devices

Introduction

This application note is a design guide for magnetic loop antennas connected directly to the ST25R500. Beyond the antenna design, it describes the antenna parameters measurement and matching, as well as the design verification.

The examples in this document are based on the ST25R500 and ST25R300 devices, but the techniques and tools can be used (when applicable) for other products of the same family.

This document is intended to be used with the ST25R antenna matching tool software (STSW-ST25R004), which supports the calculation of the matching components and reduces the tuning iteration effort to a minimum. Along with the tool an open-source simulator is provided for basic system validation via simulation.

The following documents are considered as reference:

- ST25R500 datasheet (DS14593)
- ISO/IEC 14443 and ISO/IEC 10373-6:2011, from www.iso.org

1 List of acronyms and notational conventions

1.1 Acronyms

Table 1. List of acronyms

RFO1,2	Antenna driver output pins
RFI1,2	Receiver input pins
Tx	Transmit signal (from RFO to antenna)
Rx	Receive signal (from antenna to RFI)
$L_{EMC1,2}$	Inductor of the EMC filter
$C_{EMC1,2}$	Capacitor of the EMC filter
$C_{S1,2}$	Series capacitor of the matching network
C_P	Parallel capacitor of the matching network
R_Q	Parallel resistor used for the Q factor adjustment (calculated)
L_{ANT}	Antenna inductance (measured)
C_{ANT}	Parasitic antenna parallel capacitance (calculated)
R_{PANT}	Total antenna parallel resistance (calculated)
f_{work}	NFC operating frequency (13.56 MHz)
f_{res}	Antenna self-resonance frequency (measured)
R_{SDC}	Antenna series resistance (measured)
$R_{P@fres}$	Antenna parallel resistance at self-resonance (measured)
K	Skin effect correction factor (calculated)
$R_{P@work}$	Antenna parallel resistance at operating frequency (calculated)
R_{PDC}	Antenna parallel resistance converted from measured series resistance (calculated)
R_T	Parallel resistance for target Q factor (calculated)
Q	Antenna Q factor (calculated)

1.2 Representation of numbers

The following conventions and notations apply in this document unless otherwise stated:

- **Binary numbers** are represented by strings of 0 and 1 digits, shown with the most significant bit (MSB) on the left, the least significant bit (LSB) on the right, and “0b” added at the beginning. Example: 0b11110101.
- **Hexadecimal numbers** are represented by using numbers 0 to 9 and characters A to F, and adding “0x” at the beginning. The most significant byte (MSB) is shown on the left and the least significant byte (LSB) on the right. Example: 0xF5.
- **Decimal numbers** are represented without any trailing character. Example: 245.

2 Hardware and software requirements

To use the ST25R antenna matching tool, perform antenna measurements and verify the design, the following hardware and software resources are required:

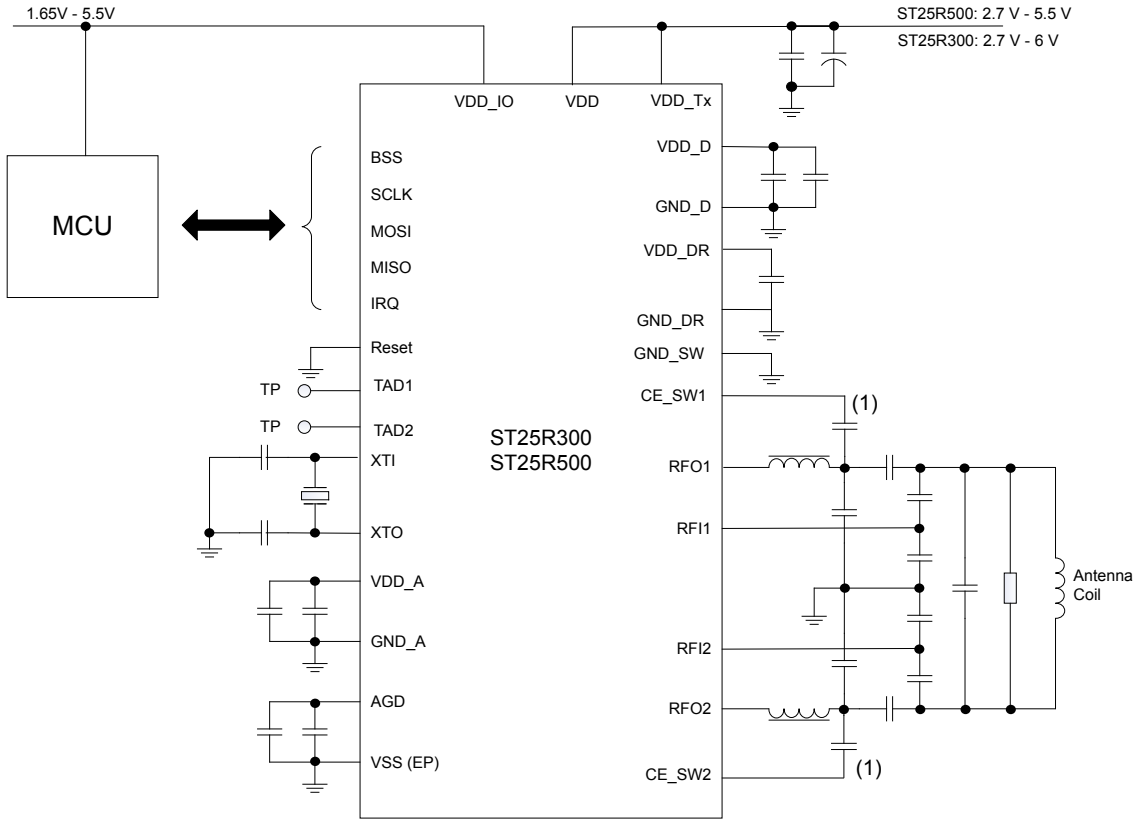
- Network analyzer
- Oscilloscope (capable of pulse triggering)
- SMA cable
- ISO 10373-6 calibration coil 1
- Software/Firmware to control the ST25R500 (for example, ST25R500 STEVAL demo)
- Windows® OS
- ST25R antenna matching tool (STSW-ST25R004)

3 Antenna interface stage

Figure 1 shows the minimum configuration for driving an antenna through a differential matching network, and Figure 2 the antenna circuit schematic.

From the ST25R500 antenna driver output pins RFO1 and RFO2, the Tx signal goes through the EMC filter into the matching network and to the antenna. The Rx signal coming from the antenna is led through the capacitive voltage divider back into the ST25R500 receiver input pins RFI1 and RFI2. The antenna interface stage can be set up as single ended or as differential topology, this document focuses on the latter configuration.

Figure 1. Antenna interface stage (differential matching network)



(1) Capacitors connected to the GPIO pin should only be populated if card emulation operation is required. Due to parasitic inductance (bond wire, PCB traces) the capacitor can build a series resonating structure which is stimulated by the RFO signal. If the series resonance is hitting a spurious emission of the 13.56 MHz signal, issues during radiated and conducted emission testing can be the result. The issue can be mitigated by changing the capacitance value.

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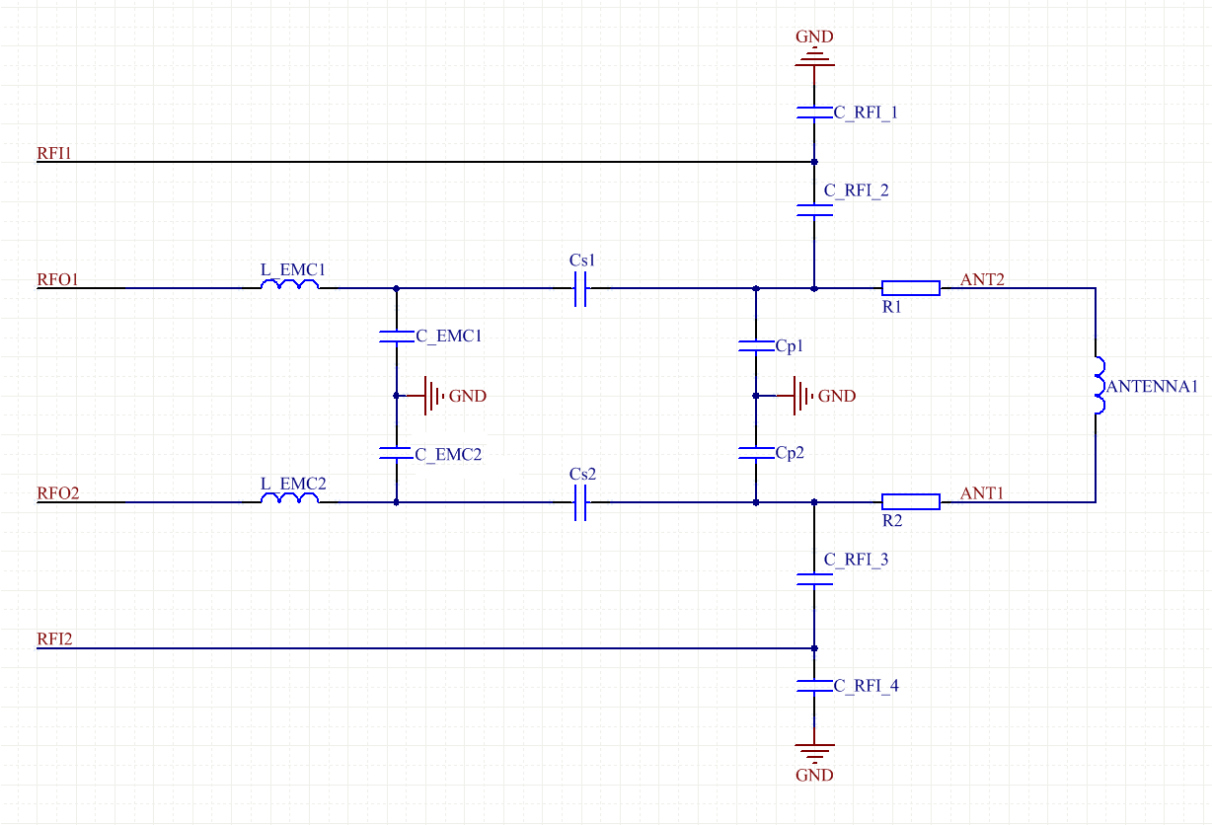
Figure 2. **Antenna circuit (including EMI filter and matching)**



3.1 Reader mode and output power

During the NFC/RFID reader design process several different requirements must be considered, a key one is the output power.

Different methods, such as inductive wake-up, can be used to reduce the power consumption of the complete system. Besides using this power saving functions or reducing the power consumption by optimizing the polling cycle, the key criterion is the power consumption during field on.

There are three steps to adjust the power consumption:

1. Impedance matching: fewest power losses
2. Antenna driver output resistance (dres, register 0x03): higher power losses
3. Chip internal regulator voltage: higher power losses

The impedance matching is the most important factor to determine the power consumption. When designing the matching circuitry and defining the target matching impedance, pay attention to Figure 6. It shows that with a higher target matching impedance less power is transferred forward to the antenna, and therefore the power consumption of the whole reader unit is reduced. Figure 6 shows the relation between the reader power and the target matching impedance.

The last point to adjust the output power is the supply voltage of the driver stage. The VDD_DR driver supply can be automatically set to VDD minus the regulator dropout voltage. This is the optimal value for operation and noise rejection. It is also possible to manually overwrite the regulator setting and set VDD_DR to a specific value. More detailed information can be found in the datasheet.

The Smith chart in Figure 3 and Figure 4 show the recommended capacitive and symmetrical matching impedance as starting point in reader mode. Measurements are explained in Section 9.4: Measurement of the target matching impedance. By keeping the quality factor low as shown in Figure 5, the antenna system supports basic and higher bit rates for the different reader mode technologies. Measurements are explained in Section 9.3: Verification of the Q factor in the frequency domain. The matching and quality factor may have to be adapted to the user requirements in a second step. Refer to Section 8.1: Capacitive antenna matching and EMC cutoff frequency for more details.

Figure 3. **Recommended capacitive matching impedance**

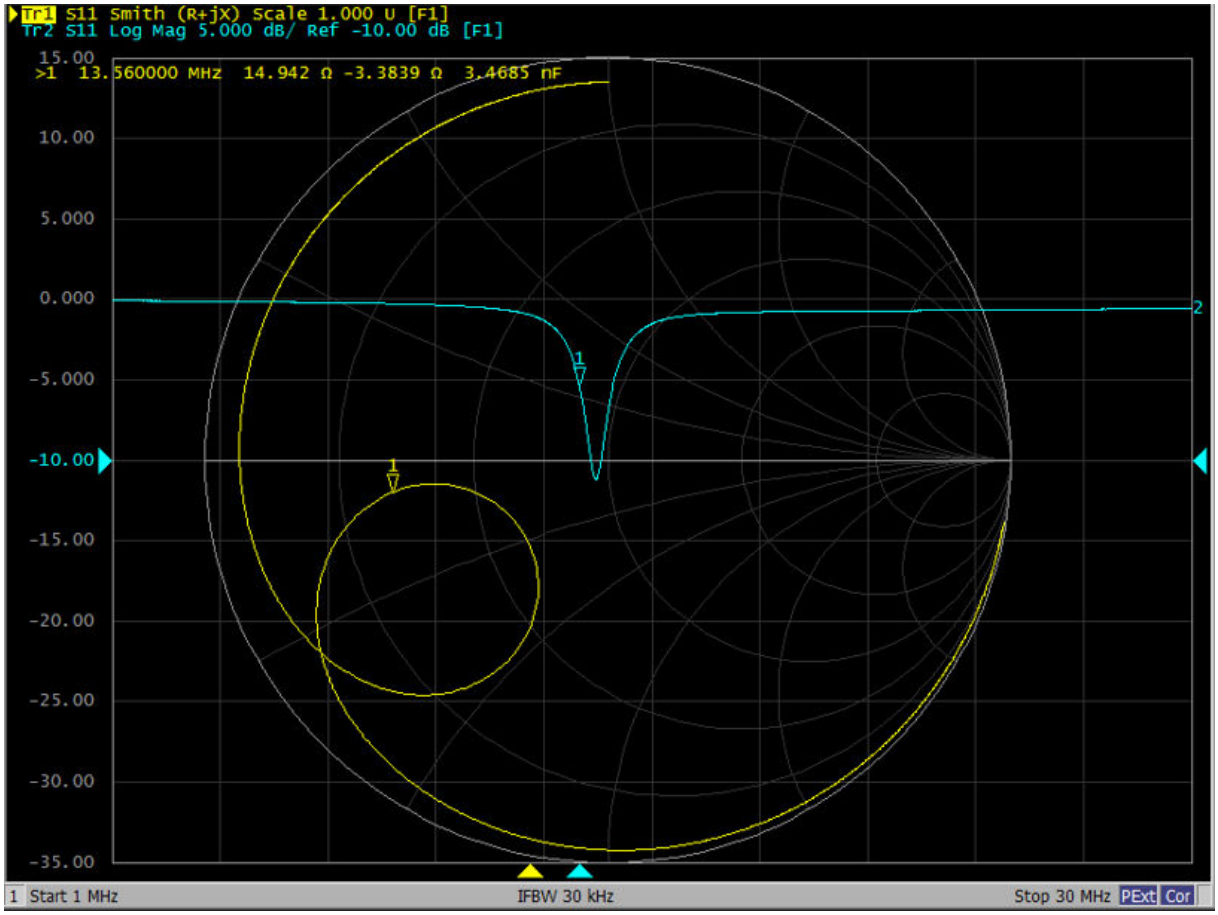


Figure 4. **Recommended symmetrical matching impedance**

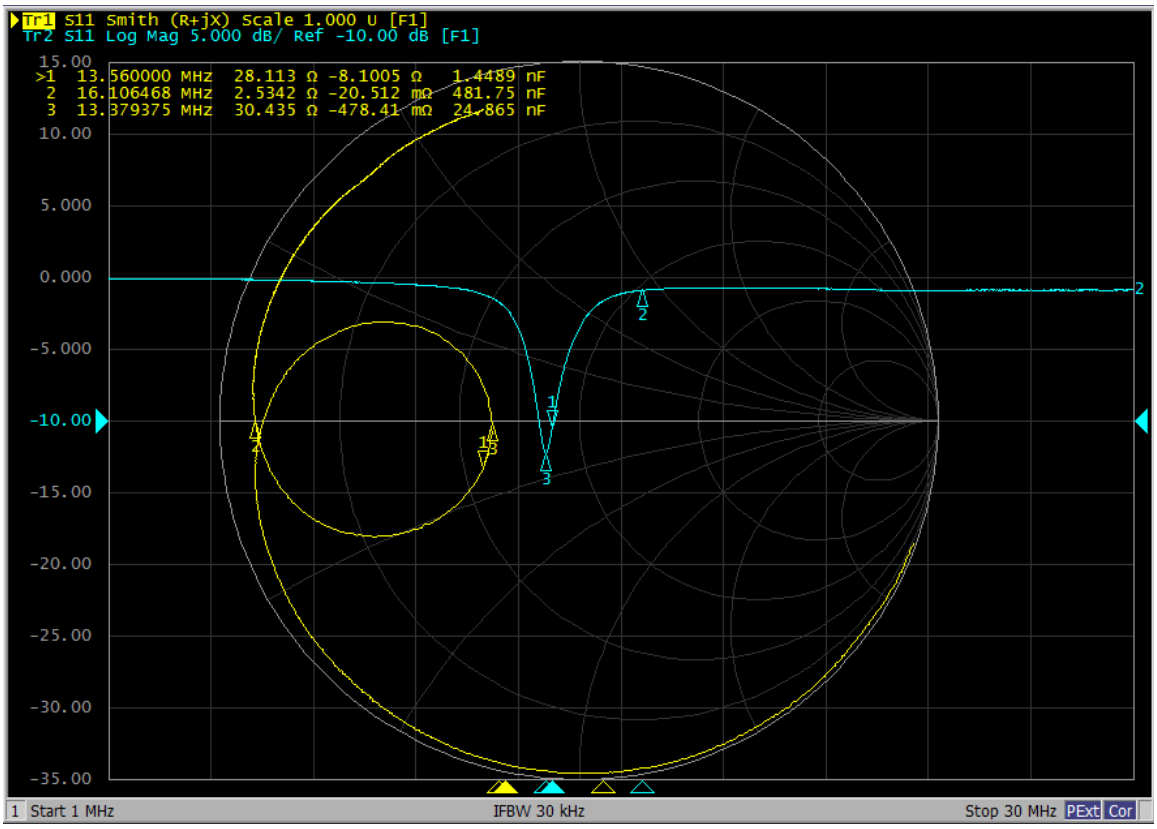
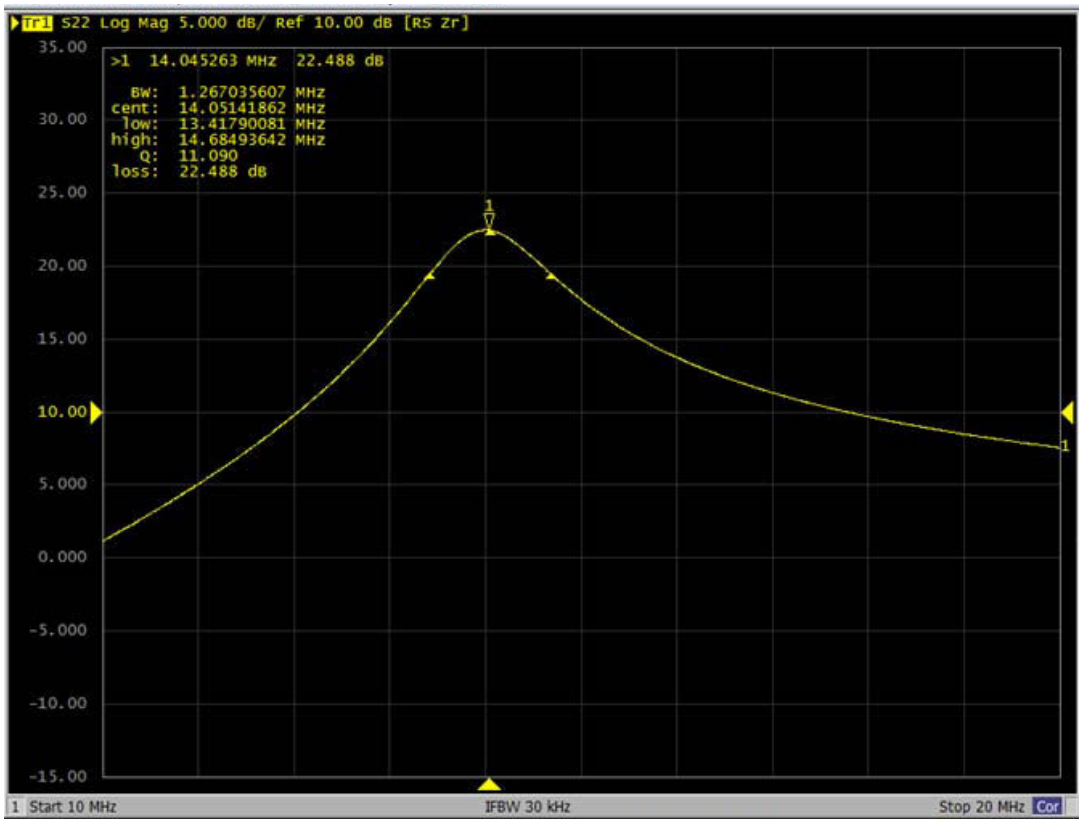


Figure 5. **Quality factor**



3.2 EMC filter

The EMC filter is implemented as a single stage low-pass filter consisting of a serial inductor and a parallel capacitor. The purpose of the EMC filter is to filter out higher harmonics caused by the rectangular output signal of the push-pull driver. The filter cutoff frequency should be between ~15 MHz (symmetrical) and ~20 MHz (capacitive).

To optimize the EMC behavior of the reader board, some considerations must be made:

- Filter coils:
  - Self-resonance frequency of the inductance: it can boost unwanted emissions in the investigated frequency range.
  - Equivalent serial resistance: influences the system Q factor of the reader, and can lower the conducted output power. EMC inductors with a higher ESR (>1 Ω) can only be used for mid and low power matchings. The ESR is put in series to the RFO output resistance. Therefore, higher ESR lower system Q factor and more power is lost in the EMC inductors.
  - The rated current of the chosen filter coils must be higher than the current in the matching network.
- Antenna design:
  - The electrical length must be kept short to avoid additional self-resonances that boost unwanted emissions.
- PCB layout:
  - Short traces between the RFO, the inductor (L), the capacitor (C), and the via to GND.

3.3 Matching network

The matching network in L topology follows the EMC filter and consists of one series and two parallel capacitors, in differential topology.

The purpose of the matching network is to match the antenna to a desired impedance value so that, depending on the application, either a maximum power transfer from the ST25R500 to the antenna or a certain current consumption is achieved.

Figure 2 shows the antenna interface stage.

3.4 Capacitive voltage divider

As the voltage on the antenna can be high, a capacitive voltage divider is needed in the receive path at the antenna terminals to limit the signal strength going back to the RFI pins. This voltage divider is connected to the antenna and consists of two capacitors.

In Figure 2 the capacitor pairs C_RFI_1/C_RFI_2 and C_RFI_3/C_RFI_4 form the capacitive voltage divider.

The voltage at the receive pins must not exceed 3 Vpp. In HF reader mode and NFC transmit mode, the recommended signal level is 2.5 Vpp.

3.5 Antenna

The antenna of the HF reader is a magnetic loop antenna, typically implemented as a printed coil. Flex PCB, wire-wound antennas, or metal casings are other possible approaches.

Factors like size, number of tracks, track, and gap width determine the electrical parameters of the antenna: inductance, series and parallel resistance, self-resonance frequency, and, most important of all, the Q factor.

The antenna must be designed with a Q factor higher than the target system Q factor. This is because the antenna Q factor can only be decreased by damping resistors afterwards, and not increased anymore.

4 Dissipated power calculation

The typical NFC application has a matching network attached to the RFO pins. This matching network transforms the inductive impedance to a real ohmic load. The EMI filter is the first part of this matching network (see Figure 6).

The EMI filter is transforming the rectangular voltage, which is outputted by the driver into a sinus-shaped voltage. As a result, the current going through the regulator is approximately sinus shaped. This is because the drivers produce a square wave voltage, but the EMC filter only passes the first harmonic.

Equation 4 takes these considerations into account.

4.1 Equations

To calculate the total dissipated power, the analog and digital logic power, the internal voltage regulator power, and the transmitter driver stage power must be summarized:

Total dissipated power

$$P_{TOT} = P_{AL} + P_{REG} + P_{DRV} \quad (1)$$

Where:

P_{TOT}= Total dissipated power [W]

P_{AL}= Analog and digital logic power [W]

P_{REG}= Internal voltage regulator power [W]

P_{DRV}= Transmitter driver stage power [W]

Analog and digital logic power

$$P_{AL} = I_{AL} \times V_{DD} \quad (2)$$

Where:

P_{AL}= Analog and digital logic power [W]

I_{AL}= Analog and digital logic current [A]

V_{DD}= Positive supply voltage [V]

Internal voltage regulator power

$$P_{REG} = V_{drop} \times I_{DD_{DR}} \quad (3)$$

Where:

P_{REG}= Internal voltage regulator power [W]

V_{drop}= LDO voltage drop [V]

$I_{DD_{DR}}$= Regulated supply current for antenna driver [A]

Regulated supply current for antenna driver

$$I_{DD_{DR}} = \frac{\left(V_{DD_{DR}} \times 1.27 \times 0.637\right)}{\left(2 \times R_{RFO} + Z_{LOAD}\right)} \quad (4)$$

Where:

$I_{DD_{DR}}$= Regulated supply current for antenna driver [A]

$V_{DD_{DR}}$= Regulated supply voltage for antenna driver [V]

R_{RFO}= Driver output resistance [Ω]

Z_{LOAD}= Target matching impedance [Ω]

The factor 1.27 (4/π) represents the amplitude of the first harmonic of a square wave with an amplitude of 1.

The factor 0.637 (2/π) represents the average of a sine wave.

Regulated supply voltage for antenna driver

$$V_{DD_{DR}} = V_{DD} - V_{drop} \quad (5)$$

Where:

$V_{DD_{DR}}$= Regulated supply voltage for antenna driver [V]

V_{DD}= Positive supply voltage [V]

V_{drop}= LDO voltage drop [V]

Transmitter driver stage power

$$P_{DRV} = {I_{PEAK}}^2 \times R_{RFO} \quad (6)$$

Where:

P_{DRV}= Transmitter driver stage power [W]

I_{PEAK}= Regulator peak current [A]

R_{RFO}= Driver output resistance [Ω]

The LDO is acting as a rectifier therefore the averaged current through the EMI filter is calculated based on Fourier.

Regulator peak current

$$I_{PEAK} = \frac{2 \times V_{REG_avg}}{2 \times R_{RFO} + Z_{LOAD}} \quad (7)$$

Where:

I_{PEAK}= Regulator peak current [A]

V_{REG_avg} = Regulator average voltage [V]

R_{RFO}= Driver output resistance [Ω]

Z_{LOAD}= Target matching impedance [Ω]

Regulator average voltage

$$V_{REG_avg} = V_{DD_{DR}} \times 0.637 \quad (8)$$

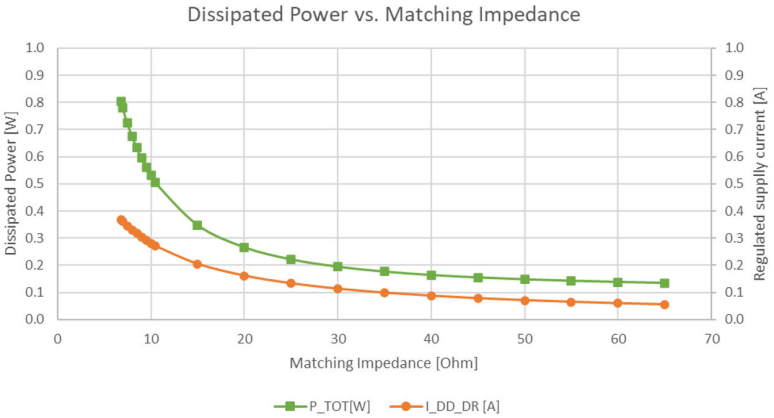
Where:

$V_{DD_{DR}}$= Regulated supply voltage for antenna driver [V]

The factor 0.637 (2/π) represents the average of a sine wave.

Figure 6 shows the dependency of the dissipated power and the target matching impedance at 5 V. The higher the matching impedance is, the lower the dissipated power and the regulated supply current.

Figure 6. Dependency of the dissipated power and the matching impedance at 5 V



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4.2 Calculation example

Given parameters:

V_{DD} = 5 V

Z_{LOAD} = 8.4 Ω

V_{drop} = 0.3 V

R_{RFO} = 1.75 Ω

I_{AL} = 0.021 A

Equation 2

$$P_{AL} = I_{AL} \times V_{DD} = 0.021 \times 5 = 0.105W$$

Equation 5

$$V_{DD_{DR}} = V_{DD} - V_{drop} = 5 - 0.3 = 4.7V$$

Equation 4

$$I_{DD_{DR}} = \frac{(V_{DD_{DR}} \times 1.27 \times 0.637)}{(2 \times R_{RFO} + Z_{LOAD})} = \frac{(4.7 \times 1.27 \times 0.637)}{(2 \times 1.75 + 8.4)} = 0.32A$$

Equation 3

$$P_{REG} = V_{drop} \times I_{DD_{DR}} = 0.3 \times 0.32 = 0.096W$$

Equation 8

$$V_{REG_avg} = V_{DD_{DR}} \times 0.637 = 4.7 \times 0.637 = 2.99V$$

Equation 7

$$I_{PEAK} = \frac{2 \times V_{REG_avg}}{2 \times R_{RFO} + Z_{LOAD}} = \frac{2 \times 2.99}{2 \times 1.75 + 8.4} = 0.503A$$

Equation 6

$$P_{DRV} = {I_{PEAK}}^2 \times R_{RFO} = 0.503^2 1.75 = 0.443W$$

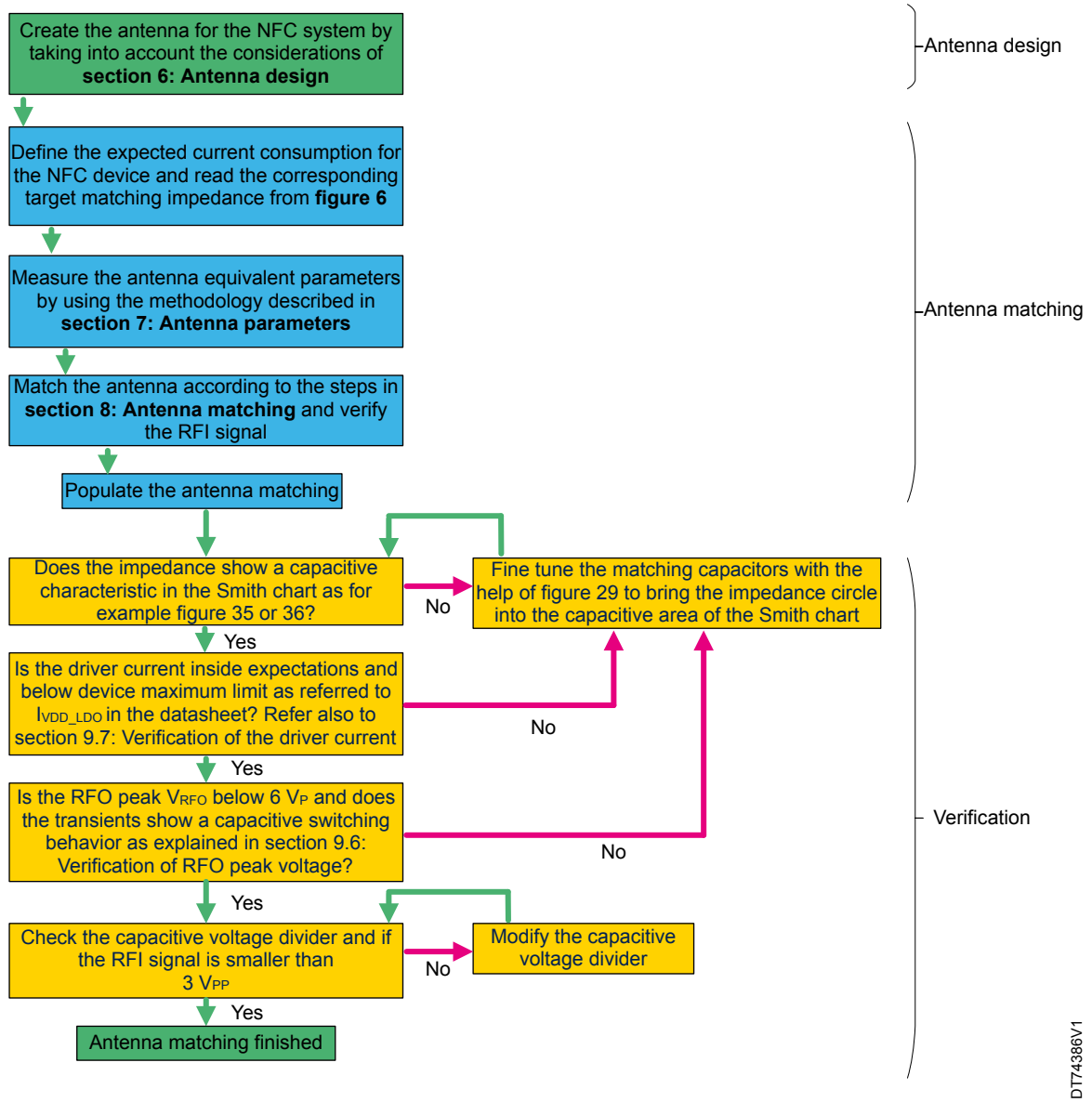
Equation 1

The total dissipated power of the device:

$$P_{TOT} = P_{AL} + P_{REG} + P_{DRV} = 0.105 + 0.096 + 0.443 = 0.64W$$

5 Step by step procedure for antenna matching and finetuning

Figure 7. Step by step antenna matching guide



6 Antenna design

6.1 Boundary conditions and simulation model

The design of a proximity reader system requires a knowledge of the end user application. This includes the environmental conditions when placing the reader or type of cards to be used.

Some basic boundary conditions need to be considered in advance, among them:

- target reading distance
- Tag / card type
- Output power
- EMC regulations
- Industrial design
- Antenna placement
- Environmental influences
- Supported NFC technologies and standards, and data rates.

It is sometimes difficult to place the magnetic loop because of the industrial design of the application. The best case of an antenna placement is far away from electronics or other components like batteries, displays, or large ground planes that harm the effective radiated RF field.

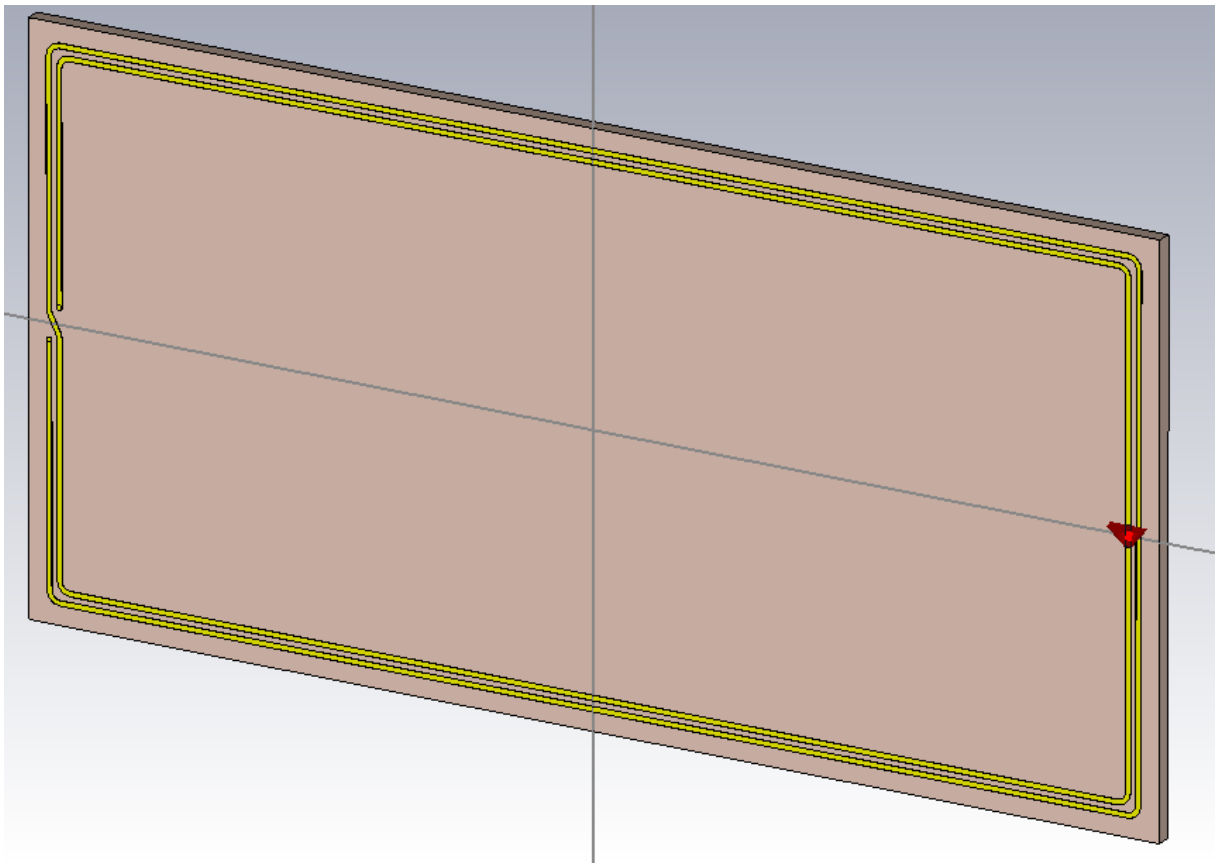
As guidelines for the antenna design, three antennas of different (but no specific) sizes have been simulated. All of them have a constant number of tracks (two) with a copper thickness of 35 µm on an FR4 plate, with a thickness of 1.5 mm.

The characteristics of the three antennas are the following:

- Size: large, middle, small
- Trace width: 0.5; 1; 1.5 mm
- Gap width: 0.5; 1; 1.5 mm

Figure 8 shows the EM - simulation model with the biggest size. The simulations have been carried out in the frequency domain.

Figure 8. Simulation model of the coil antenna



To find the dependency of the antenna Q factor and of its other parameters upon the geometry, the trace width and the gap width between traces, as well as the antenna size, have been varied in the simulation.

6.2 Simulation results

The main antenna electrical parameters, as a function of antenna size, trace and gap width, are shown in figures Figure 9 to Figure 13 summarizes their behavior.

Additional antenna parameters like inductance, series DC resistance, parallel resistance, and self-resonance frequency influence the Q factor, too.

The Q factor of a parallel resonance circuit is:

$Q = R_{PANT} / (2 \pi f_{carrier} L)$

Where:

- R_{PANT} is the total parallel resistance. See Section 7.3: Antenna equivalent circuit for details
- L is the antenna inductance
- $f_{carrier}$ is the carrier frequency

The self-resonance frequency depends on the electrical length of the antenna. The shorter the electrical length, the higher this frequency. Further it also depends on the parasitic capacitance of the antenna, the number of turns, the spacing between the turns, the use of ferrite and the coupling with surrounding conductive parts.

Figure 9. **Antenna Q factor vs. antenna size, trace, and gap width**

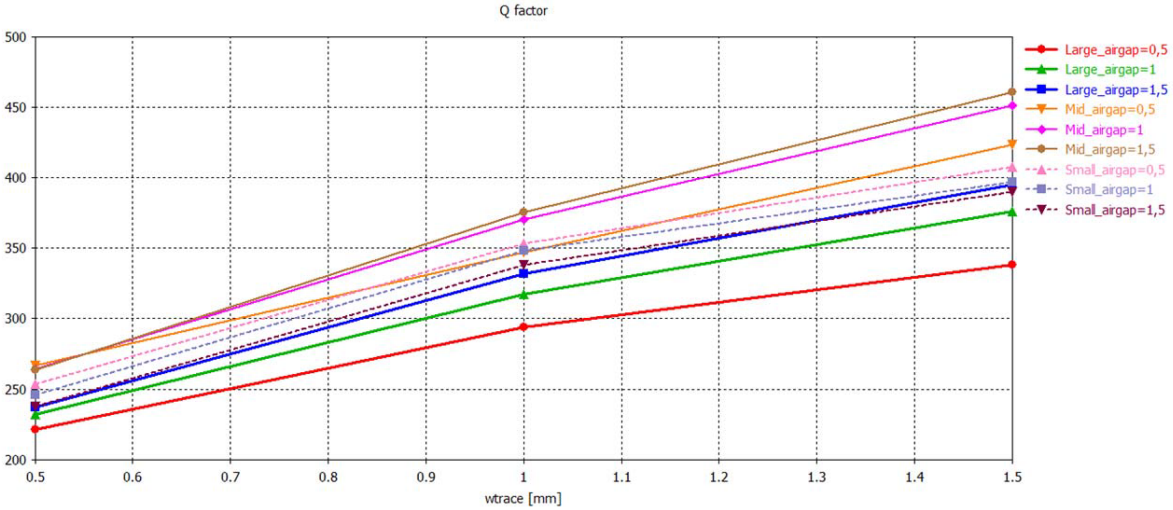


Figure 10. **Inductance vs. antenna size, trace, and gap width**

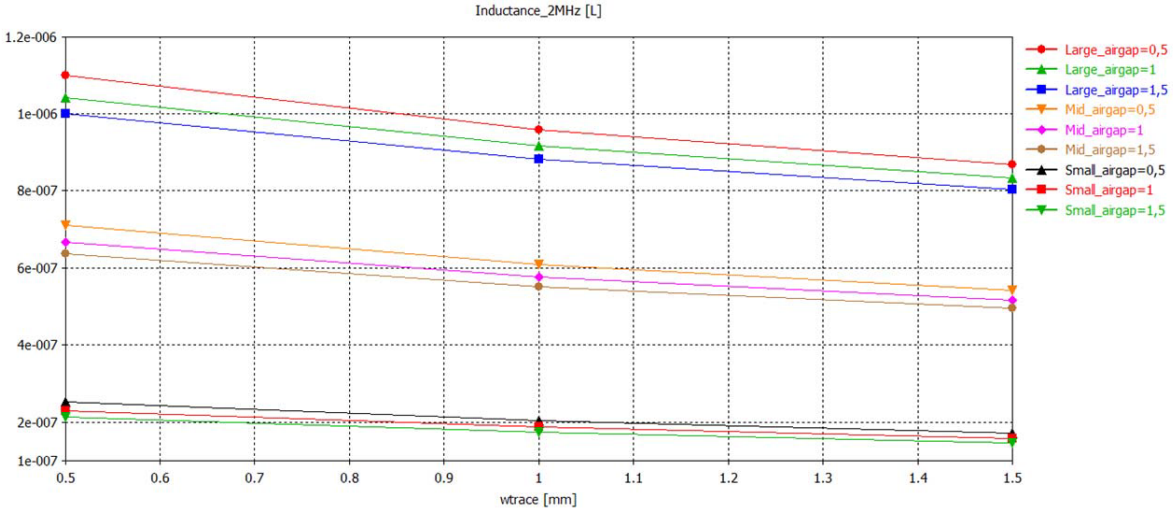


Figure 11. **Series DC resistance vs. antenna size, trace, and gap width**

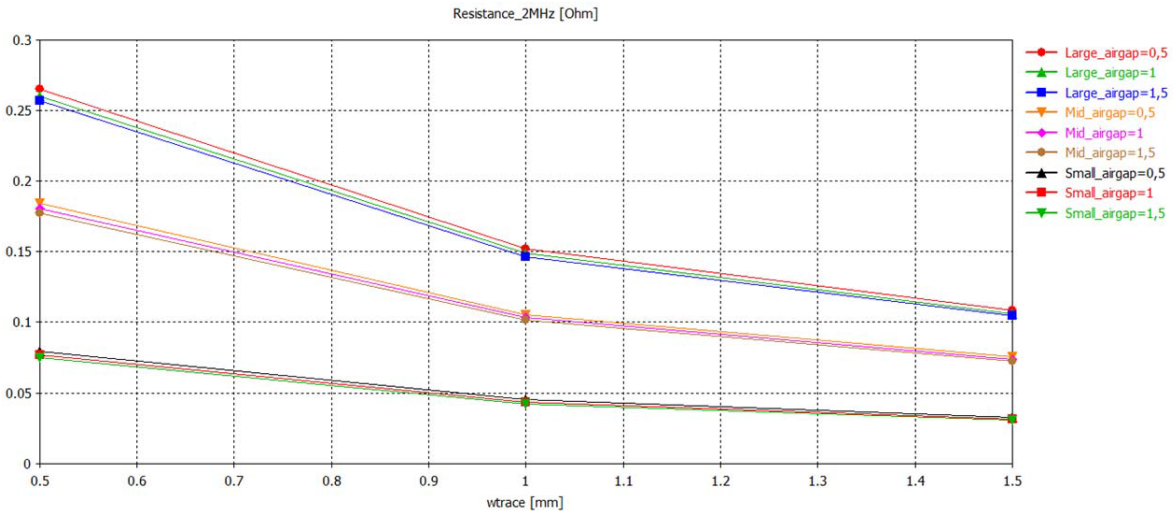


Figure 12. **Parallel resistance vs. antenna size, trace, and gap width**

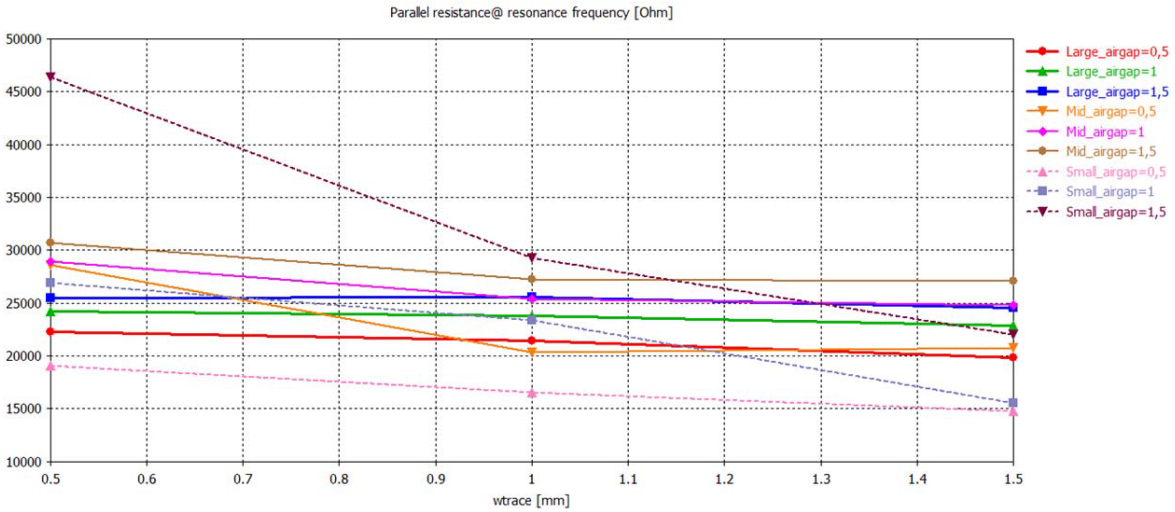


Figure 13. **Resonance frequency vs. antenna size, trace, and gap width**

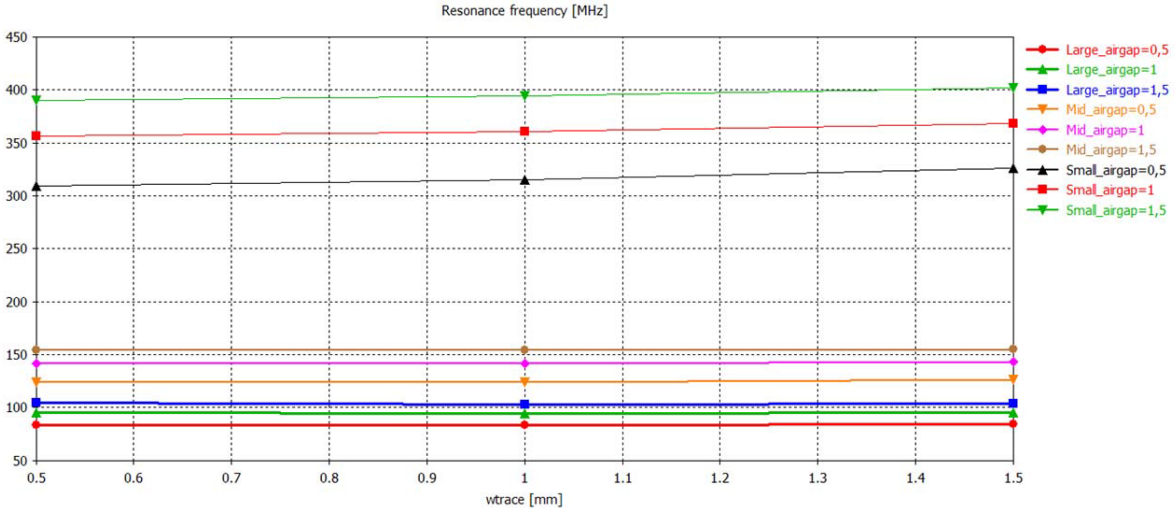


Table 2. Behavior of antenna parameters vs. geometrical parameters

Parameter	Action	Effect on parameter	Q factor
Q factor	Increase trace width	-	Increases
	Increase gap width		
Inductance	Larger antenna	Increases	Decreases
	Decrease trace width		
	Decrease gap width		
Series DC resistance	Larger antenna	Increases	Decreases
	Decrease trace width		
	Decrease gap width		
Parallel resistance	Decrease trace width	Increases	Increases
	Increase gap width		
Resonance frequency	Smaller antenna	Increases	Increases
	Increase gap width		

Note: The separated view of each antenna parameter is a theoretical one to understand the basic behavior. In reality, all parameters are linked together, for example, if the inductance is increased by a larger antenna (lower Q), the electrical length increases, which in turn lowers the resonance frequency (Q increases) and the series DC resistance increases (lowering Q).

The inductance of magnetic loop antennas is defined by the electrical length of the conductor. The longer and thinner the way the signal has to travel (more electrical length) the higher the inductance of the coil. On the other hand, the wider and shorter a transmission line is the more capacitive its behavior. Changing the inductance of a loop antenna may thus be realized by altering the thickness of the turns, the gap width, or the size of the antenna.

A value to be targeted in loop antenna design for NFC reader applications is in the 200 to 1500 nH range. Depending on the application higher inductance values can be chosen and are supported by the chip.

In direct relation to the change of the inductance stands the series resistance of the loop antenna, which increases with longer and thinner turns. The antenna self-resonance frequency shows the tendency to increase with larger gap widths between the antenna tracks and also with decreasing size of the antenna.

As mentioned in Section 6: Antenna design the antenna has to be designed with a Q factor higher than the one needed for the application. The reason is that the Q factor can be decreased by a damping resistor connected at the antenna pins, but it cannot be increased anymore, except with a redesign of the antenna.

7 Antenna parameters

Every antenna is composed of inductance, resistance, and capacitance. These values and the self-resonance frequency of the antenna must be determined first to calculate the antenna equivalent circuit and its Q factor, and then determine the matching components.

7.1 Network analyzer preparation

In order to measure the antenna parameters, a network, or impedance analyzer is used and set up according to the procedure detailed below:

1. Set the measurement mode of the network analyzer to S11 reflection measurement
2. Use the Smith chart format (R + jX) to display the impedance curve
3. Set the start frequency at 1 MHz and the stop frequency at 300 MHz

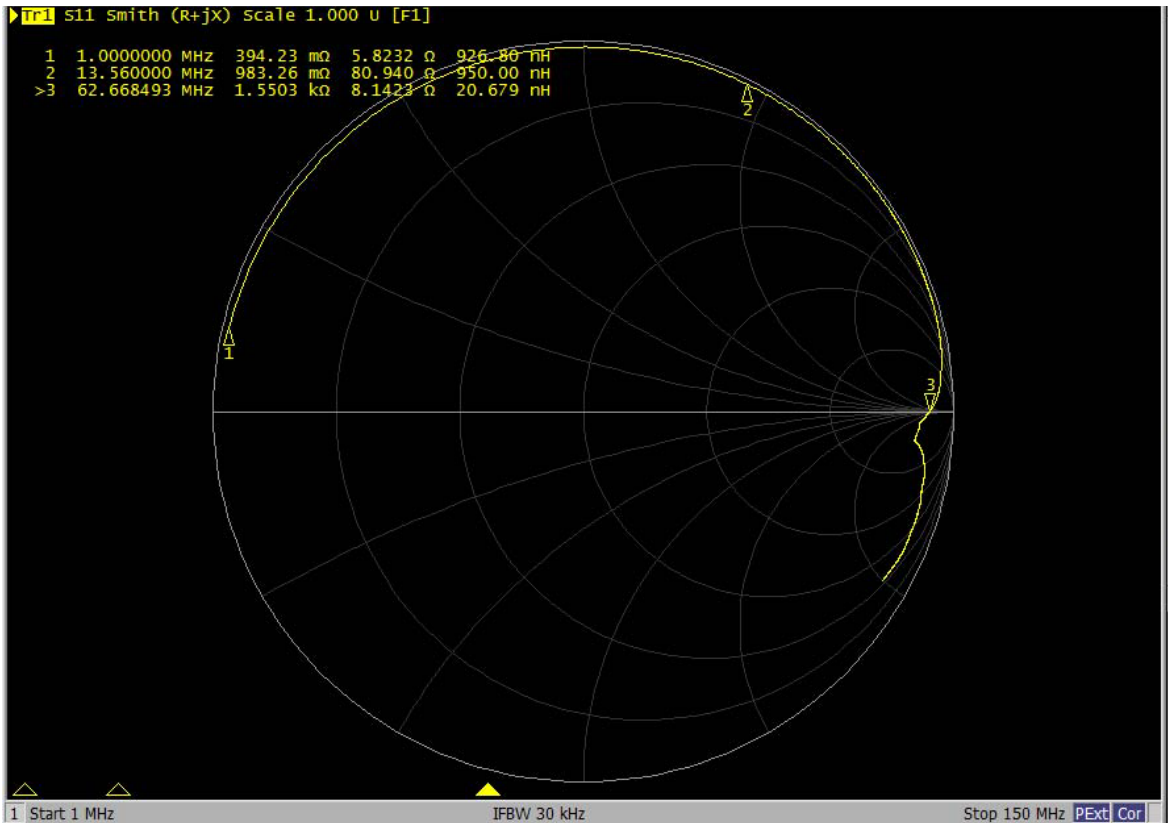
Note: Some of the antenna parameters are measured at 1 MHz, far off the self-resonance frequency of the antenna to minimize the skin effects measured at higher frequencies. The stop frequency must be higher than the first self-resonance frequency (usually between 50 and 250 MHz) of the reader antenna.

4. Set the network analyzer resolution (number of points) to the maximum to ensure accurate measurements
5. Connect a short SMA cable (<50 cm) to the RF port of the network analyzer and start the calibration using OPEN, SHORT, and LOAD from a calibration kit or autocalibration. If no calibration kit is available, a workaround with a 50 Ω resistance as load, as well as an open and short connection on the cable can be used. With the calibration the SMA cable length is accounted for.
6. To connect the SMA cable to the antenna to be measured, a probe connection from pins (one pin soldered to the signal connection of an SMA connector, the other one soldered to one of its ground connections) must be made.
7. The added pins can be taken into account for calibration with the auto port extension function of the VNA.

7.2 Parameter measurement

1. The impedance curve from 1 to 300 MHz is displayed in the Smith chart (see Figure 14)
2. Set a marker to 1 MHz and read the series inductance and the DC series resistance values (in Figure 14 they are displayed in the upper part of the network analyzer screen):
   - L_{ANT} = 926 nH
   - R_{SDC} = 394 mΩ
3. Set another marker to the real axis of the Smith chart, where the inductive and the capacitive parts of the impedance cancel each other. At this point, the parallel resistance and the self-resonance frequency of the antenna are measured:
   - $R_{P@fres}$ = 1.55 kΩ
   - f_{res} = 62.67 MHz

Figure 14. **Antenna parameter measurement at 1 MHz and SRF (62.67 MHz)**



The antenna parameters have now been measured, and the equivalent circuit can be determined, as described in Section 7.3: Antenna equivalent circuit.

7.3 Antenna equivalent circuit

Using the antenna inductance measured at 1 MHz, the parasitic capacitance at self-resonance-frequency can be calculated as follows:

$$C_{ANT} = 1 / (\omega^2 * L) = 1 / [(2\pi * f_{res})^2 * L_{ANT}] = 1 / [(2\pi * 62.7\ MHz)^2 * 926\ nH] = 6.96\ pF$$

The measured value of the parallel resistance has to be converted from the self-resonance to the operating frequency (fwork = 13.56 MHz). The reason for this conversion is the correction for the frequency-dependent change due to the skin effect. To convert the parallel resistance at the self-resonance frequency, a correction factor has to be calculated:

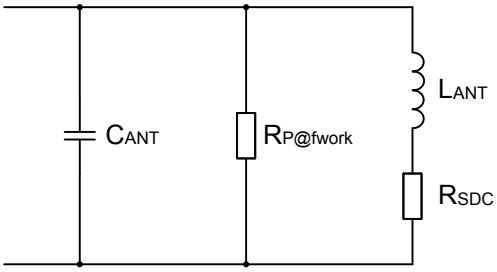
$$K = \sqrt{\frac{f_{res}}{f_{work}}} = \sqrt{\frac{62,7MHz}{13.56MHz}} = 2.15$$

The parallel resistance at the operating frequency is calculated as

$$R_{P@fwork} = K * R_{P@fres} = 2.15 * 1.55\ k\Omega = 3.33\ k\Omega$$

All antenna components are now known, so the equivalent circuit can be determined (see Figure 15).

Figure 15. Antenna equivalent circuit



The equivalent circuit can be simplified by recalculating the series resistance into a parallel resistance (see Figure 16) at the operating frequency, with the formula:

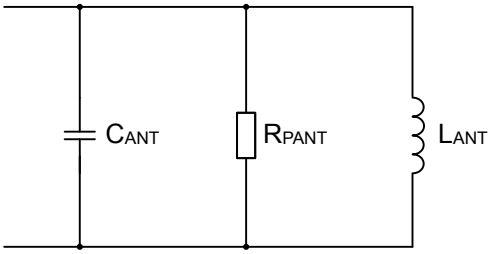
$$Q = \frac{\omega L_{ANT}}{R_{SDC}} \approx \frac{R_{PDC}}{\omega L_{ANT}} \Rightarrow R_{PDC} = \frac{(2 \cdot \pi \cdot f_{res} \cdot L_{ANT})^2}{R_{SDC}} = \frac{(2 \cdot \pi \cdot 13{,}56\text{MHz} \cdot 926\text{nH})^2}{394\text{m}\Omega} = 15.9\text{k}\Omega$$

The total resistance for the antenna equivalent circuit can be represented by a parallel resistance consisting only of the DC series resistance (recalculated into a parallel one), and the parallel resistance converted to the operating frequency.

Adding the two parallel resistances leads to the total parallel resistance:

$$R_{PANT} = \frac{R_{PDC.} \cdot R_{P@fwork}}{R_{PDC} + R_{P@fwork}} = \frac{15.9\Omega \cdot 3.33\text{k}\Omega}{15.9\text{k}\Omega + 3.33\text{k}\Omega} = 2.76\text{k}\Omega$$

Figure 16. Antenna equivalent circuit (final)



The values for the final and simplified antenna equivalent resonance circuit are:

- R_{PANT} = 2.76 kΩ
- C_{ANT} = 6.96 pF
- L_{ANT} = 926 nH

The maximum achievable Q factor for this antenna can now be calculated:

Q = R_{PANT} / (ω * L_{ANT}) = 2.76 kΩ / (2 π * 13.56 MHz * 926 nH) = 34.8

This Q factor is valid for the freely oscillating unconnected antenna.

The Q factor has a direct influence on the rise and fall times of the modulated signal.

Figure 17 and Table 3 show the definition of rise and fall times for a Type-A signal modulated with 100% ASK and a data rate of 106 Kbit/s (f_{work} / 128), while Figure 18 is an example of their dependence on the Q factor.

Figure 17. Definition of timing parameters for Type-A with 106 Kbit/s (ISO/IEC 14443-2)

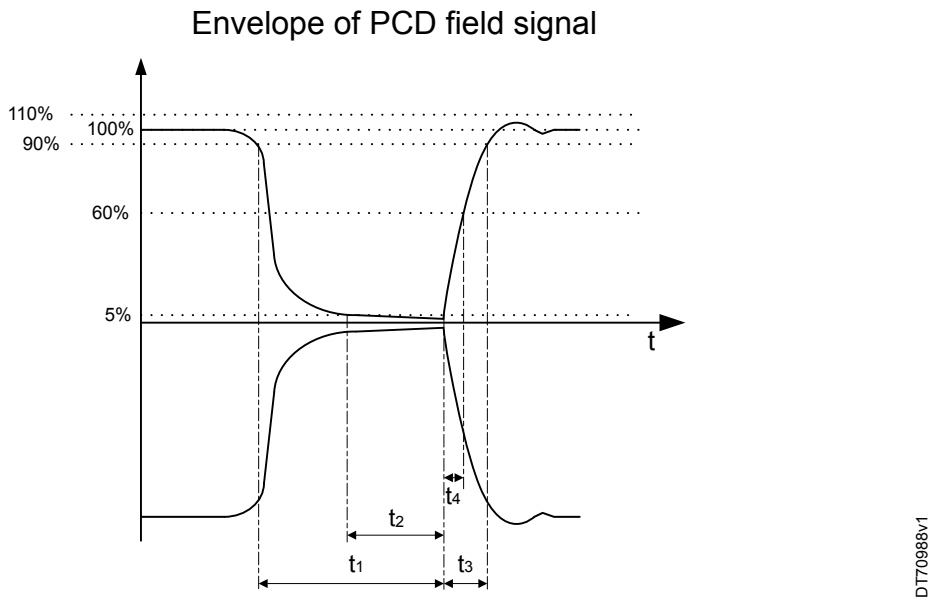
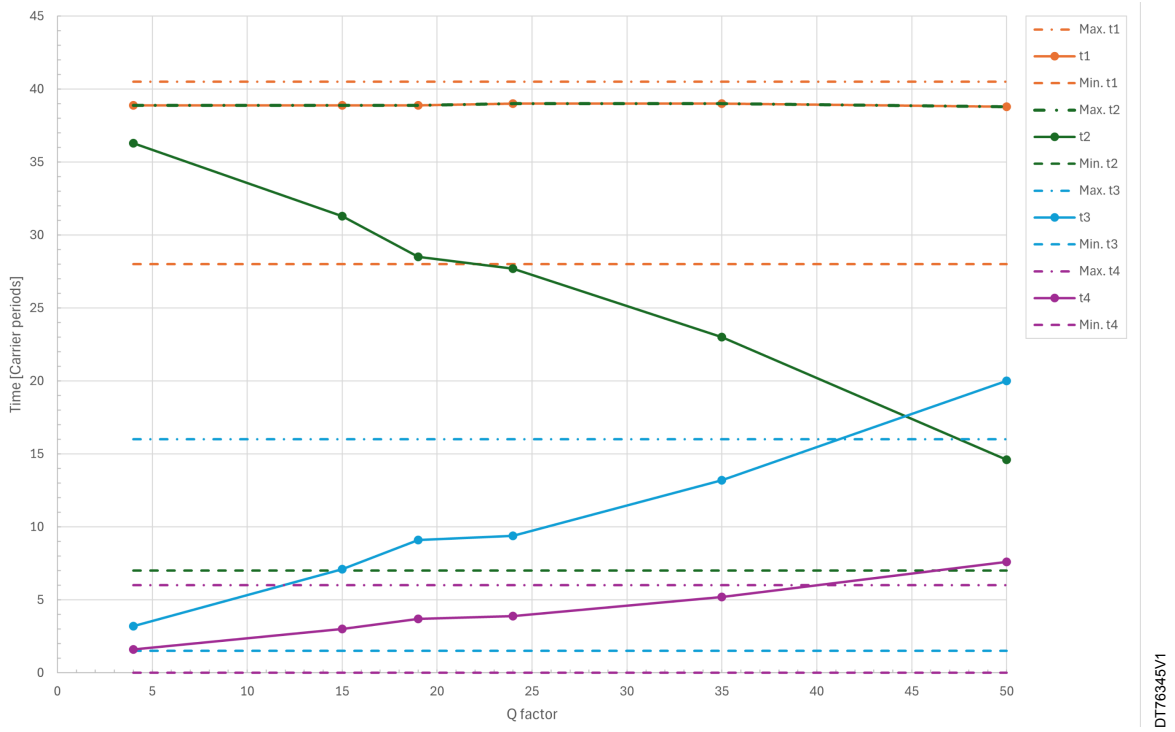


Table 3. Timing parameters for Type-A with 106 Kbit/s

Parameter	Condition	Min.	Max.
t_1	-	28 / fc	40.5 / fc
t_2	t1 > 34 / fc	7 / fc	t_1
	t1 ≤ 34 / fc	10 / fc	
t_3	-	1.5 x t_4	16 / fc
t_4	-	0	6 / fc

Figure 18. Timing parameters vs. Q factor



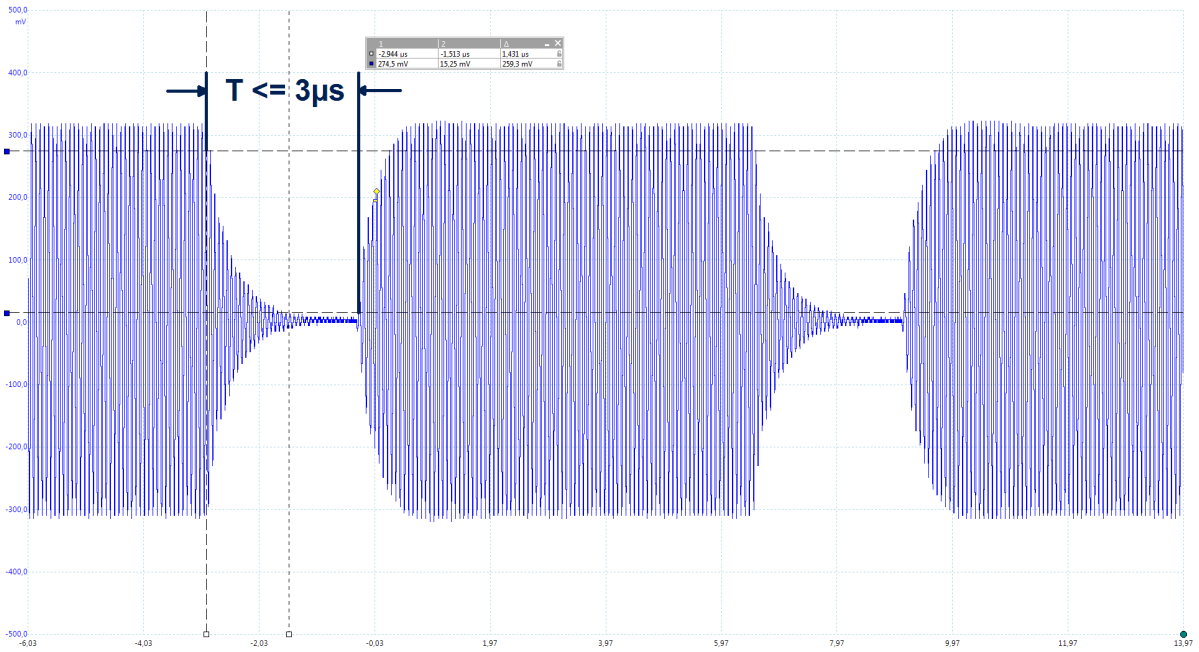
For each protocol (Type-A, Type-B) and data rate a maximum allowable Q factor can be determined, it must not be exceeded to get a modulated signal compliant with ISO waveforms.

The calculation of the maximum allowable Q factor for Type-A with a data rate of 106 Kbit/s is based on the time - bandwidth product (TBP), and a on a definition of the Q factor resulting in the following equation:

$B[MHz] * T[\mu s] \geq 1$; $Q = f_{work} / B \rightarrow Q \leq f_{work} * T \rightarrow Q \leq 13.56\ MHz * 3\ \mu s = 41$

In the above calculation the time T, represented in Figure 19, is the highest possible value of the timing parameter t1 according to the ISO 14443 standard.

Figure 19. Definition of t_1 for Type-A with a data rate of 106 Kbit/s



The Q factor for the application must be below 41 (for Type-A and 106 Kbit/s) to achieve standard-compliant rise and fall times, hence the previously calculated Q factor is too high and has to be lowered. This is achieved by connecting an external parallel resistor (RQ) at the antenna pins. The resistor value depends upon the targeted Q factor (8), and is determined as follows:

$R_T = Q * \omega * L_{ANT} = 8 * 2\ \pi * 13.56\ MHz * 926\ nH = 631\ \Omega$

Taking the parasitic resistor RPANT from the antenna equivalent circuit into account, the effective resistor RQ to adjust the Q factor to 20 is calculated by the formula below:

$R_Q = (R_{PANT} * R_T) / (R_{PANT} - R_T) = (2.76\ k\Omega * 631\ \Omega) / (2.76\ k\Omega - 631\ \Omega) = 818\ \Omega$

The closest available component value is 820 Ω.

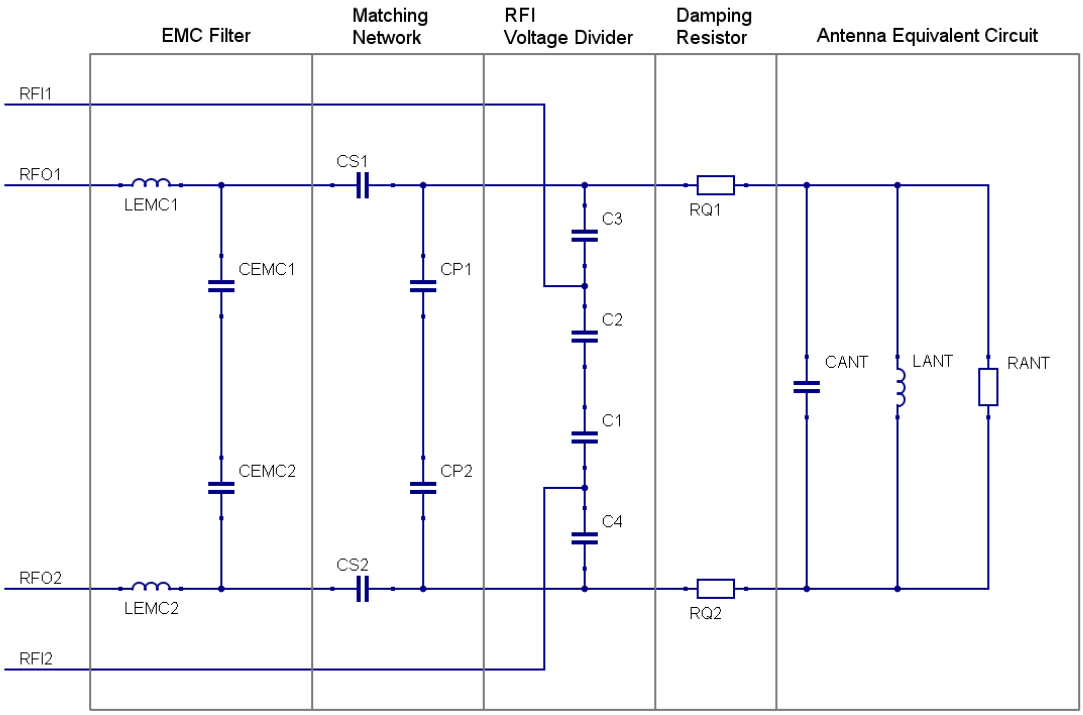
The explanation of how to determine the antenna equivalent circuit and the resistor for the Q factor adjustment is the theoretical background on which the ST25R antenna matching tool is based on.

8 Antenna matching

The whole antenna interface stage consisting of EMC filter, matching network, RFI voltage divider and antenna equivalent circuit together with the resistor for the Q factor adjustment is represented in Figure 20 as a differential topology.

The EMC filter is a one stage filter made up of a series inductor and a parallel capacitor to ground. The matching network consists of a series and a parallel capacitor, whereas just one parallel component is used in this topology. The resistor for the Q factor adjustment is a series resistor. The antenna is shown as an equivalent circuit consisting of a series inductor, a parallel resistor, and a parallel capacitor. The voltage divider for the receive path is capacitive and connected directly at the antenna pins.

Figure 20. Differential matching topology



8.1 Capacitive antenna matching and EMC cutoff frequency

Asymmetric and capacitive matchings are commonly used terms that relate to the selection of the EMI cutoff frequency and the way the Smith chart looks like.

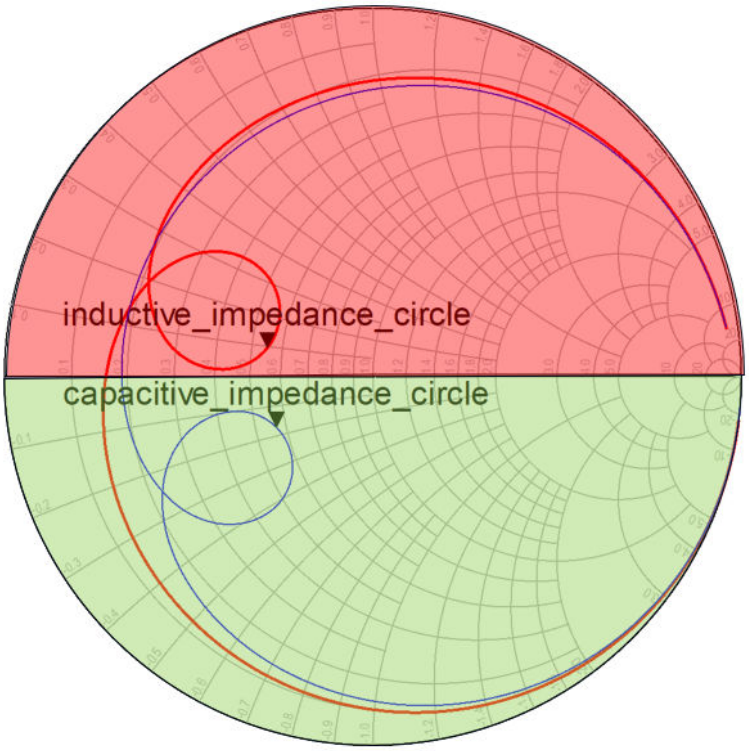
For ST25R500 it is strongly recommended to implement a cutoff frequency between 15 and 20 MHz, which brings various benefits in order to ensure the correct operating conditions detailed on the device electrical characteristics.

With capacitive matchings, the impedance seen by the RFO drivers increases in most cases with the coupling factor. In other words, the closer the tag, the higher the matching impedance which in turn automatically lowers the output power and the Tx current. This is beneficial because when the tag is close, the Tx current remains below the maximum limit.

Furthermore, capacitive matchings greatly reduce the transients at RFO pins compared to inductive matched loads.

Section 9.6: Verification of RFO peak voltage and Section 9.7: Verification of the driver current describe how to verify that design implementation operates within limits.

Figure 21. Inductive and capacitive areas



The Smith chart above depicts the inductive area in red (above), and capacitive area in green (below).

The ST25R500 requires a capacitive reactance at 13.56 MHz (approximately from -j4 Ohm to -j8 Ohm and capacitor tolerances of 1%). The impedance circle could be in the capacitive region or symmetrical along the real axis of the Smith chart.

A capacitive matching is used, if a slower rise time is needed. A symmetrical matching is used, if a faster rise time is needed. It is important to follow the instructions in Section 5 to avoid omitting important steps in the design procedure.

Table 4 shows the resulting Smith charts of four different matching examples.

The recommended RFO signal behavior as shown in Figure 43 can be achieved by keeping the resonance circle in the capacitive area of the Smith chart, as shown in Figure 37 and Figure 38 examples.

Figure 39 and Figure 40 show two nonrecommended matching examples with inductive switching characteristics.

8.2 Matching tool

The STMicroelectronics ST25R antenna matching tool is a straightforward tool to determine the matching for the antenna once the electrical antenna parameters have been measured. The tool comes with an intuitive GUI to guide the user through the process of finding the component values. Additionally, a program called qucs circuit simulator can be started directly from the GUI. The Qucs simulation tool can be used to perform AC,

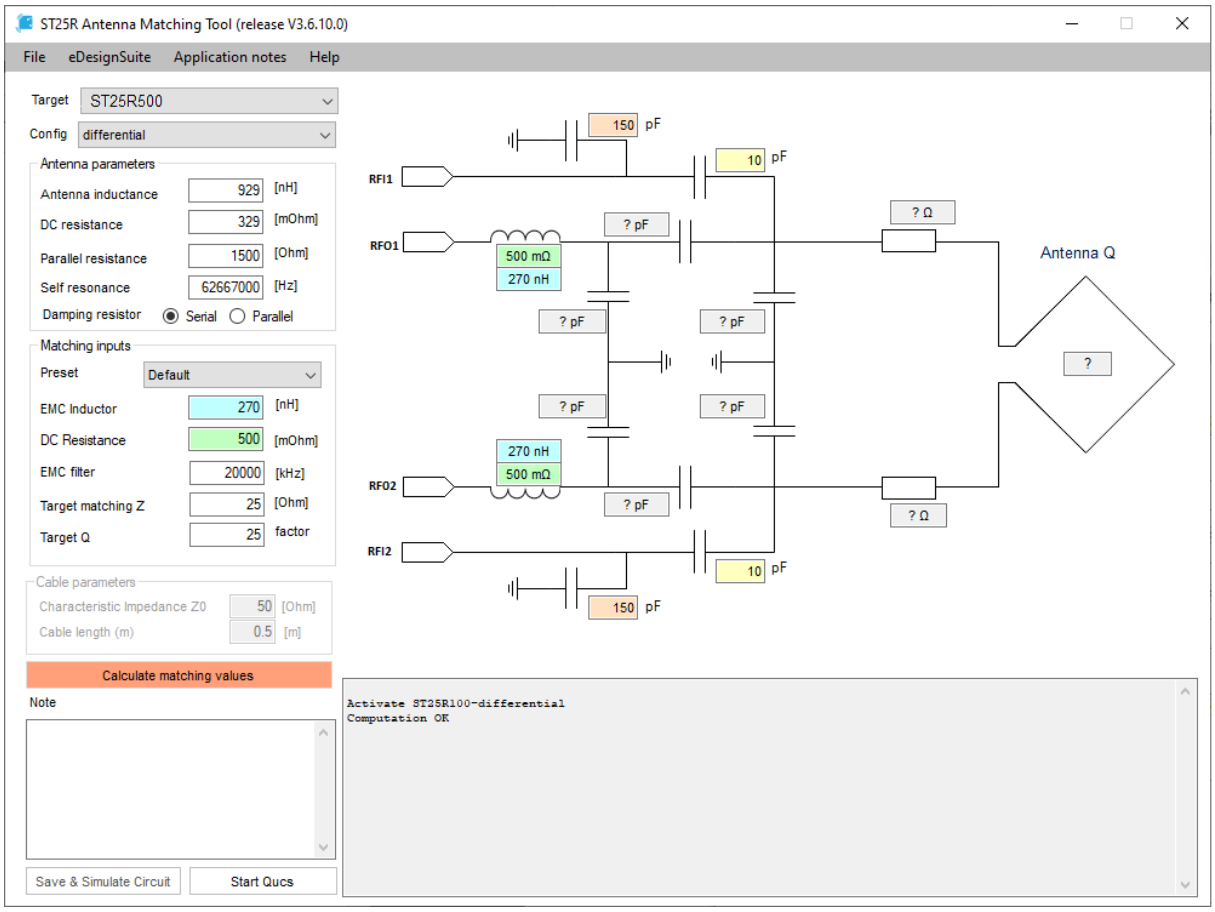
S-Parameter and transient simulations to verify the component values.

Qucs is integrated into the ST25R antenna matching tool installer, and can also be freely downloaded at http://sourceforge.net (it is recommended to use version number 0.0.18, the one embedded into the ST25R antenna matching tool). As for the installation path, do not use the default Windows directory, but rather a path like C:\Tools\Qucs. To open the matching tool, download the executable (STSW-ST25R004) from www.st.com. The main window is shown in Figure 22.

The process flow is from top to bottom, made up of five basic steps:

1. Insert the measured antenna input parameters at 1 MHz and SRF
2. Select a precondition, or define your own condition
3. Define EMC filter coil inductance and DC resistance
4. Enter the target matching impedance and target Q factor
5. Calculate and simulate the computed values

Figure 22. ST25R antenna matching tool - main window



The first step is already completed in Figure 22: as described in Section 7.2: Parameter measurement the antenna parameter have already been entered in the input parameter fields.

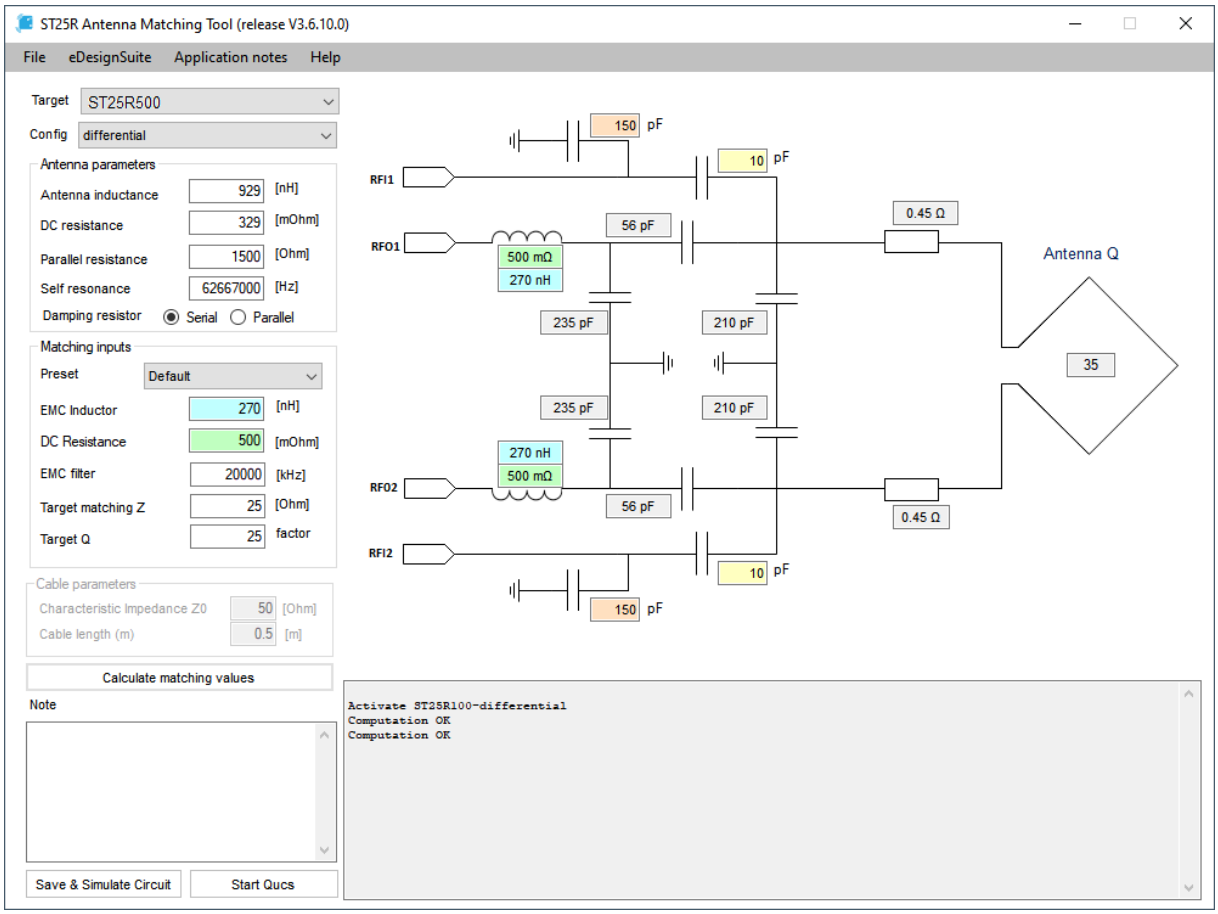
In the matching inputs area, enter the desired EMC filter cutoff frequency, the target matching impedance and the desired antenna Q factor. There are predefined example/presets, either select one of them or define your own condition, depending on the application.

The third step is to choose a value for the inductance of the EMC filter.

The selected EMC filter frequency and inductance are dependent on each other and may have to be adapted. The EMC filter capacitor value is calculated from these two inputs. Depending on the chosen EMC inductors, a proper inductor DC resistance has to be entered. This value can be found in the datasheet of the inductor. The antenna Q factor is shown after the computation in the schematic area. If the desired Q factor is higher than the calculated antenna Q factor, a negative damping resistor value is displayed.

By clicking the “Calculate” button all the component values are calculated and shown in the schematic part (Figure 23).

Figure 23. ST25R antenna matching tool - calculated matching components



Parasitic (like ESR of the capacitors) and special component parameters are not taken into account.

With all values calculated the results can now be simulated: click on Simulate Circuit, a save dialog pops up asking to save the schematic file. Carefully choose the data destination (depending on the r/w permissions), the suggested location is

`%userprofile%\.qucs\PROJECT_prj (PROJECT = Project Name; _prj = QUCS suffix)`

If the schematic files need to be loaded to continue the simulations, Qucs can be started by pressing the “Start Qucs” button. If the files are saved in above mentioned location, Qucs automatically finds and displays them in the projects panel.

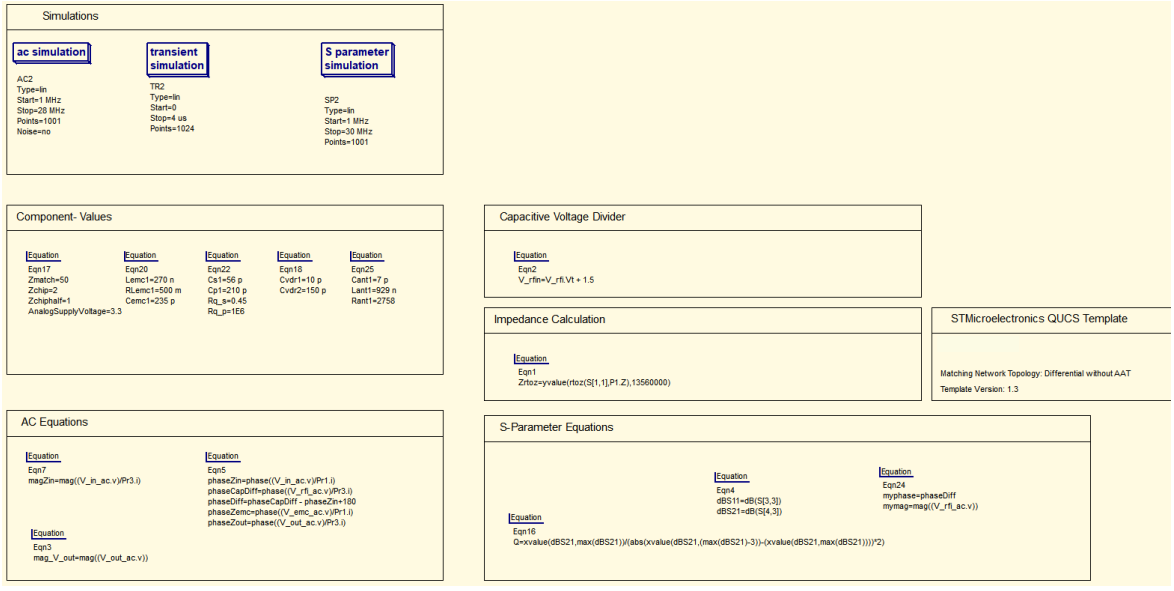
8.3 Simulation

If Qucs has been started via the “Simulate Circuit” button and the schematic files have been saved accordingly, Qucs automatically loads the schematics. If this does not happen, use the file-open dialog to load the schematics.

Qucs uses a schematic file to setup the simulation and a display file for the results. The before-calculated values are automatically inserted in a Qucs schematic template, displayed while saving.

The component values and simulation parameters are found in the top section of the sheet, which also contains formulas required for the display file/view. It is strongly recommended to change component values only in the section “Component-Values” and not in the simulation model itself. Figure 24 shows the antenna parameters, very similar to the before-calculated values.

Figure 24. Simulation parameters



8.3.1 Models

Three models are used to perform simulations:

1. S-parameter model (Figure 25) is used to calculate the target matching impedance in the Smith chart. 50 Ω is used as source impedance to compare the results with the VNA. The results are shown in Figure 28. Simulation results of the S-parameter and the AC model.
2. Transient simulation (Figure 26) checks the waveform of the OOK and calculates the RFI Voltage to define the capacitive voltage divider values. The estimated IC output driver impedance of 2 Ω is used. The results are shown in Figure 30. Fine tuning of the matching circuit.
3. AC simulation (Figure 27) calculates the reflection and transmission coefficients (S11 and S21) with the IC output driver impedance of 2 Ω. This is used to calculate the Q factor, the phase differences between RFO and RFI and to monitor the relation between the resonance frequencies of the antenna and EMC filter stages. The results are shown in Figure 28. Simulation results of the S-parameter and the AC model and Figure 30. Fine tuning of the matching circuit.

Figure 25 shows the S-Parameter model, while “Component-Values” and “Antenna-Trim” areas are shown in Figure 24. The values assigned here are automatically linked to all three models.

The difference between S-parameter and AC model is the impedance of the power source.

While measuring the impedance (S-parameter measurement) the matching network and antenna is powered by this VNA. The impedance of the VNA is in most cases 50 Ω, therefore the source impedance of the S-parameter model has to be 50 Ω.

The transient model is powered by two periodic rectangular voltage pulse sources. Every source represents one single ended driver stage. The output resistance of the driver stage can be defined by setting ZRFO.

The AC model is used to simulate the matching network during normal operation, hence the source impedance of the AC power source must correlate with the chip impedance. The forward reflection (S11) and forward transmission coefficients (S21), as well as the phase and magnitude characteristics can be calculated with this simulation. At the end, the results are displayed in a new tab. It is also possible to include further simulations, like parameter sweep.

Figure 25. S-parameter model

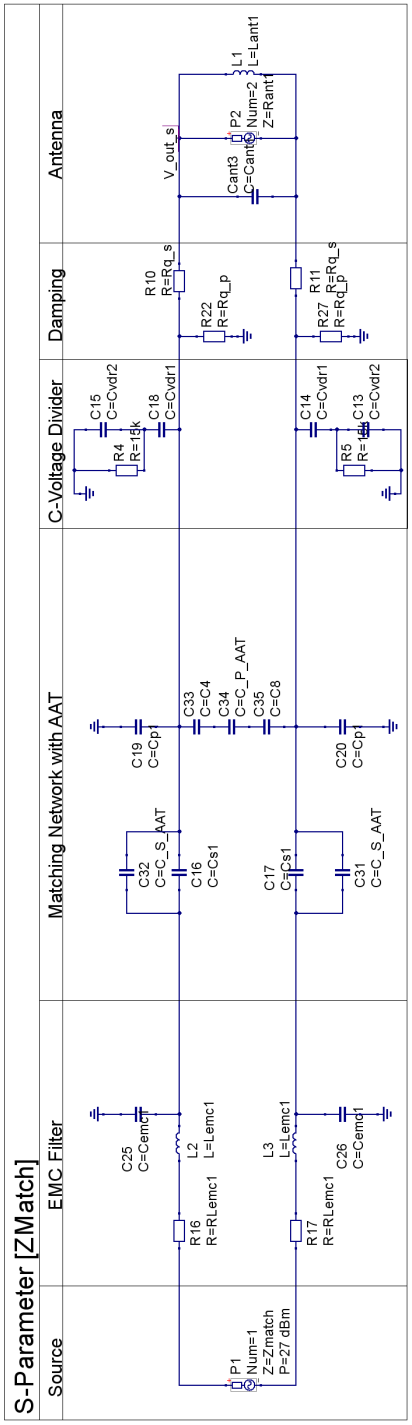


Figure 26. Transient simulation

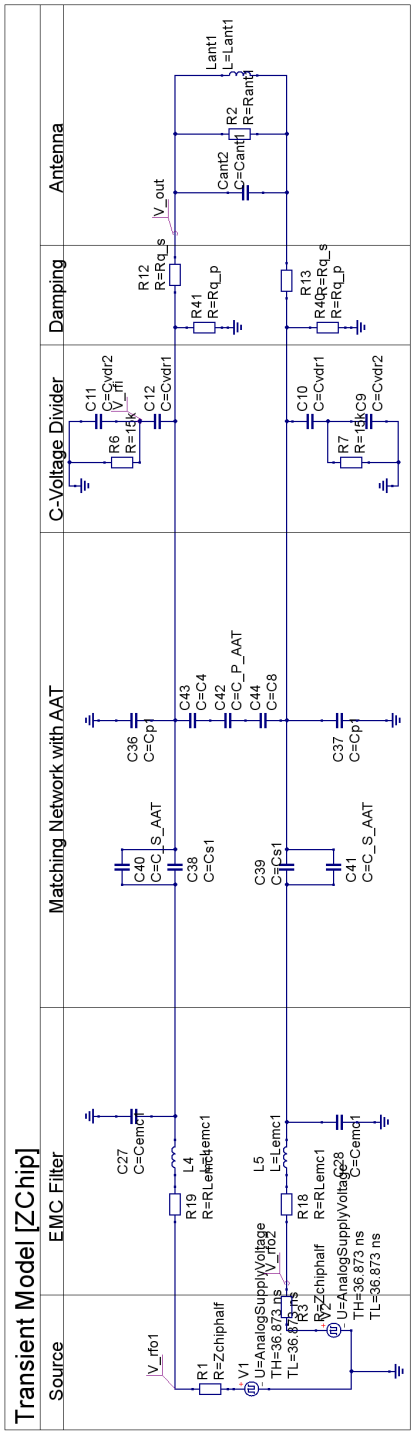
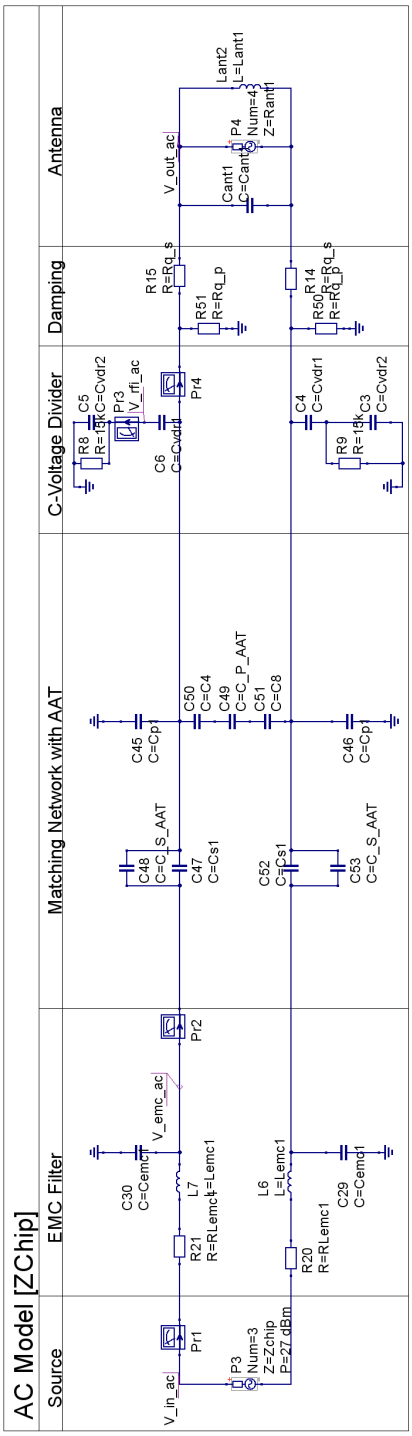


Figure 27. **AC simulation**

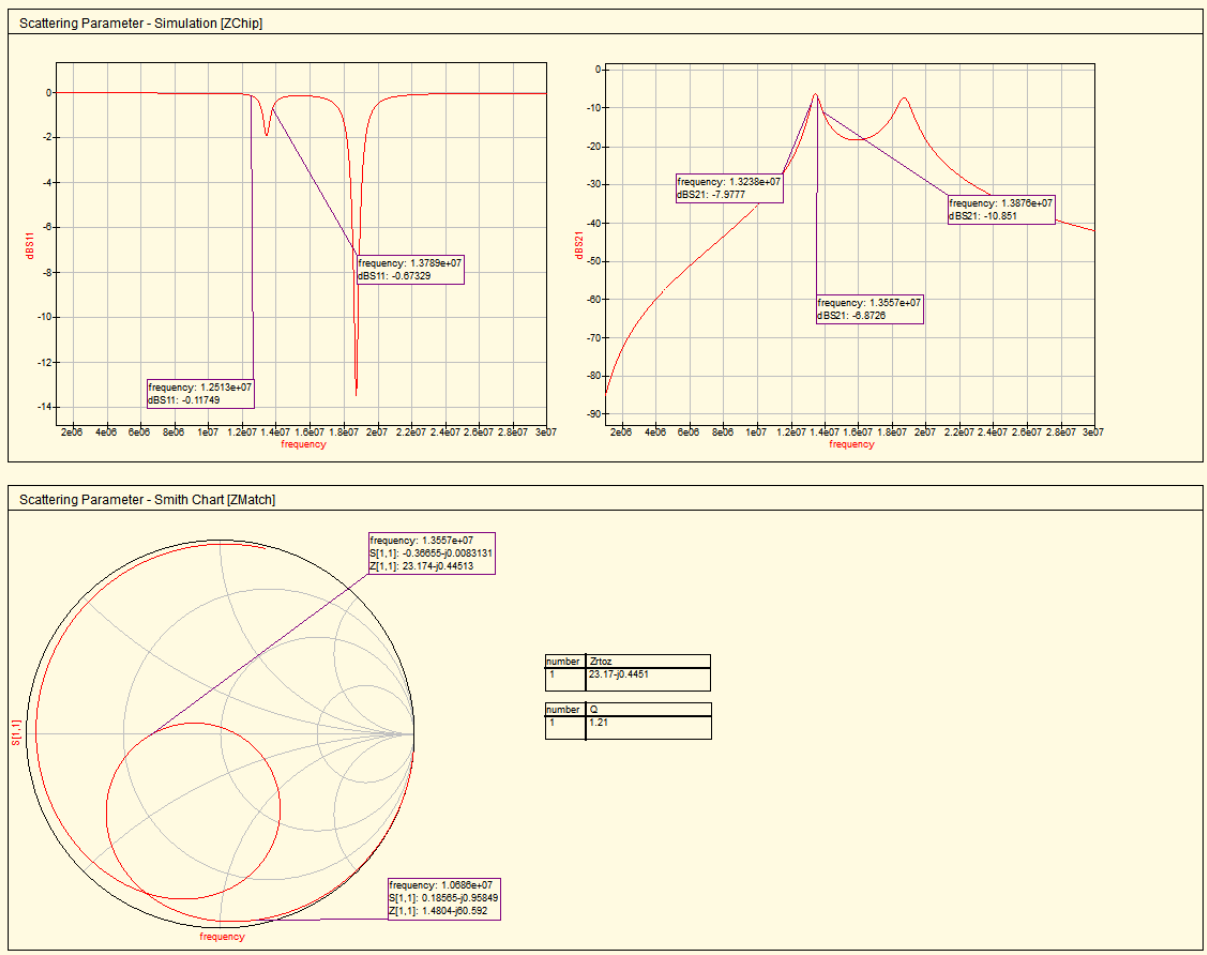


8.3.2 Results

The transfer functions dB [S11] and dB [S21] are calculated in Eqn4 (S-Parameter equations box in Figure 1). This equation uses port 3 and 4 of the AC simulation model,dB [S11] represents the reflected power on the RFOx pins.

Figure 28 shows the forward transmission, which evidences the damping over frequency. The Smith chart displays the nominal resistance of the matching network plus antenna over frequency. The Smith Chart shows the 13.56 MHz marker at (23.1 -j0.5) Ohm with the impedance curve positioned in capacitive region of the Smith chart caused by the 20 MHz EMC cutoff frequency. This reflects already an ideal matching that can be implemented as a next step on the real PCB.

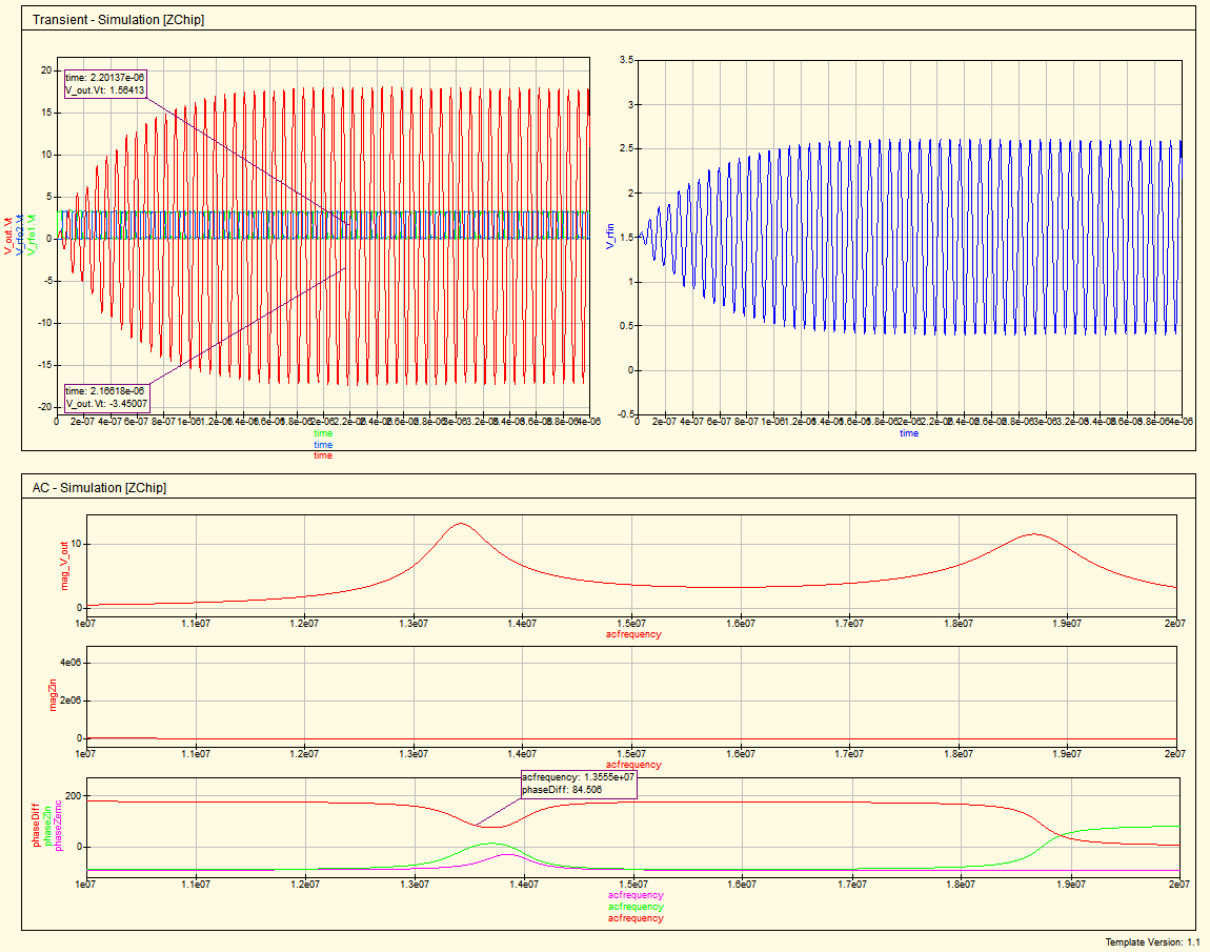
Figure 28. Simulation results of the S-parameter and the AC model



The Q factor simulation is calculated from the dB[S21] result.

As a result of the transient simulation, we can have a look at the shape of the antenna voltage and the voltage at the RFIx pins. Eqn2 (Capacitive Voltage Divider box in Figure 1) describes how the voltage at RFIx pins gets biased to the level of AGD (the analog reference voltage). The input voltage must not exceed 3 VPP. In the lower section of Figure 29 the magnitude of the antenna voltage and matching impedance as well as the phase difference (phasediff) between RF0x and RFIx pins are displayed.

Figure 29. Simulation results of the transient and of the AC model



8.4 Matching network behavior

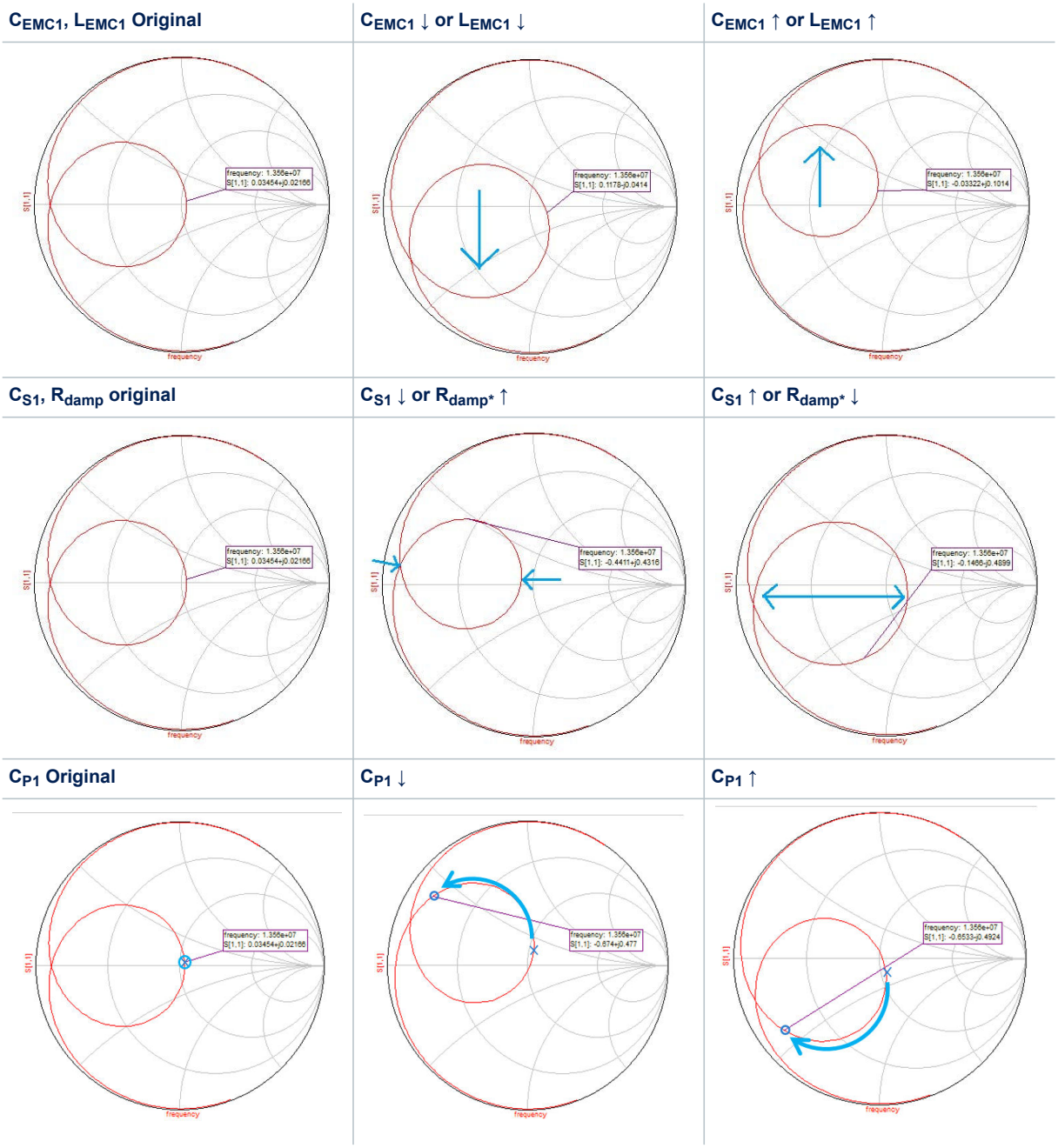
Since the simulation does not always match with the reality, some fine tuning may be needed.

Figure 30 shows how the matching network behaves when some components are changed.

Note that the behavior of Rdamp is valid only for the series resistor configuration, for the parallel damping resistor the behavior is the opposite.

When changing a component, other effects can appear. As an example, changing the serial capacitor changes the diameter of the resonance circle, but also shifts the resonance frequency, similarly as when changing the parallel capacitor.

Figure 30. Fine tuning of the matching circuit



9 Design verification and device limit checks

This section discusses the verification of the designed antenna and explains the measurement of timing parameters, Q factor, and target matching impedance.

9.1 Measurement of PCD RF analog parameters

To ensure correct operation and interoperability of a reader system, all measurements must be performed according to the required standard (for example, ISO 14443, or EMV contactless). As an example, to test against ISO 14443 contactless standard it is necessary to use the ISO reference PICC defined in ISO/IEC 10373-6.

Verifying the RF signaling parameters with an oscilloscope loop only gives a first indication on signal forms, but does not produce any meaningful or comparable measurement result.

Figure 31, Figure 32, and Figure 33 show, respectively, snapshots of Type A 106 kbit/s, Type B 106 kbit/s and FeliCa™ measurements with a reference PICC.

Figure 31. ISO 14443 Type A wave shape measurement

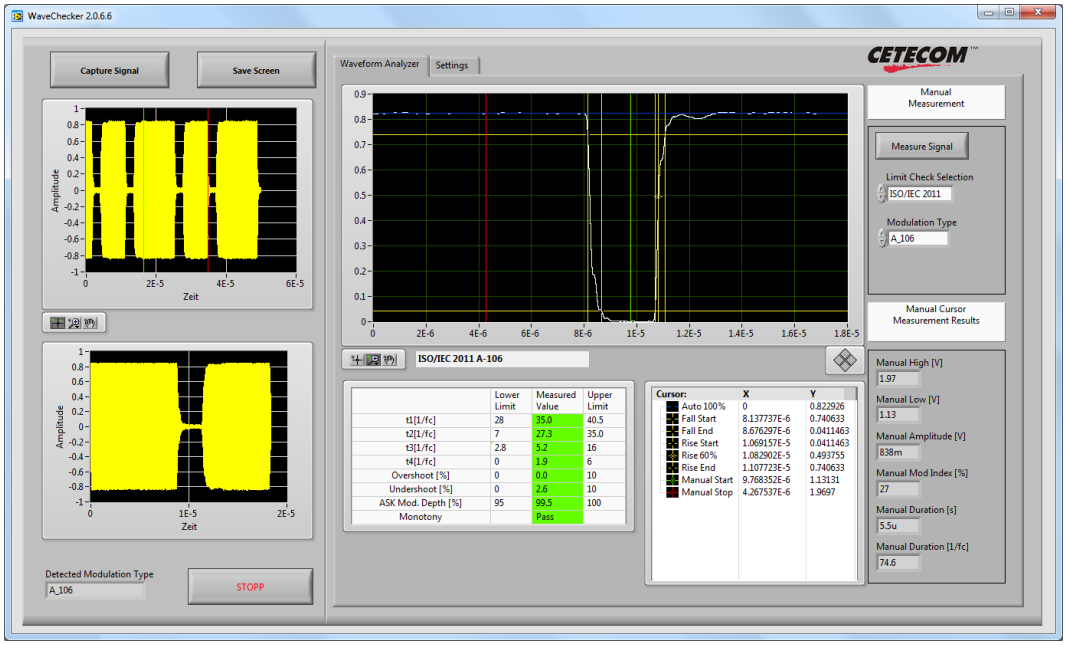


Figure 32. **ISO 14443 Type B wave shape measurement**

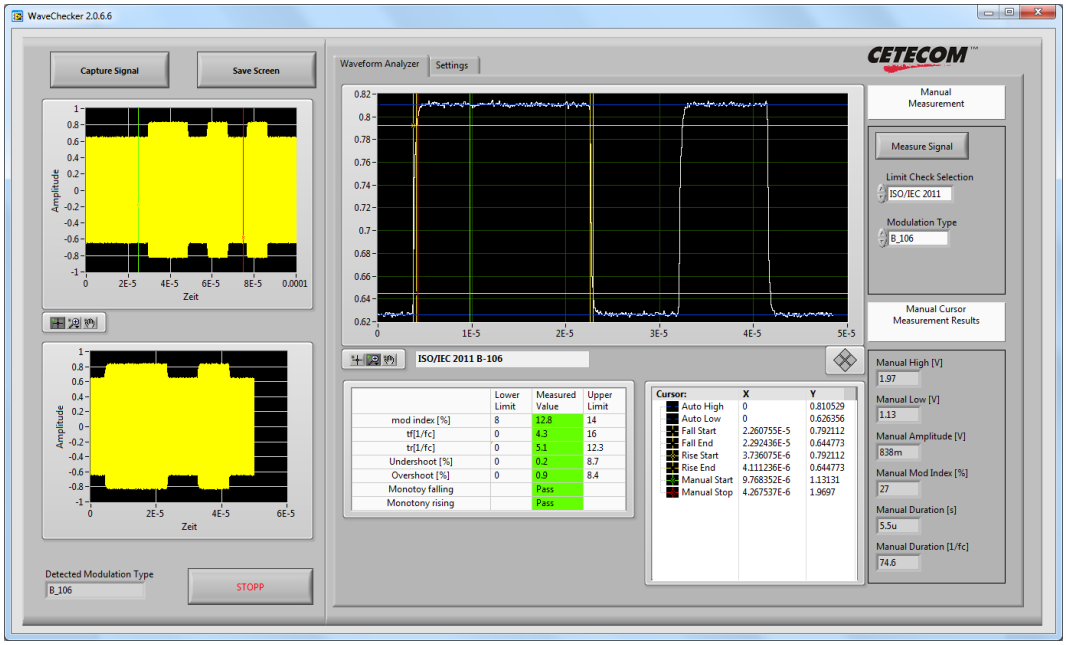
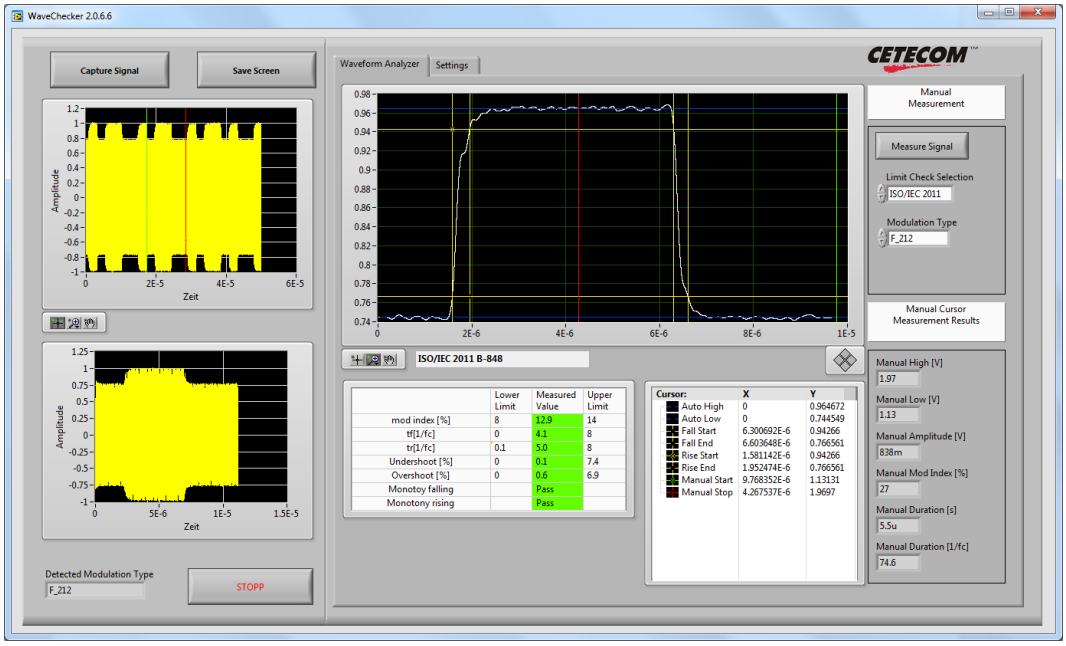


Figure 33. **FeliCa wave shape measurement**



9.2 Verification of the Q factor in the time domain

The resonance circuit envelope can be calculated (for falling and rising edges) with exponential functions:

$Q_f = 2\ \pi\ f_{work}\ [(t1 - t2) / (\ln 0.9 - \ln 0.05)]$

$Q_r = 2\ \pi\ f_{work}\ [t3 / (\ln 0.9 - \ln 0.05)]$

The overall Q is determined averaging Q_f and Q_r, that is, $Q = (Q_f + Q_r) / 2$.

9.3 Verification of the Q factor in the frequency domain

The Q factor can be measured using a vector network analyzer and an ISO10373-6

Class 1-3 calibration coil. The sequence is made up of the following steps:

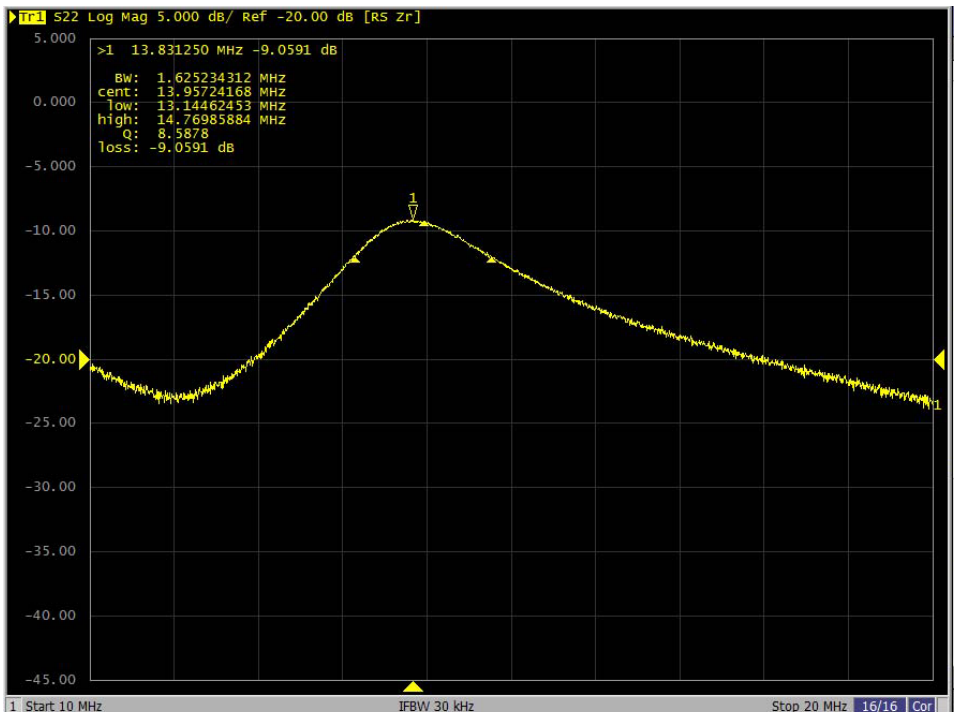
1. Calibrate the network analyzer for a frequency sweep in the 10 to 20 MHz range
2. S11 measurement must be displayed in log mag format.
3. Connect the calibration coil to the VNA.
4. “Short” calibration of the coil and conversion to “Z: Reflection”.
5. Set marker 1 and enable the bandwidth / Q factor measurement.
6. Place the PCD antenna on the measurement coil.

Note: If the reader is plugged and powered, ensure that the TX driver is set to high-Z to avoid a high power transfer to the VNA ports, which can damage the VNA.

7. Place a 2 Ω resistor between the RFO pin to simulate the chip resistance during operation.
8. Press “max search” to align the marker on the resonance frequency peak of the PCD antenna.

Figure 34 shows the results of the measurement.

Figure 34. Measurement of the Q factor with the network analyzer



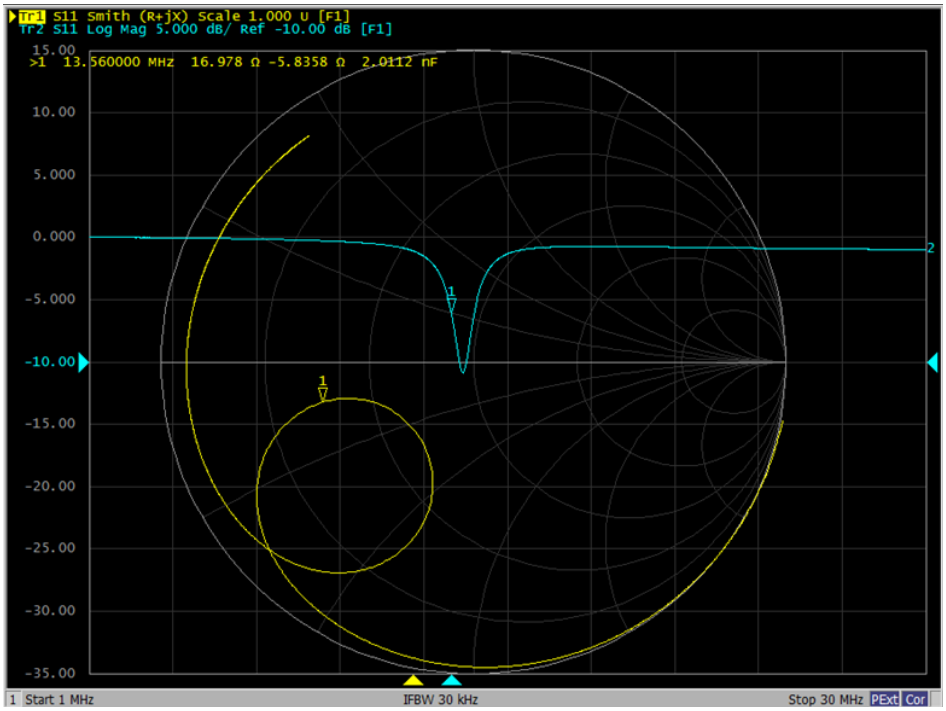
9.4 Measurement of the target matching impedance

The matching impedance of a reader system must be measured with the antenna placed in its final position. A network analyzer is required and must be configured as described in Section 7.1: Network analyzer preparation.

The target matching impedance is measured differentially between RFO1 and RFO2. The ST25R500 must not be powered during the measurement.

The Smith charts in figure Figure 35 and Figure 36 show appropriate examples of a capacitive and a symmetrical matching. The reactance at 13.56 MHz should be always capacitive (approximately from -j4 Ohm to -j8 Ohm and capacitor tolerances of 1%). The large reactance value of, for example -j6 Ω, helps in achieving the capacitive switching behavior, as shown in Section 9.6: Verification of RFO peak voltage.

Figure 35. Capacitive matching impedance measured with network analyzer



DT76341V1

Figure 36. **Symmetrical matching impedance measured with network analyzer**

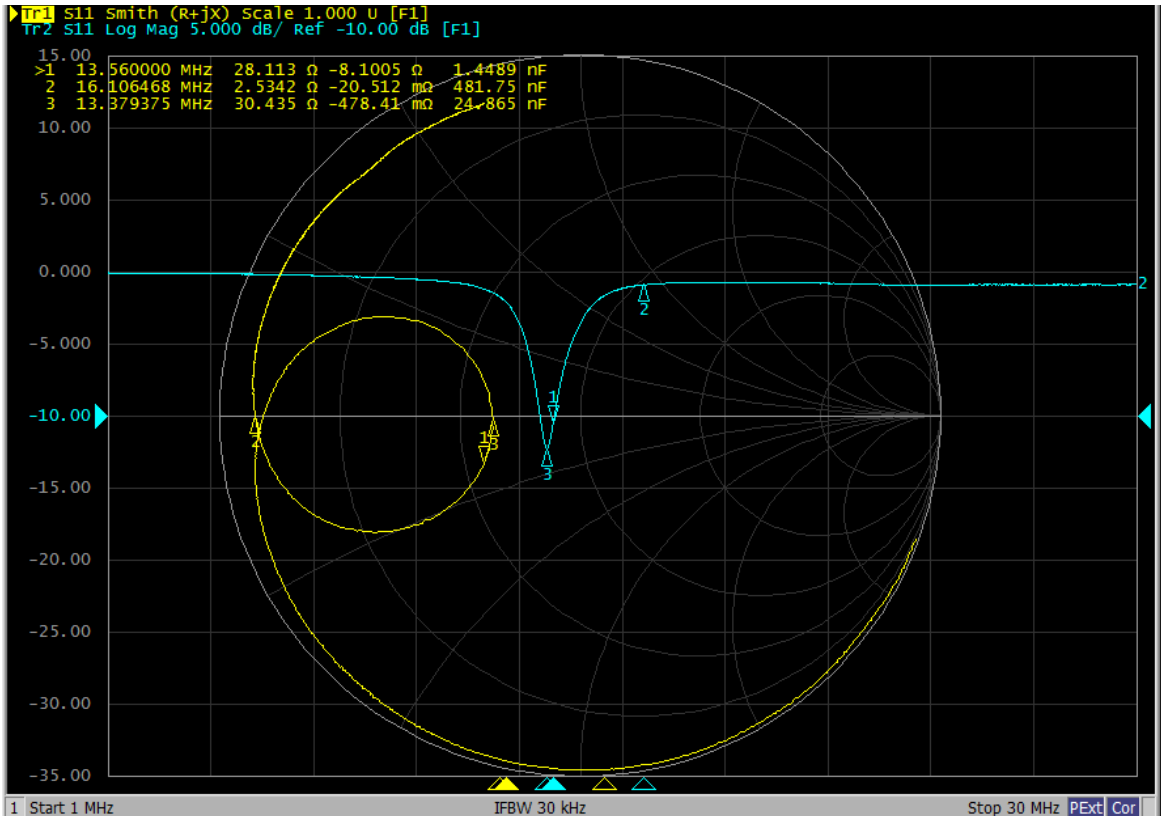


Table 4. **Matching examples**

Figure 37. **Capacitive matching 1**

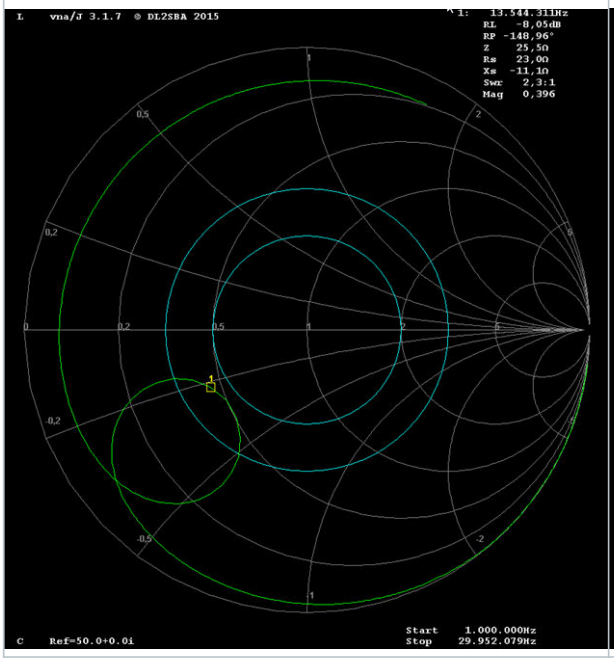


Figure 38. **Capacitive matching 2**

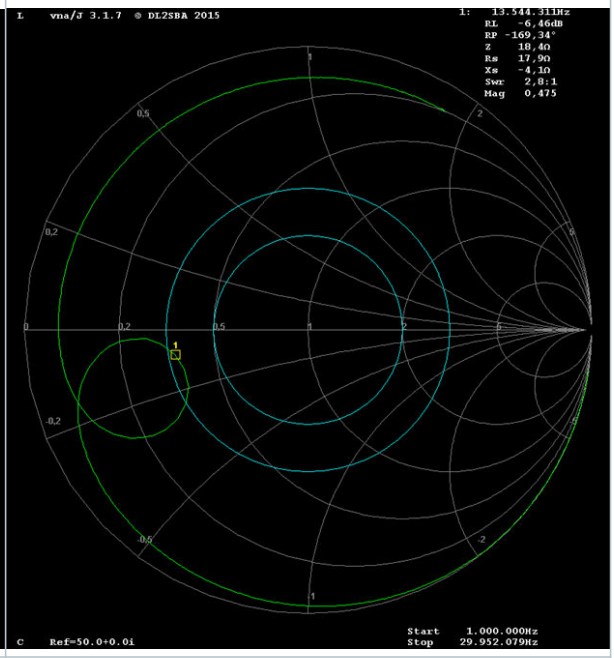


Figure 39. **Symmetric matching (not recommended !)**

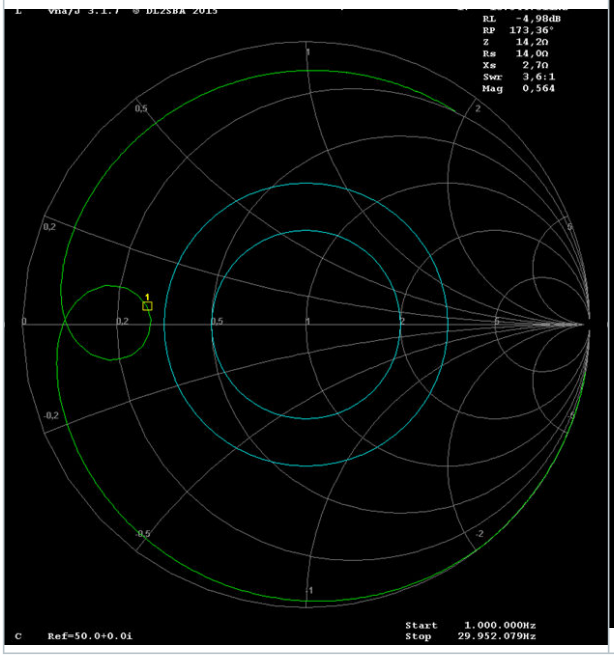
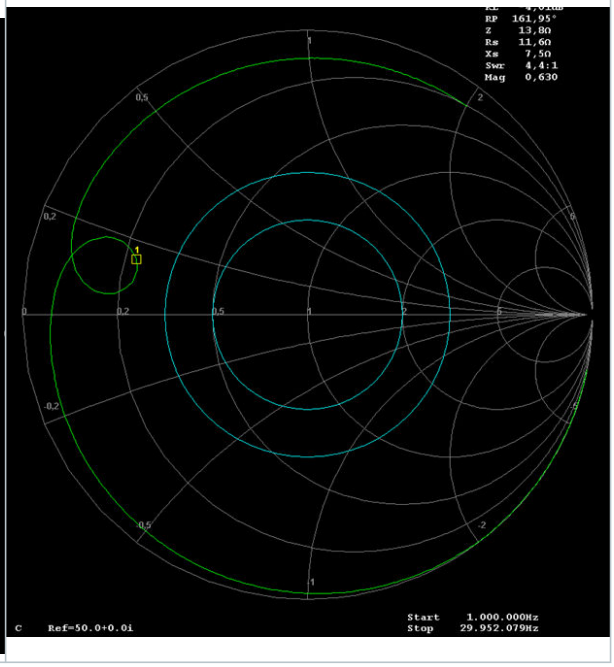


Figure 40. **Inductive matching (not recommended !)**



Caution: *ST25R300 and ST25R500 must not be used with an inductive matching.*

9.5 NFC tuning circuit calculation

The NFC tuning circuit calculator applies to ST25R readers. It provides the component values of the matching network for a given NFC antenna.

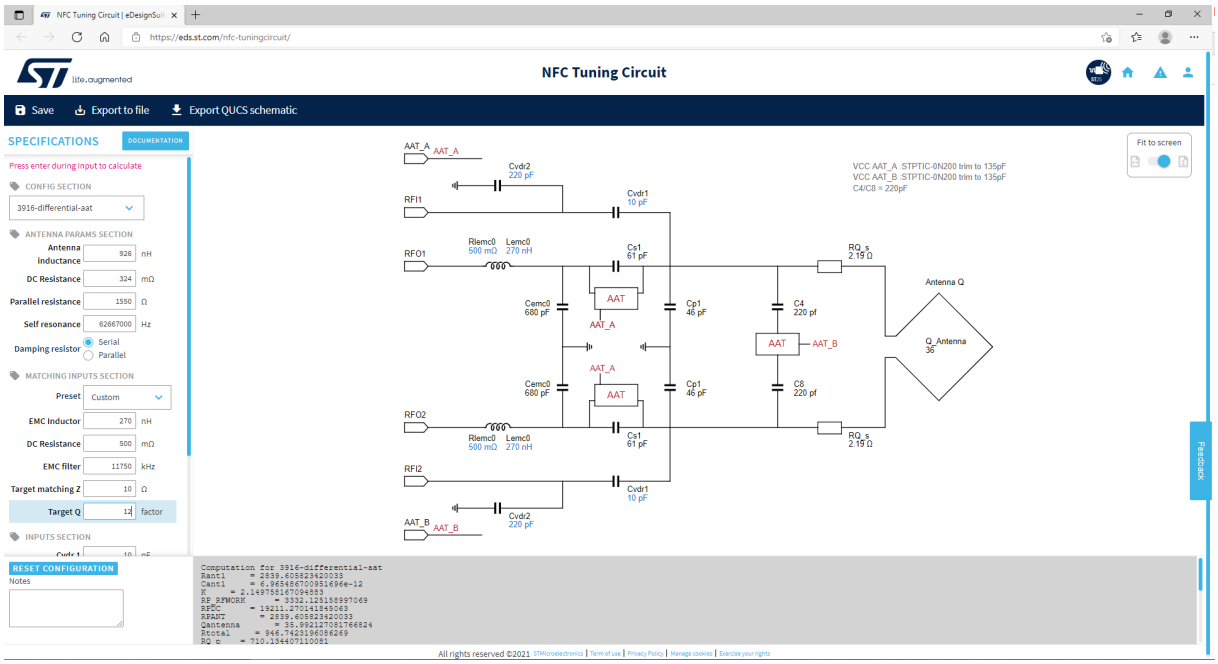
To compute the components value of the matching network located between the NFC reader and the antenna, simply enter the antenna electrical parameters and matching targets values, and select the topology of the matching network.

The tool returns the complete set of component values (including the capacitors in the AAT circuit) requested to achieve the desired design targets.

The circuit can then be exported as a Qucs file to further analyze and optimize the design.

An on-line version of the tool is available at https://eds.st.com.

Figure 41. NFC tuning circuit calculator



9.6 Verification of RFO peak voltage

By using an oscilloscope and a high impedance probe, measure the signal on both RFO1 and RFO2 to GND (see the following picture). Verify the RFO peak voltage with the oscilloscope probe in unloaded and loaded cases.

The loaded condition is met when a contactless card/device is loading and detuning the antenna. The abs (max) value or also called Vmax in some oscilloscopes must be below V_{RFO} (6.6 V) in order not to exceed the device's electrical characteristics for these pins.

Figure 42. **RFO setup**

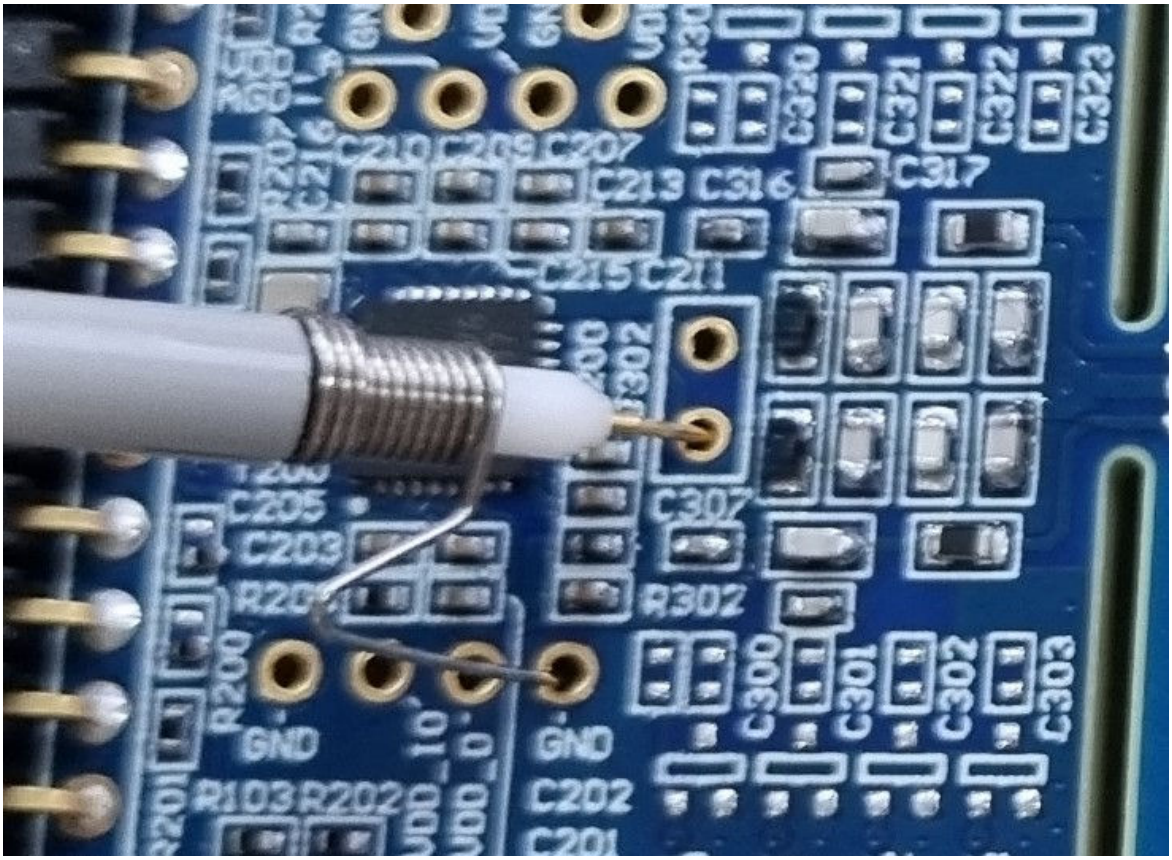


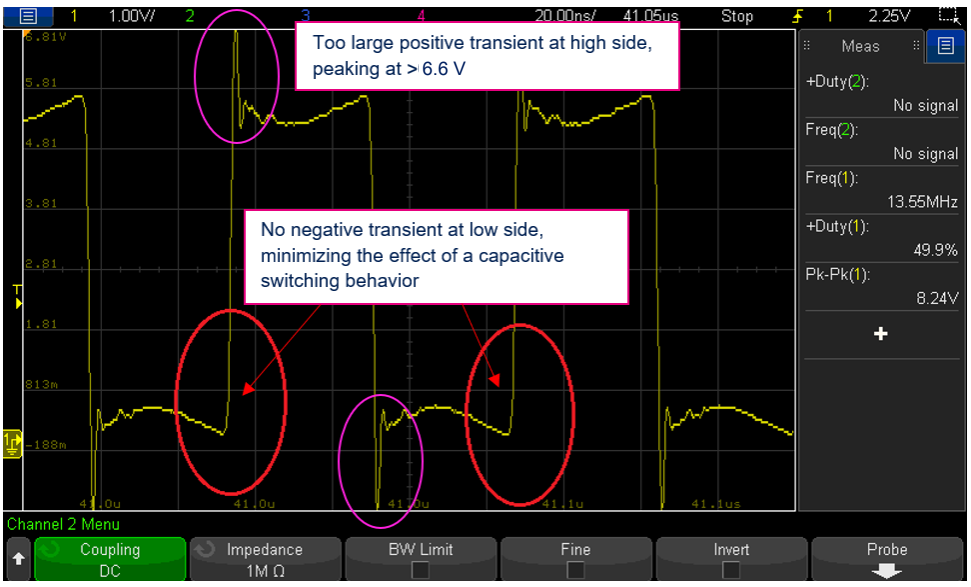
Figure 43 shows an example of a lower ohmic tuning and the ST25R500 device supplied with 5.5 V. The RFO peak signal is measured with V_{max} at 5.8 V and is thus below the maximum V_{RFO} of 6.6 V as defined in the electrical characteristics of the datasheet.

Figure 43. Example of RFO peak measurement

In case the RFO peak signal is larger than 6.6 V, countermeasures must be taken to reduce this peak value. This can be achieved by for example reducing the supply voltage, lowering the device internal regulated voltage, adapting the matching circuit and/or adding damping resistance.

A bad RFO signal example causes unwanted inductive transient behaviour in the unit and must be avoided. This is typically the outcome of matching that results in an impedance curve and a 13.56 MHz target point in the inductive region of the Smith chart.

Figure 44. RFO transients showing inductive switching behavior



9.7 Verification of the driver current

Verify the max I_{VDD_LDO} current in loaded and unloaded conditions of the antenna to not exceed the device maximum limit. This can be accomplished by simply measuring the current into the device's VDD path when the RF carrier is switched on. The RF carrier can be switched on by enabling tx_en bit in operation register.

10 Conclusion

This document describes the basic antenna design and tuning process for the ST25R500 device.

It helps the user defining the output power of the reader, specifying the components like EMC inductors used for the matching network. It also guides through the measurements of the antenna parameters, and the computation and simulation of the matching network.

The last section is dedicated to basic design verification steps, to ensure that the matching network is properly defined and operates within device limitations.

Revision history

Table 5. **Document revision history**

Date	Version	Changes
02-Apr-2024	1	Initial release.
07-Feb-2025	2	Updated: • Section Introduction • Section 3: Antenna interface stage • Section 3.1: Reader mode and output power • Section 3.2: EMC filter • Section 3.4: Capacitive voltage divider • Section 4.1: Equations • Section 5: Step by step procedure for antenna matching and finetuning • Section 6.1: Boundary conditions and simulation model • Section 6.2: Simulation results • Section 7: Antenna parameters • Section 7.3: Antenna equivalent circuit • Section 8.1: Capacitive antenna matching and EMC cutoff frequency • Section 8.3: Simulation • Section 8.3.2: Results • Section 8.4: Matching network behavior • Section 9.3: Verification of the Q factor in the frequency domain • Section 9.4: Measurement of the target matching impedance • Section 9.6: Verification of RFO peak voltage • Section 10: Conclusion Added Section 5: Step by step procedure for antenna matching and finetuning. Reoganized sections Section 6: Antenna design, Section 7: Antenna parameters and Section 8: Antenna matching.
12-Mar-2025	3	Added Figure 42. RFO setup
21-Mar-2025	4	Updated the document title and the Section Introduction.

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