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Application note

L9788 variable reluctance sensor (VRS)

Introduction

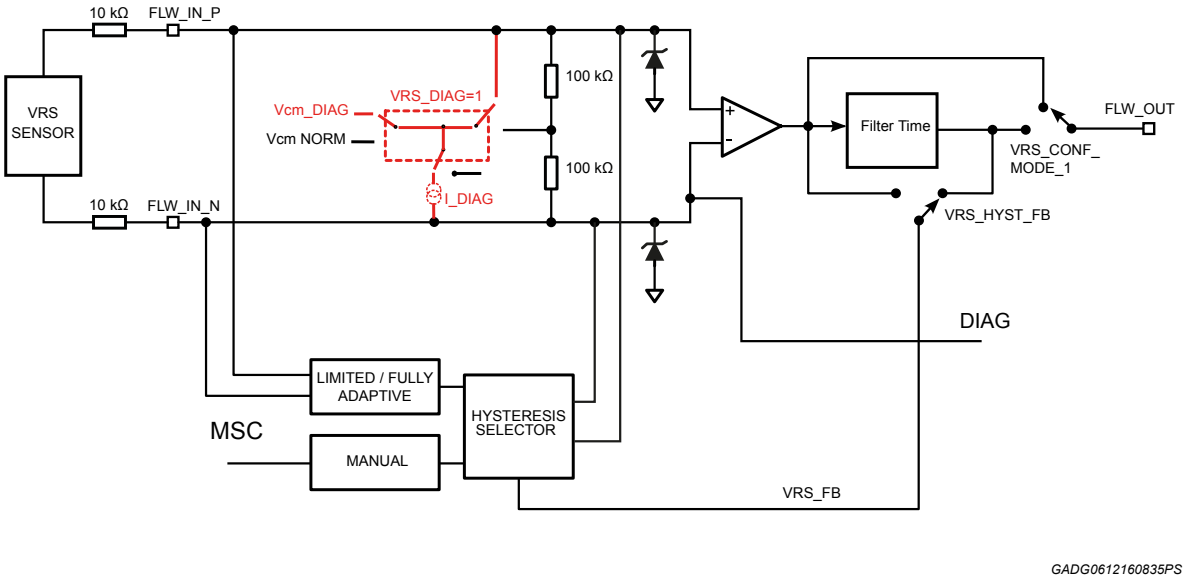
This application note is intended to integrate the information provided in the L9788 product datasheet to facilitate the usage.

1 VRS interface detailed explanation

VRS interface runs either in normal mode to convert the input differential voltage or in diagnostic mode to detect eventual short to ground, short to battery, or open condition at sensor pins.

The Figure 1 shows the main elements of the VRS interface and, in red, the internal connection in case of diagnostic mode active.

Figure 1. VRS interface block diagram



The operating mode is defined in the VRS register through the VRS_DIAG bit in CONFIG_REG8:

- If VRS_DIAG = 0, the VRS block is set in normal mode
- If VRS_DIAG = 1, the VRS diagnosis mode is activated

When the L9788 is supplied and the VRS is running, the following conditions may occur:

- If the FLW_IN_P or FLW_IN_N voltage rises over V_{clpH}, the voltage is clamped at V_{clpH}.
- If the FLW_IN_P or FLW_IN_N voltage falls below V_{clpL}, the voltage is clamped at V_{clpL}.

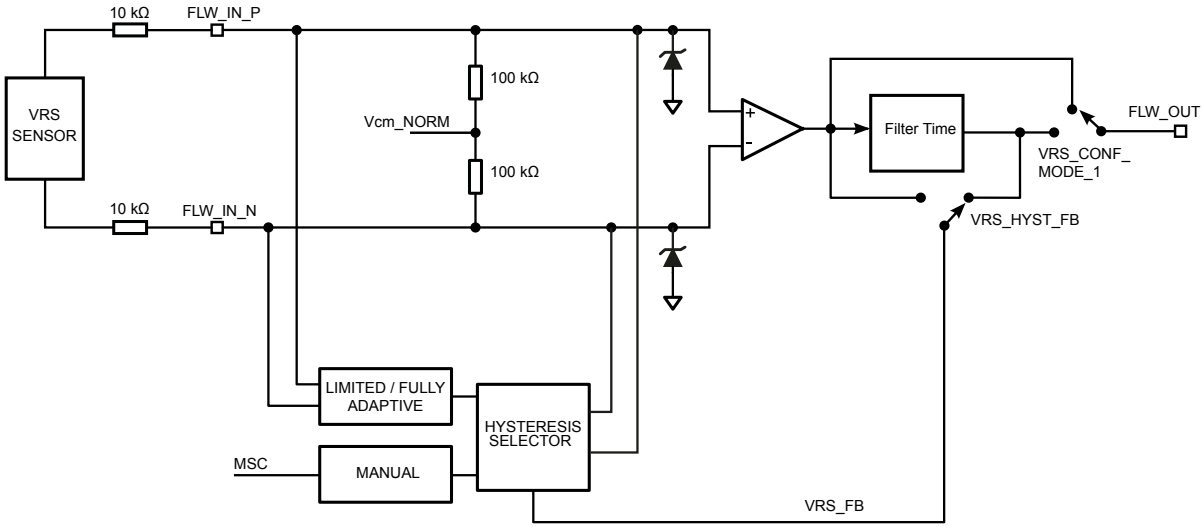
The clamp activation, either on FLW_IN_P or FLW_IN_N, is specified by design and the FLW_IN_P voltage is higher than FLW_IN_N.

2 VRS–Normal mode

The VRS normal mode is set with VRS_DIAG = 0.

In normal mode, the circuit is configured as the one reported in the Figure 2. It allows decoding the VRS signal while the flying wheel is in rotation.

Figure 2. VRS–Normal operating mode



2.1 V_{diff} steps

When “adaptive hysteresis current” is selected, the peak detector in the VRS block identifies the peak value of the input differential voltage (V_{diff} = FLW_IN_P - FLW_IN_N) and sets the hysteresis current consequently.

Instead, when the “manual hysteresis current” is selected, hysteresis current is user defined.

The hysteresis current is applied to avoid spurious commutation of the zero-crossing comparator that senses the FLW_IN_P - FLW_IN_N signal.

The hysteresis current is switched ON or OFF depending on the value of the zero-crossing comparator:

- If the output of the zero-crossing comparator is high, the hysteresis current is kept OFF
- If the output of the zero-crossing comparator is low, the hysteresis current is switched ON

This approach applies the hysteresis current only on the transition H-L of the VRS_FB signal.

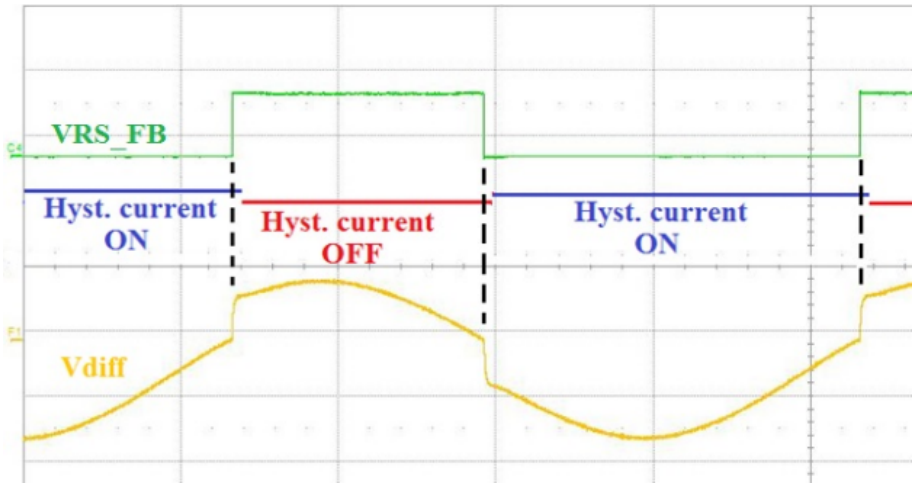
When the hysteresis current is on, it generates a voltage drop across the external resistors.

Next considerations are based on the 10 kΩ in series to FLW_IN_P and 10 kΩ FLW_IN_N pins.

The turning ON or OFF of the hysteresis current determines the steps of the input differential signal (V_{diff} = FLW_IN_P - FLW_IN_N) in correspondence of each zero-crossing.

This is visible in the Figure 3:

Figure 3. **VRS–Steps in input differential signal**



- If the hysteresis current is small, steps in V_{diff} (= FLW_IN_P - FLW_IN_N) are small
- If the hysteresis current is large, steps in V_{diff} (= FLW_IN_P - FLW_IN_N) are large

The VRS block senses the input differential voltage (V_{diff} = FLW_IN_P - FLW_IN_N) and FLW_OUT toggles on the V_{diff} zero-crossing.

The output of the zero-crossing comparator can be further processed by a filtering circuit or directly routed to FLW_OUT.

2.2 VRS clamp

Sensor signal range can be very wide, up to ±200 V. These signals reported to the L9788 VRS input pins, shall be limited within the specified voltage AMR to prevent damage on the internal receiver structure. For these reasons VRS inputs are internally clamped in the range [V_{clpH}–V_{clpL}]; current has to be externally limited as depicted in the specification. Sensor input pins have the common-mode VCM input, internally set for proper operation.

This allows the input differential signal to be processed that is V_{diff} = FLW_IN_P - FLW_IN_N.

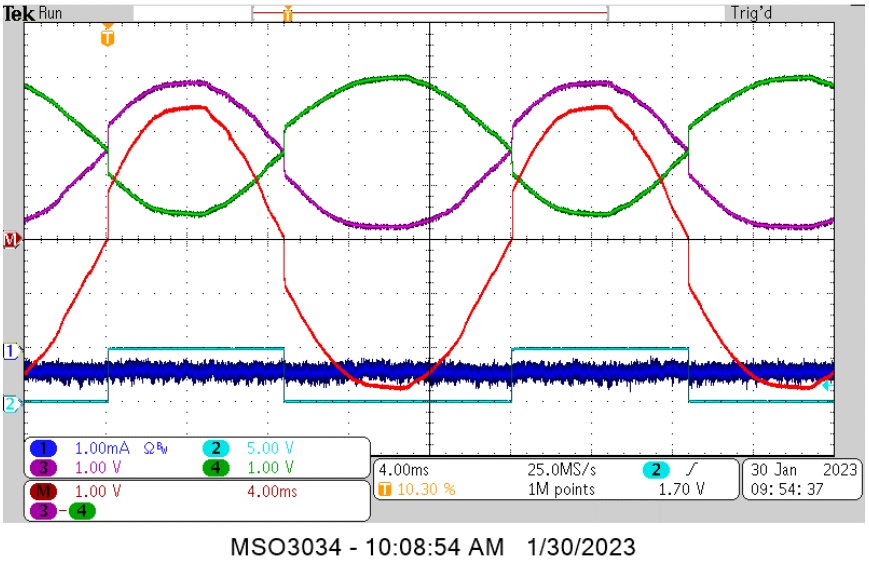
Current flowing through FLW_IN_P - FLW_IN_N has to be limited inside the absolute values, as reported in the specification. When the amplitude of the input signals overcomes the clamp values (FLW_IN_x < V_{clpL} and FLW_IN_y > V_{clpH}), FLW_IN_P, FLW_IN_N and VCM reduce their value, refer to the Figure 4, Figure 5, and Figure 6.

The VRS block still senses the input differential signal and sets FLW_OUT accordingly.

As an example:

- VRS_MODE[1:0] = 00 (manual hysteresis current no filter time)
- VRS_HYST[2:0] = 101 (high hysteresis current)

Figure 4. **VRS–Manual HI5_small input signal**

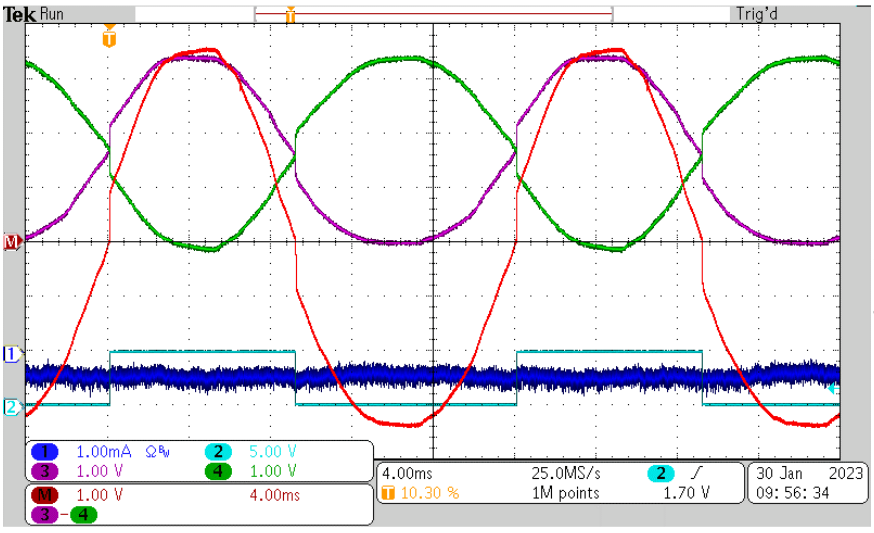


1: I_FLW_IN_P
2: FLW_OUT
3: FLW_IN_P
4: FLW_IN_N
M: Vdiff = FLW_IN_P - FLW_IN_N

Note: Evidence of wide steps on V_{diff} 0 V crossing due to the high hysteresis current set and no clamps in FLW_IN_x.

Increasing the amplitude of the VRS sensor, cuts on the positive waveform of FLW_IN_P and V_{diff} (refer to Figure 5) are evident, as the steps on V_{diff} 0 V crossing.

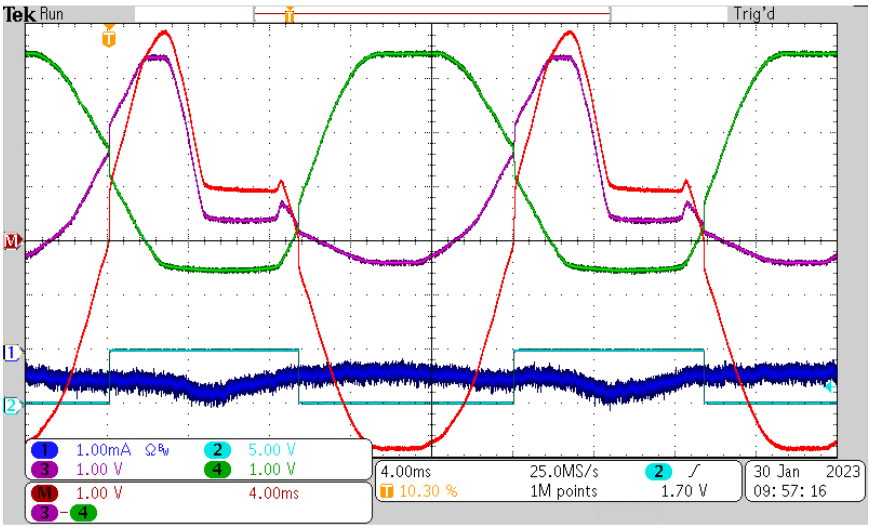
Figure 5. **VRS–Manual HI5, FLW_IN_P at clampH**



1: I_FLW_IN_P
2: FLW_OUT
3: FLW_IN_P
4: FLW_IN_N
M: Vdiff = FLW_IN_P - FLW_IN_N

Increasing again the amplitude of the VRS sensor, positive FLW_IN_P and V_{diff} signals are reduced. Negative FLW_IN_N is cut at clampL and V_{diff} is cut consequently. This is due to the current in the ESD network limited to the AMR shown in the specification (±200 mA, refer to Figure 5), and the VCM is reduced accordingly.

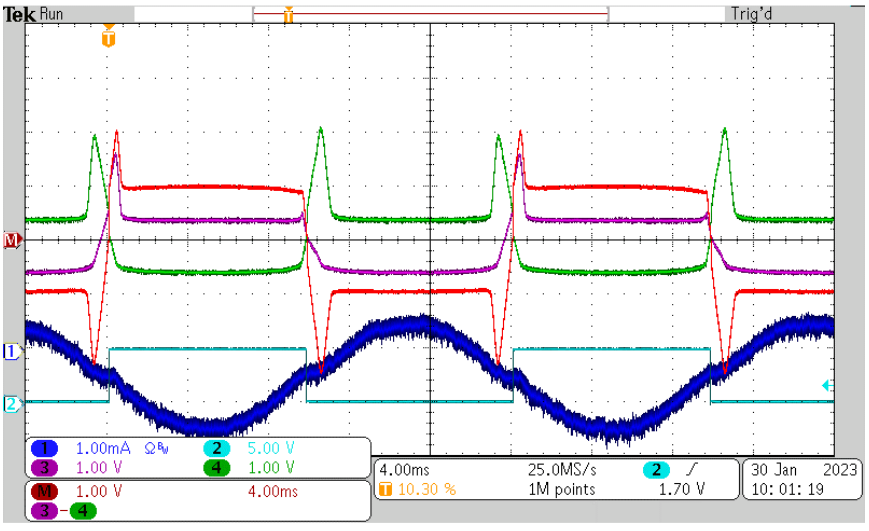
Figure 6. **VRS–Manual HI5 and FLW_IN_N at clampL**



1: I_FLW_IN_P
2: FLW_OUT
3: FLW_IN_P
4: FLW_IN_N
M: Vdiff = FLW_IN_P - FLW_IN_N

A further increase of the VRS amplitude signal, determines the reduction of FLW_IN_P, FLW_IN_N, and VCM, due to the current in the ESD network, refer to Figure 7

Figure 7. **VRS–Manual HI5, fading of FLW_IN_P, FLW_IN_N, and VCM**



1: I_FLW_IN_P
2: FLW_OUT
3: FLW_IN_P
4: FLW_IN_N
M: Vdiff = FLW_IN_P - FLW_IN_N

In all the cases mentioned above, FLW_OUT follows the input differential voltage (V_{diff} = FLW_IN_P - FLW_IN_N) as expected, so the VRS signal is properly processed.

2.3 VRS normal mode configurations

The L9788 integrates two main configurable modes: VRS_A and VRS_B. These modes are selected in the VRS register, VRS_MODE_SEL bit in CONFIG_REG2.

Once VRS_A (VRS_MODE_SEL = 1) or VRS_B (VRS_MODE_SEL = 0) has been configured, the hysteresis and filtering strategy are defined through the VRS_MODE[1:0] bit in the same CONFIG_REG8 register:

- VRS_MODE[1] defines a filtering function (OFF/ON and if ON, its time value)
- VRS_MODE[0] defines the hysteresis (manual or adaptive)

The Table 1 and Table 2 summarize the parameters of the VRS_A and VRS_B modes; the next paragraphs detail the two configurations.

Table 1. VRS_A hysteresis and filter time definition

VRS_MODE_SEL (A config.)	VRS_MODE[1:0]	Filter		Hysteresis	
1	00	OFF	0 µs	Manual	Refer to: VRS_A manual hysteresis
1	01	OFF	0 µs	Full adaptive	Refer to: VRS_A fully adaptive hysteresis
1	10	ON	T(n-1)/32	Manual	Refer to: VRS_A manual hysteresis, VRS_A adaptive filter time
1	11	ON	T(n-1)/32	Full adaptive	Refer to: VRS_A fully adaptive hysteresis, VRS_A adaptive filter time

Table 2. VRS_B hysteresis and filter time definition

VRS_MODE_SEL (B config.)	VRS_MODE[1:0]	Filter		Hysteresis	
0	00	OFF	0 µs	Manual	Refer to: VRS_B manual hysteresis
0	01	OFF	0 µs	Limited adaptive	Refer to: VRS_B limited adaptive hysteresis
0	10	ON	4 µs	Manual	Refer to: VRS_B manual hysteresis, VRS_B fixed filter time
0	11	ON	4 µs	Limited adaptive	Refer to: VRS_B limited adaptive hysteresis, VRS_B fixed filter time

In case a change of the VRS_MODE_SEL bit within the normal operating mode occurs (1 → 0 or 0 → 1) with hysteresis current active, this leads to the change of the hysteresis (to HI1 or HI3 –default values–, according to the new selection programmed) not synchronized with any VRS_FB zero-crossing.

2.4 VRS_A manual hysteresis

To set the manual hysteresis on VRS_A configuration, bit VRS_MODE[0] has to be configured at ‘0’. The hysteresis value is manually set through the VRS_HYST[2:0] of CONFIG_REG8 according to Table 3. Such hysteresis is fixed until a new programming frame occurs.

The default hysteresis current after exiting reset is HI3.

A new current value set through the MSC interface is updated during the HYST CURRENT OFF phase that means that the output comparator is high.

Table 3. VRS_A hysteresis values

Hysteresis current [HI]	Value			Unit	Correspondent value on 20 kΩ ext. resistor	Unit
	Min.	Typ.	Max.			
HI1	3	5	7	µA	100	mV
HI2	7.5	10	13.5	µA	200	mV
HI3	13	17	23	µA	347	mV
HI4	23	32	40	µA	644	mV
HI5	35	51	60	µA	1020	mV
No hyst.						

2.5 VRS_A fully adaptive hysteresis

To set the adaptive hysteresis on the VRS_A configuration, the VRS_MODE[0] bit has to be set to ‘1’.

In this configuration, VRS input differential signal is fed into a peak detector circuit and then it is quantized on 5 different voltage levels, based on 4 PVi thresholds (see Table 4). The default hysteresis current after exiting reset is HI3.

Table 4. Peak voltage value ranges

Peak voltage [PVi]	Min.	Typ.	Max.	Unit
PV1	600	930	1300	mV
PV2	1200	1600	1950	mV
PV3	2000	2300	2650	mV
PV4	2600	3000	3300	mV

The quantized output is sent to a logic block (hysteresis selection Table) that chooses the proper hysteresis value HIi depending on the input peak voltage (PVi), see Table 5.

Table 5. Peak voltage range correspondence with hysteresis selection

Input peak voltage range	Selected hysteresis (HIi)
0–PV1	HI1
PV1–PV2	HI2
PV2–PV3	HI3
PV3–PV4	HI4
> PV4	HI5

Peak detector and hysteresis selection table circuits are enabled by the VRS_FB signal according to the HYS_FB_SEL bit in the CONFIG_REG8 register.

This bit defines if the feedback signal is before (HYS_FB_SEL=0) or after (HYS_FB_SEL=1) the filter time.

VRS input differential voltage is continuously acquired.

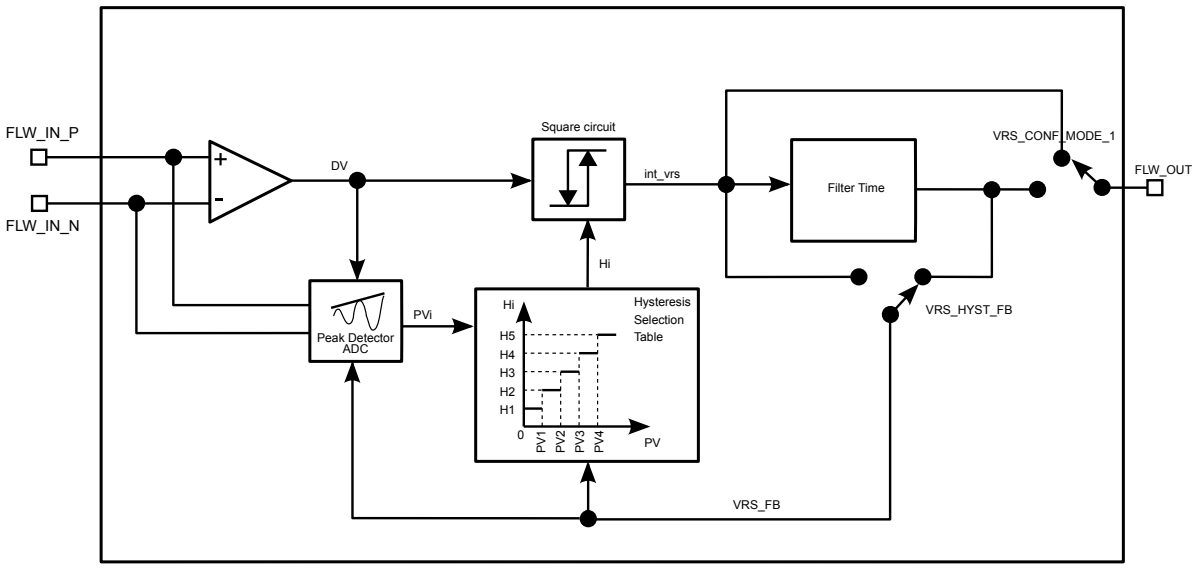
During the time frame with the VRS_FB signal asserted (that corresponds to the hysteresis current HI OFF), the maximum value of V_{diff} is reached.

This maximum value of V_{diff} is latched through the peak detector and the peak detector defines the appropriate hysteresis current HIi.

When VRS_FB falls down crossing 0V, the hysteresis current is turned ON immediately or with a delay depending on the MASK_TIME or FILTER_TIME selection.

Based on the hysteresis current, the signal is processed by a squaring circuit, which processes the output signal of the comparator, see Figure 8.

Figure 8. **VRS_A fully adaptive hysteresis**



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2.6 VRS_A adaptive filter time

In VRS_A mode, it is possible to enable the filter time on the output of the zero-crossing comparator through the bit VRS_MODE[1] of CONFIG_REG8.

Once enabled, the most suitable internal filter based on the input signal frequency is determined.

According to the previous period of VRS, the filter time value is updated as per the following:

$$Tfilter_{(n)} = \frac{Tperiod_{(n-1)}}{32}$$

If the value of the previous period is longer than 128 µs, the filter time would be saturated at 4 µs fixed value. After reset T_{filter} = 200 µs (typ.)

Through the EN_FALLING_FILT bit in the CONFIG_REG8 register, it is possible to configure two different strategies for the filtering algorithm:

1. VRS_OUT rising edge: the transition depends on the hysteresis crossing of the differential signal V_{diff}; VRS output is set if V_{diff} remains asserted and stable for a period longer than T_{filter}.
2. VRS OUT falling edge: the transition depends on the zero-crossing of the differential signal V_{diff}:
   - EN_FALLING_FILT = 1: VRS_OUT is deasserted when the differential signal V_{diff} is low and remains stable for at least T_{filter} time (see Figure 9).
   - EN_FALLING_FILT = 0: VRS_OUT is deasserted at the first zero-crossing transition of the differential signal and the next eventual commutations are ignored for T_{filter} time (see Figure 10).

Figure 9. **EN_FALLING_FILT = 1**

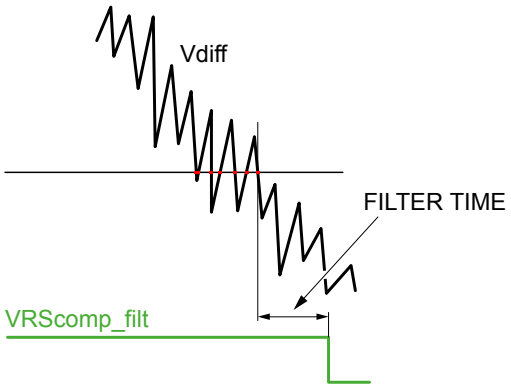

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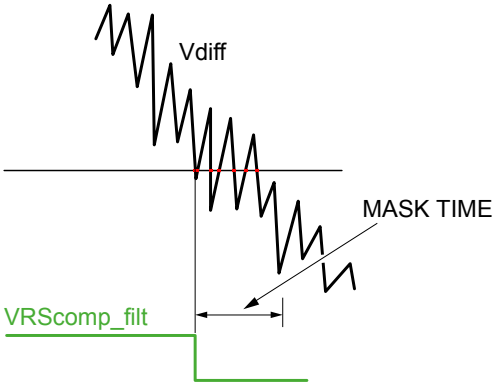
Figure 10. **EN_FALLING_FILT = 0**



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2.7 VRS_B manual hysteresis

To define the manual hysteresis on VRS_B configuration, bit VRS_MODE [0] is set to ‘0’. Hysteresis value is manually selected through VRS_HYST [2:0] of CONFIG_REG8 according to Table 6. Such hysteresis is fixed until a new MSC programming occurs.

Table 6. **VRS_B hysteresis values**

Hysteresis current [HI]	Value			Unit	Correspondent value on 20 kΩ ext. resistor	Unit
	Min.	Typ.	Max.			
HI1	3	5	7	µA	100	mV
HI2	7.5	10	13.5	µA	200	mV
HI3	13	17	23	µA	347	mV
HI4	23	32	40	µA	644	mV
HI5	35	51	60	µA	1020	mV
No hyst.						

Once a new value is defined, a new hysteresis threshold is applied after the second VRS_FB H-L transition and until the next rising edge of the VRS input differential voltage occurs.

2.8 VRS_B limited adaptive hysteresis

To set the limited adaptive hysteresis on the VRS_B configuration, bit VRS_MODE [0] has to be configured at '1'. In this mode, the user programs a hysteresis threshold through the VRS_HYST [2:0] bit in the VRS register and the internal logic selects a hysteresis based on the input signal peak value: the maximum of these two values is actually applied.

Once a new value is defined, a new hysteresis threshold is applied after the second VRS_FB H-L transition and until the next rising edge of the VRS input differential voltage occurs.

2.9 VRS_B fixed filter time

In the VRS_B configuration, it is possible to enable the filter time on the output of the zero-crossing comparator through the bit VRS_MODE[1] of the VRS register. This configuration allows defining the internal filter time at a fixed value of 4 µs, active on both rising and falling edges of VRS output.

As per the VRS_A architecture, EN_FALLING_FILT allows configuring the same two different strategies for the filtering algorithm.

3 VRS–Diagnostic mode

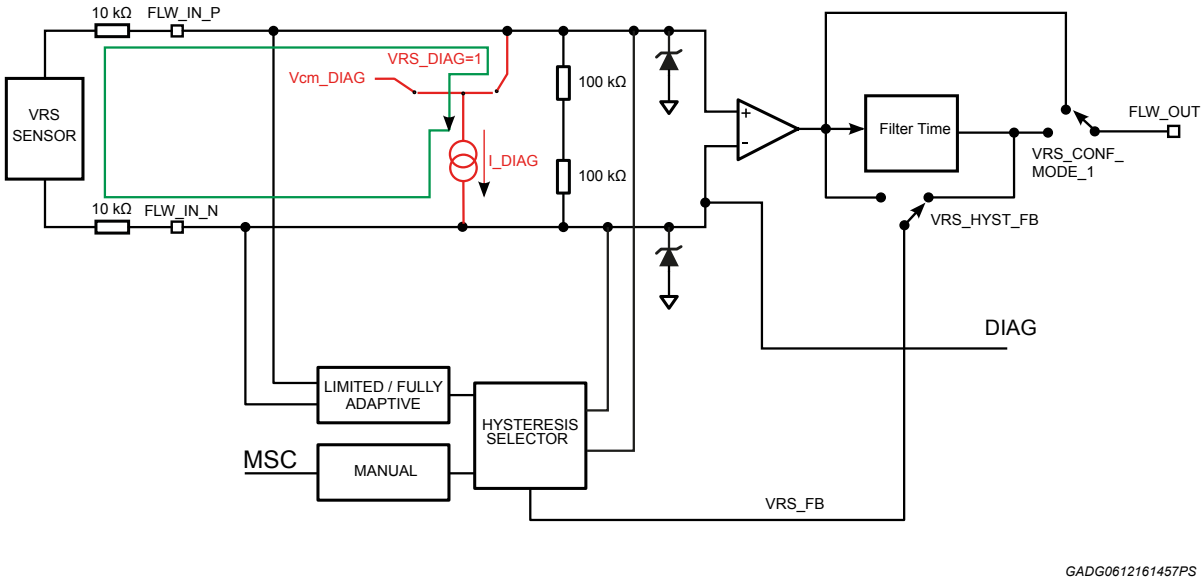
The diagnostic mode is selected through VRS_DIAG = ‘1’ in CONFIG_REG8. This mode provides feedback to detect faulty conditions either on FLW_IN_P or FLW_IN_N.

To be noted that diagnostic results are not reliable while the flying wheel is rotating.

If a fault is detected in DIAG mode, the VRS correct functionality is not ensured. Fault bit VRS_DIAG of the VRS register is consequently set.

The Figure 11 shows the circuit used in diagnostic mode. When VRS diagnostic mode is activated, FLW_IN_P is fixed at Vcm_DIAG and I_DIAG current generator is enabled, so the current path is the one in green.

Figure 11. VRS block diagram–Diagnostic operating mode–Current path



4 Application circuit

Sensor sketch and parameters are reported in the Figure 12.

Figure 12. VRS sensor sketch

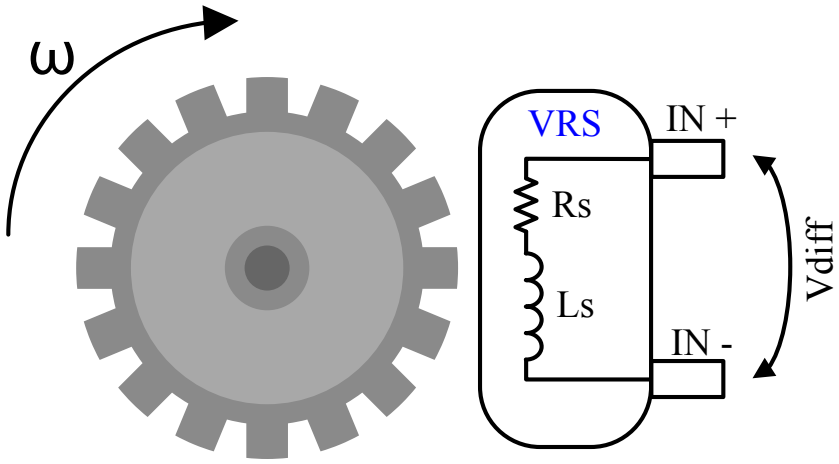


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Table 7. VRS sensor parameters

Symbol	Parameter	Min.	Typ.	Max.	Unit
R_s	Sensor resistance	300	600	1000	Ω
L_s	Sensor inductor	-	250		mH
V_{diff}	Sensor output voltage	-200		+200	V
T_{out}	Output period	100		5000	µs

The interface handles signals coming from magnetic pick-up sensors. The interface feeds the digital signal to the microcontroller that extracts flying wheel rotational position, angular speed and acceleration.

Revision history

Table 8. **Document revision history**

Date	Revision	Changes
19-Dec-2023	1	Initial release.

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