How the STDES-ISV002V1 augments the STEVAL-ASTRA1B with energy harvesting features

Introduction

The STDES-ISV002V1 is both a standalone design and a STEVAL-ASTRA1B expansion board built around the ultralow power energy harvester and battery charger SPV1050 device. The design leverages all the SPV1050 based features enhanced by an external photovoltaic panel monitoring circuit. This allows its use as a solar energy harvester with advanced energy detection and management features, making the user aware of the available light in the environment and the battery charging status.

The STDES-ISV002V1 is designed to be housed inside the STEVAL-ASTRA1B plastic case; the electrical connections between the two boards occur through a 34-pin expansion connector.

The two photovoltaic panels can also be housed in a 3D printed add-on that can be docked to the STEVAL-ASTRA1B plastic case. Two 3D printed add-on designs are available: one of them provides buttonholes that allow secure fixing by means of cable ties. The other one is equipped with a 1/4-inch photographic nut which makes the design compatible with all photographic support and anchoring equipment.

This document explains the STDES-ISV002V1 technical details and how it can be used to enhance the STEVAL-ASTRA1B energy management capabilities. Refer to the STDES-ISV002V1 data brief and the SPV1050 datasheet for features and performance details regarding the board and the featured device, respectively.

1 Acronyms

Table 1. **List of used acronyms**

Acronym	Description
PV	Photovoltaic
EOC	End of charge
UVLO	Undervoltage lockout
BG	Bandgap
UVP	Undervoltage protection
EOCHYS	End of charge hysteresis
$UVLO_L$	Undervoltage lockout deactivation threshold: low
MPPT	Maximum power point tracking
V_{OC}	Open circuit voltage
V_{MP}	Voltage at maximum power point
LDO	Low-dropout regulator
RS	Range selector
AM	Air Mass coefficient

2 STDES-ISV002V1

2.1 Hardware

The STDES-ISV002V1 block diagram (Figure 1) is made of two main subcircuits: the first revolves around the SPV1050 device, the second one is a PV V_{OC} measurement system. The block diagram consists of a circuit for selecting the supply voltage and a 34-pin expansion connector. The detailed schematic is in Schematics.

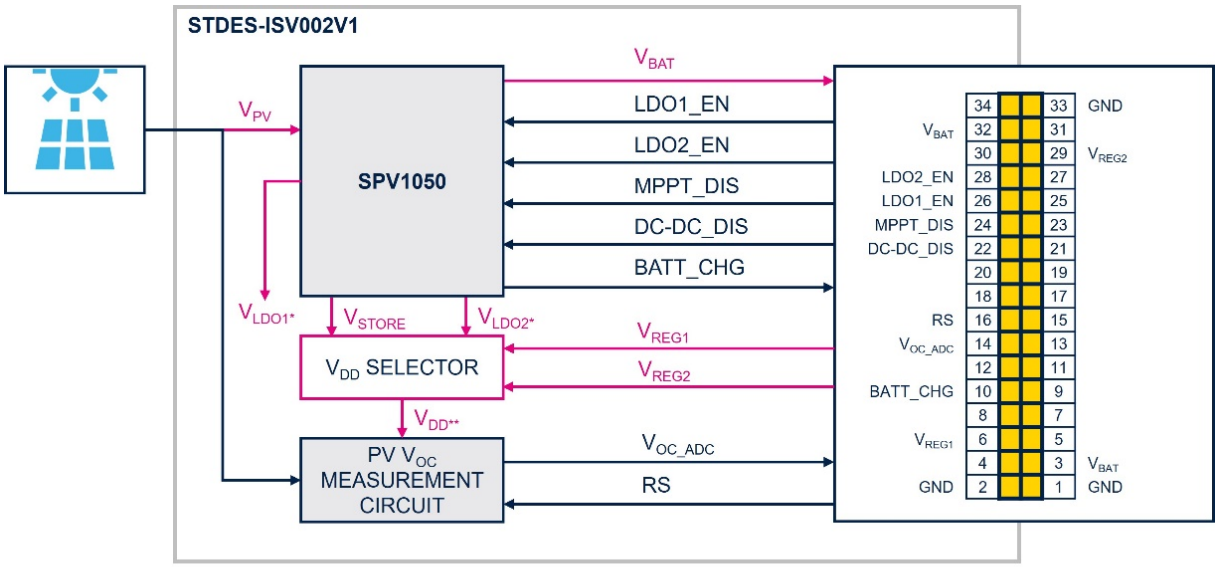
2.1.1 SPV1050

The SPV1050 is an ultralow power and high efficiency energy harvester and battery charger that implements the MPPT function and integrates all the switching elements to address the chosen boost converter configuration.

The SPV1050 device allows charging the battery by monitoring the end-of-charge (EOC) and the minimum battery voltage (UVLO) to avoid overdischarge and to preserve battery life.

The EOC and UVLO thresholds are through a resistive chain made up of the resistors R4, R5, R6.

Figure 1. STDES-ISV002V1 block diagram



(*) V_{LDO1} = 1.8V (available but not used in the default configuration) – V_{LDO2} = 3.3V
(**) By default V_{DD} = V_{LDO2}

The design rules to set up the R4, R5, and R6 resistors are explained in the SPV1050 datasheet, which includes the design equations shown below:

$$10M\Omega \leq R_{OUT(TOT)} \leq 20M\Omega \quad (1)$$

$$R6 = \frac{V_{BG}}{V_{EOC}} \cdot R_{OUT(TOT)} \quad (2)$$

$$R5 = \left(\frac{V_{BG}}{V_{UVP}} \cdot R_{OUT(TOT)}\right) - R6 \quad (3)$$

These equations are applied considering the following information:

- V_{BG} is the internal bandgap voltage (V_{BG} = 1.23 V, typical value).
- V_{EOC} is the battery end-of-charge target value.
- V_{UVP} is the battery under-voltage-protection target value.

In addition, the IC provides two open drain digital outputs to be connected to an external microcontroller:

- BATT_CONN provides feedback on the embedded pass transistor between V_{STORE} and V_{BAT}. This pin is pulled down when the pass transistor is closed; otherwise it is released once the pass transistor is opened. This information is not available at the 34-pin connector because it can be indirectly obtained as described in Section 2.6.
- BATT_CHG provides feedback on the DC-DC converter status. This pin is pulled down when the DC-DC converter is switching, while it is released when the DC-DC converter is not switching. For example, the BATT_CHG is at high logic level after V_{STORE} triggers $V_{STORE(EOC)}$ and until it drops by EOCHYS or during the sampling period (T_{SAMPLE}) of the maximum power point tracking (MPPT) algorithm.

The MPPT level can be set by a resistor input divider and allows maximizing the source power under any irradiance condition. If the MPPT mode is active, then the DC-DC stops switching for ~400 ms (T_{SAMPLE}) every ~16 seconds ($T_{TRACKING}$).

During the T_{SAMPLE}, the DC-DC input is at high impedance and the open circuit voltage V_{OC} at the input stage is sampled and stored by charging the C_3 (capacitor on the MPP_REF pin) through the MPP_SET pin.

When MPPT is enabled, the SPV1050 can regulate its impedance to extract the maximum power from the harvesting source. Typically, the datasheet of a harvested source reports the main electrical characteristics: open circuit voltage (V_{OC}) and voltage at maximum power (V_{MP}); the $MPPT_{RATIO}$ is consequently calculated as V_{MP}/V_{OC}. V_{MP} and V_{OC} can change according to the external conditions (light irradiation, temperature), but usually the effect on $MPPT_{RATIO}$ remains limited.

To properly select R1, R2, and R3, it is necessary to set some application parameters and then apply equations 4 to 7 below.

- Electrical characteristics of the harvesting source:
  - $V_{OC(MAX)}$, intended as V_{OC} at max operating condition of the source.
  - $MPPT_{RATIO}$, intended as V_{MP}/V_{OC} at typical operating conditions of the source.
- Application constraints:
  - $I_{LEAKAGE}$, intended as the acceptable leakage through the resistors at the input stage.
  - Usually, $0.1\mu A \leq I_{LEAKAGE} \leq 1\mu A$ fits for most of the applications.
- SPV1050 constraints:
  - $V_{EN\_TH(MAX)} \leq V_{MPP(MAX)} \leq \left(V_{UVP(MIN)} - 100mV\right) \Rightarrow 150mV \leq V_{MPP(MAX)} \leq 2.1V$
  - $V_{MPP(MAX)} \leq V_{OC(MAX)}$

$$R_{IN(TOT)} = R1 + R2 + R3 > \frac{V_{OC(MAX)}}{I_{LEAKAGE}} \cdot MPPT_{RATIO} \quad (4)$$

$$R1 = R_{IN(TOT)} \cdot \left(1 - \frac{V_{MPP(MAX)}}{V_{OC(MAX)}}\right) \quad (5)$$

$$R2 = R_{IN(TOT)} \cdot \frac{V_{MPP(MAX)}}{V_{OC(MAX)}} \cdot \left(1 - MPPT_{RATIO}\right) \quad (6)$$

$$R3 = R_{IN(TOT)} \cdot \frac{V_{MPP(MAX)}}{V_{OC(MAX)}} \cdot MPPT_{RATIO} \quad (7)$$

To increase the circuit efficiency, an external back-to-back pass transistor (U3) has been added. It allows reducing the R_{ON} resistance between V_{STORE} and V_{BAT}. By default, the back-to-back pass transistor is automatically driven by the BATT_CON signal. However, the customization section describes how to drive it manually.

The SPV1050 device embeds two fully independent LDOs, which provide 1.8 V and 3.3 V output voltage respectively. Both LDOs can supply up to 200 mA from V_{STORE}, and each of them can be enabled bthrough two dedicated pins: LDO1_EN and LDO2_EN, respectively. Note that the internal logic inhibits both LDOs when the embedded pass transistor between V_{STORE} and V_{BAT} is open.

2.1.2 PV V_{OC} measurement circuit

The STDES-ISV002V1 is equipped with a PV V_{OC} measurement circuit. It works together with the SPV1050 device, exploiting the property of photovoltaic panels to vary the V_{OC} according to light irradiation. This circuit allows enhancing the photovoltaic panel as an ambient light sensor.

Before being converted into a digital value, the V_{OC} value crosses a signal conditioning circuit which uses a TSU102 operational amplifier to adapt the values within the dynamic range defined by the microcontroller supply voltage. Furthermore, the circuit allows increasing the reading resolution by separating the indoor use case from the outdoor one.

The whole circuit can be supplied by different V_{DD} supply sources (V_{REG1}, V_{REG2}, V_{STORE}, V_{LDO2}). By default, it is supplied by the regulated 3.3V voltage LDO2 coming from the SPV1050. Different configuration can be selected by the V_{DD} selecting circuit.

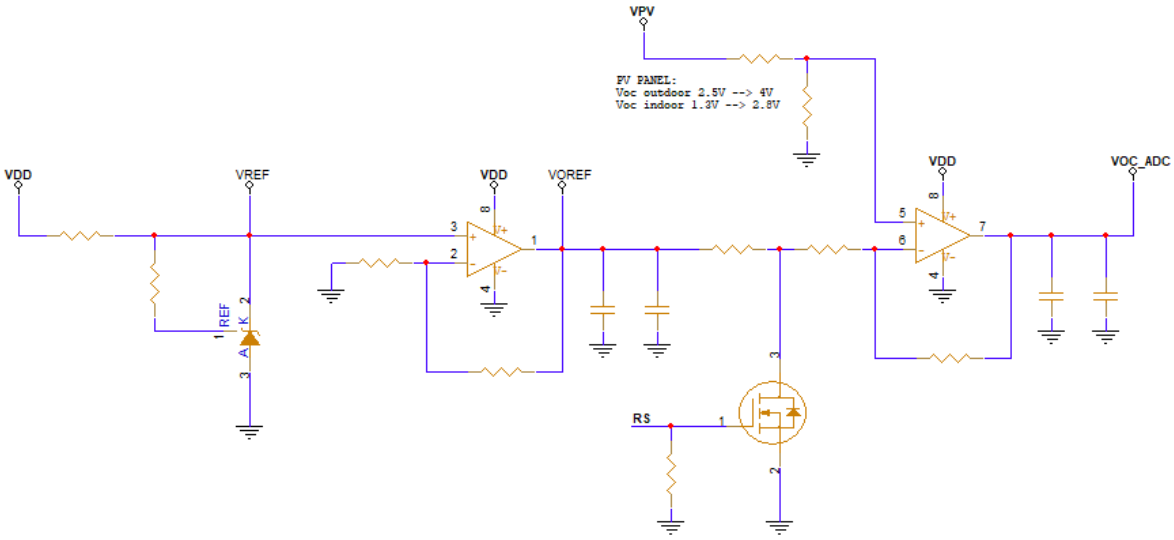
To correctly sample the V_{OC} voltage, the DC-DC embedded in the SPV1050 must be disabled. This is done by setting $V_{MPP} < V_{EN\_TH}$ (note that V_{EN_TH} = 0.1V typically).

The Range Selector (RS) pin fine tunes the PV V_{OC} measurement window according to the indoor or outdoor use cases.

Table 2. Indoor/outdoor cases addressed by RS value

RS logical value	CASE	Expected PV panel voltage range
High	Indoor	$0V \leq V_{PV} \leq 1.9V$
Low	Outdoor	$1.8V \leq V_{PV} \leq 4V$

Figure 2. PV V_{OC} measurement circuit



The next two figures show the relationship between the voltage at the output of the conditioning circuit V_{OC_ADC} and that PV panel voltage at the input (V_{PV}), in the outdoor and indoor use cases respectively, which are defined by the RS logical value according to Table 2.

Figure 3. **PV voltage swap - indoor case**

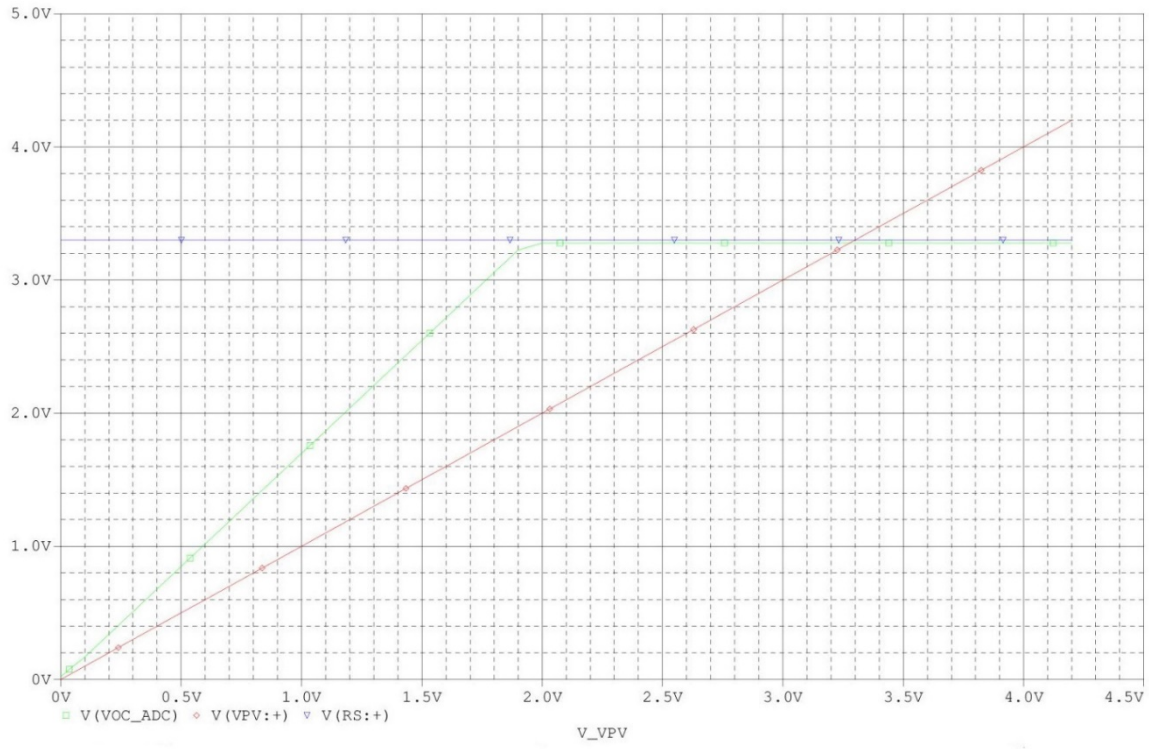
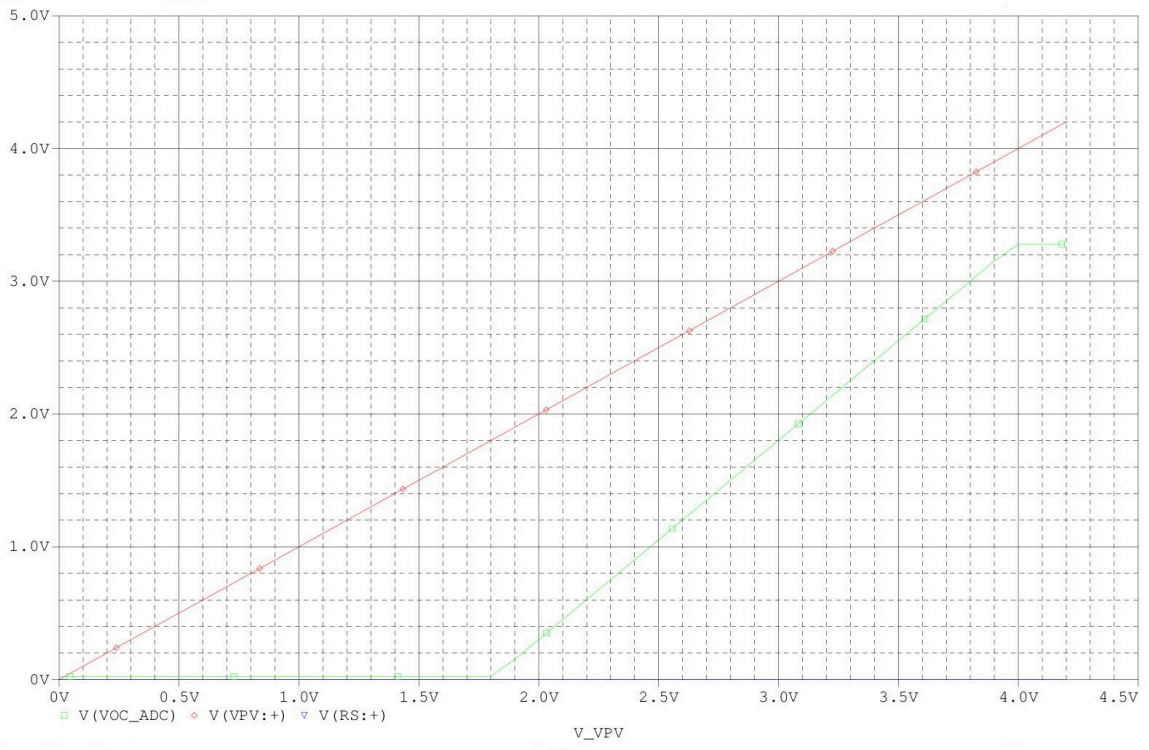


Figure 4. **PV voltage swap - outdoor case**



The PV V_{OC} measurement circuit combined with the SPV1050 device allow making evaluations on the available energy to be used by the system. The algorithm that allows retrieving this information is described in Algorithm.

As highlighted by the algorithm, the case of uncertainty that occurs when the voltage of the panel is in the range $1.8V \leq V_{PV} \leq 1.9V$ is included in the indoor use case.

2.1.3 V_{DD}, V_{REG1}, and V_{REG2} voltage selection

Multiple voltage sources are available on the STDES-ISV002V1. Some of them are generated by the on-board circuits (V_{STORE}, V_{LDO1}, V_{LDO2}). Others are exchanged by means of the 34-pin expansion connector (V_{REG1}, V_{REG2}).

The VDD voltage that supplies the PV V_{OC} measurement circuit can be linked to several supply sources (V_{REG1}, V_{REG2}, V_{STORE}, V_{LDO2}). By default, it is supplied by the regulated 3.3 V voltage LDO2 coming from the SPV1050. Different configuration can be selected by closing one of the solder bridges belonging to the group JP10, JP11, JP12, and JP13. See table below for the correct setup.

Warning: *Only one solder bridge must be used in this group to select the correct voltage. In fact, using two or more solder bridges generates short circuits.*

Table 3. V_{DD} selection table

JP10	JP11	JP12	JP13	V_{DD}	NOTE
CLOSED(1)	OPEN	OPEN	OPEN	V_{REG2}	Provided by the 34-pins expansion connector
OPEN	**CLOSED**(1)	OPEN	OPEN	V_{REG1}	
OPEN	OPEN	**CLOSED**(1)	OPEN	V_{STORE}	
OPEN	OPEN	OPEN	**CLOSED**(1)	V_{LDO2}	Default setting

1. *Only one solder bridge must be used in each setting.*

V_{REG1} and V_{REG2} voltages can be assumed by the STDES-ISV002V1 as input or output, according to what it is connected to it by means of the 34-pin connector.

If one or both of these voltages are assumed to be output, then the correct voltage to be exported can be selected by means of the two groups of jumpers JP14, JP15, JP16 and JP17, JP18, JP19, respectively. The available configurations are shown in the two tables below.

Warning: *Only one solder bridge must be used in each of the two groups to select the correct voltage. In fact, using two or more solder bridges generates short circuits.*

Table 4. V_{REG1} selection table

JP14	JP15	JP16	V_{REG1}
CLOSED(1)	OPEN	OPEN	V_{LDO1}
OPEN	**CLOSED**(1)	OPEN	V_{LDO2}
OPEN	OPEN	**CLOSED**(1)	V_{STORE}

1. *Only one solder bridge must be used in each setting.*

Table 5. V_{REG2} selection table

JP14	JP15	JP16	V_{REG1}
CLOSED(1)	OPEN	OPEN	V_{LDO1}
OPEN	**CLOSED**(1)	OPEN	V_{LDO2}
OPEN	OPEN	**CLOSED**(1)	V_{STORE}

1. *Only one solder bridge must be used in each setting.*

2.2 Photovoltaic modules

The STDES-ISV002V1 has been designed to be connected to two Panasonic amorphous silicon solar panels, model: AM-5412CAR. The outside dimension of each single panel is 50.1 mm × 33.1 mm, while the I-V characteristic of a single and the electrical specifications are in Figure 5 and Table 6 respectively. Curves refer to two characterization cases:

- 50k Lux measured by means of a Solar Simulator (SS)
- AM-1.5 100mW/cm2

AM is the air mass coefficient, which is commonly used to characterize the solar spectrum after solar radiation has gone across the atmosphere. "AM1.5" identifies performance of solar cells under solar zenith angle of 48.2° standardized conditions. "AM1.5" is almost universal when characterizing terrestrial power-generating panels referring to the overall yearly average irradiation for mid-latitude zones.

Figure 5. PV panel I-V characteristic

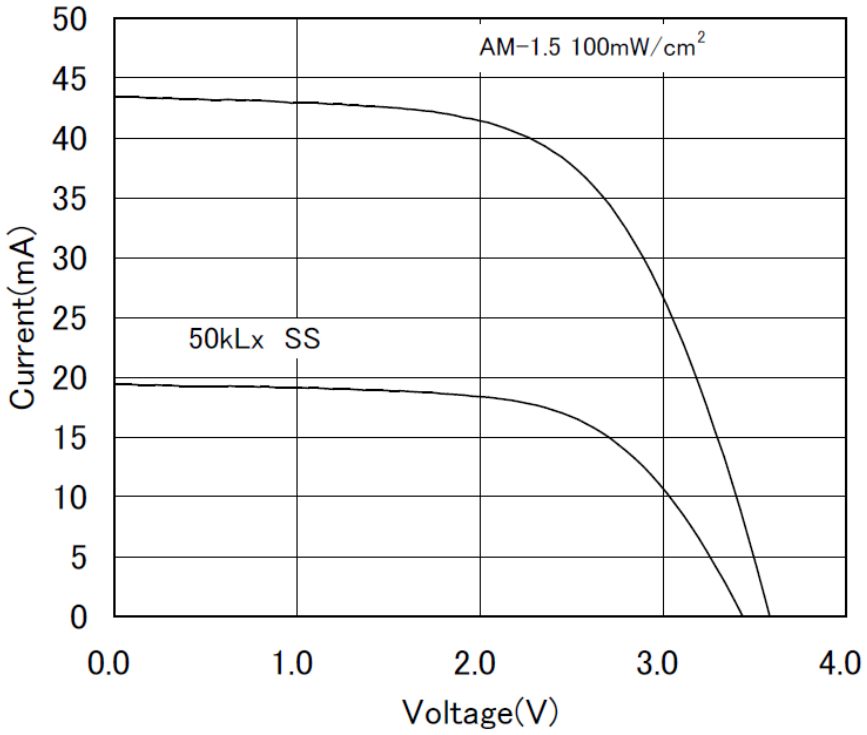


Table 6. Rated specifications (at 25 ºC)

ITEM	SPECIFICATION
Open circuit voltage: V_{OC}	3.4V Typ @ 50k Lux SS
Short circuit voltage: I_{SC}	19.4mA Typ @ 50k Lux SS
Operating voltage and current	2.2V – 17.9mA Typ @ 50k Lux SS 2.2V – 39.8mA Typ @ AM-1.5 100mW/cm2
Maximum output power	44mW (2.6V – 16.9mA Typ @ 50k Lux SS) 93mW (2.6V – 35.8mA Typ @ AM-1.5 100mW/cm2)

2.3 Features

The specifications of all the sub-blocks allows outlining the specifications of the STDES-ISV002V1:

- Energy harvesting expansion board based on SPV1050 set in boost configuration
- Cold start minimum input voltage 0.55 V
- Cold start minimum input current 30 µA
- 2.6 V to 5.3 V trimmable output overvoltage level (±1% accuracy)
- 2.2 V to 3.6 V trimmable output undervoltage level (±1% accuracy)
- Two fully independent LDOs (1.8 V and 3.3 V output) managed by enable/disable LDO pins
- PV voltage measurement circuit build around TSU102 operational amplifier
- Selectable outdoor and indoor PV voltage measurement range
- 34-pin expansion connector compatible with STEVAL-ASTRA1B

2.4 Default configuration and customizations

The STDES-ISV002V1 board is provided in a default configuration. However, by acting on solder bridges and jumpers it is possible to modify some functions.

A list of default solder bridge configurations is shown in Table 7. They are grouped by functionality.

VDD, VREG1, and VREG2 voltage selection describes how to select the power supply voltage that feeds the PV V_{OC} measurement circuit, as well as how to manage the two voltages V_{REG1} and V_{REG2}. This paragraph deals with the customizations that can be made on the use of the GPIO pins.

2.4.1 LDOs enabling signals

By default, the two solder jumpers J4 and J5 are set to allow LDOs to be enabled by the signals LDO1_EN_SIG and LDO2_EN_SIG, respectively. Alternatively, each of the two LDOs can be set to be always on when the STORE voltage is present.

LDO1 is the 1.8 V regulated voltage. According to the default configuration, the LDO1 regulator is enabled by the LDO1_EN_SIG signal managed by the GPIO3_ALT2 signal. This signal and the GPIO3_ALT1 signal can be alternatively connected to the GPIO3 pin through the 34-pin connector. In the default configuration, the GPIO3 signal is used to drive the switching on/off of the back-to-back transistor U3.

LDO2 is the 3.3 V regulated voltage. According to the default configuration, the LDO2 regulator is enabled by the LDO2_EN_SIG signal managed by the GPIO4 signal, which comes from the 34-pin connector.

2.4.2 Battery voltage to 34-pin connector

By default, the exposed battery voltage on the 34-pin connector comes from STORE voltage through the back-to-back transistor U3. J7 allows selecting the VBATT coming from SPV1050.

2.4.3 GPIOs

The four GPIOs that the 34-pin connector makes available are assigned to the purposes summarized in the following table.

PIN	LABEL	PURPOSE
J6.22	GPIO1	SPV1050 – DC-DC enable/disable signal
J6.24	GPIO2	MPPT enable/disable signal
J6.26	GPIO3_ALT1(1)	back-to-back circuit enable/disable
	GPIO3_ALT2(1)	LDO1 enable/disable signal
J6.28	GPIO4	LDO2 enable/disable signal

1. *See Table 7. Jumpers and solder bridges default configurations to check how to act on solder bridges J18 and J22 to select GPIO3_ALT1 or GPIO3_ALT2 alternate functions.*

2.4.4 PV VOC measurement circuit

Two solder bridges J23 and J24 are for the customization of the PV VOC measurement circuit. By default, J23 is CLOSED and J24 is OPEN, therefore PV V_{OC} measurement circuit accesses V_{OC} only when VDD is available. Alternatively, when J23 is OPEN and J24 is CLOSED, the V_{OC} is always connected to the PV V_{OC} measurement circuit.

Table 7. Jumpers and solder bridges default configurations

Solder bridge	Default configuration	Reference group	Notes
J1	CLOSED	SPV1050 device	
J2	CLOSED		
J3	CLOSED		
J4	1-2 CLOSED		Enabling of LDO1 driven by signal LDO1_EN
J5	1-2 CLOSED		Enabling of LDO2 driven by signal LDO2_EN
J7	1-2 CLOSED		The battery voltage transferred to the connector is the downstream voltage of the back-to-back pass transistor U3
J9	CLOSED		
J8	CLOSED		MPPT features managed by GPIO2 signal
J16	1-2 CLOSED		Back-to-back pass transistor U3 is is automatically driven by BATT_CON signal
J17	CLOSED	GPIOs linked to the 34-pins connector	
J18	OPEN		GPIO3 alternate function 2 is selected
J22	CLOSED		
J19	CLOSED		
J20	CLOSED		
J21	CLOSED		
J23	CLOSED	PV V_{OC} measurement circuit	PV V_{OC} measurement circuit accesses V_{OC} only when V_{DD} is present
J24	OPEN		
JP10	OPEN	V_{DD} selection	
JP11	OPEN		
JP12	OPEN		
JP13	CLOSED		
JP14	OPEN	V_{REG1} selection	
JP15	OPEN		
JP16	OPEN		
JP17	OPEN	V_{REG2} selection	
JP18	OPEN		
JP19	OPEN		

2.5 Measures

The two figures below show the recharging profiles (current and voltage) of a 3.7 V 100 mAh 501225 Li-Po rechargeable battery, supplied by the STDES-ISV002V1 managing the energy harvesting from the AM-5412CAR exposed to irradiation cases AM-1.5 and 60 k lux.

Figure 6. Test 1 - Outdoor_AM-1_5

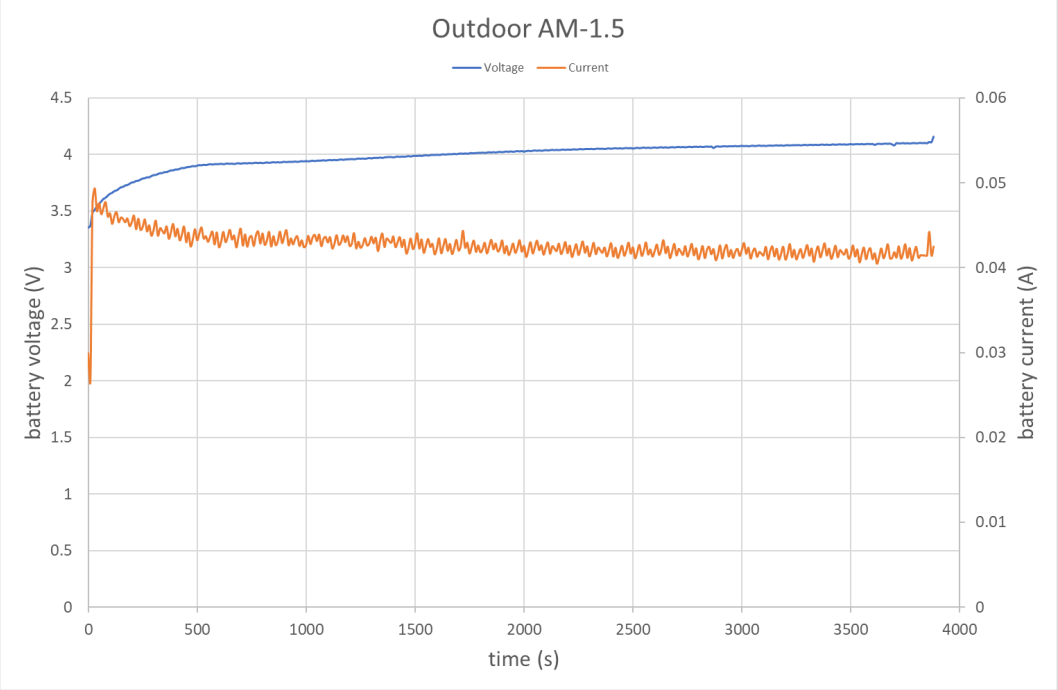
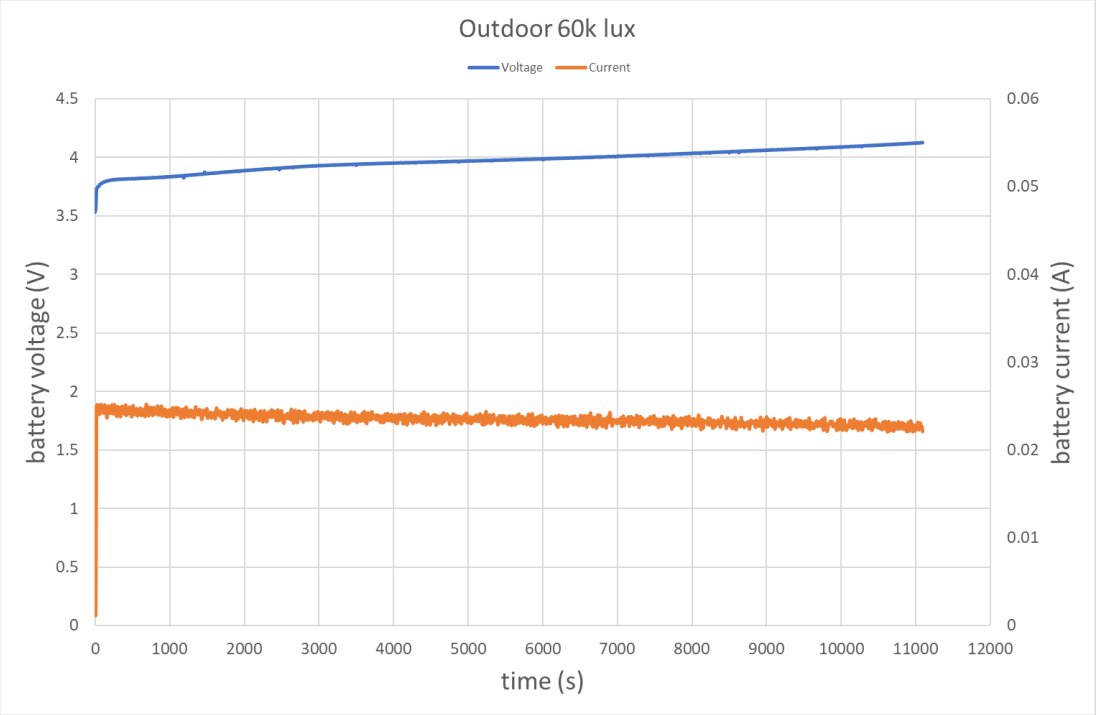


Figure 7. Test 2 - OutdoorSS_60000lux

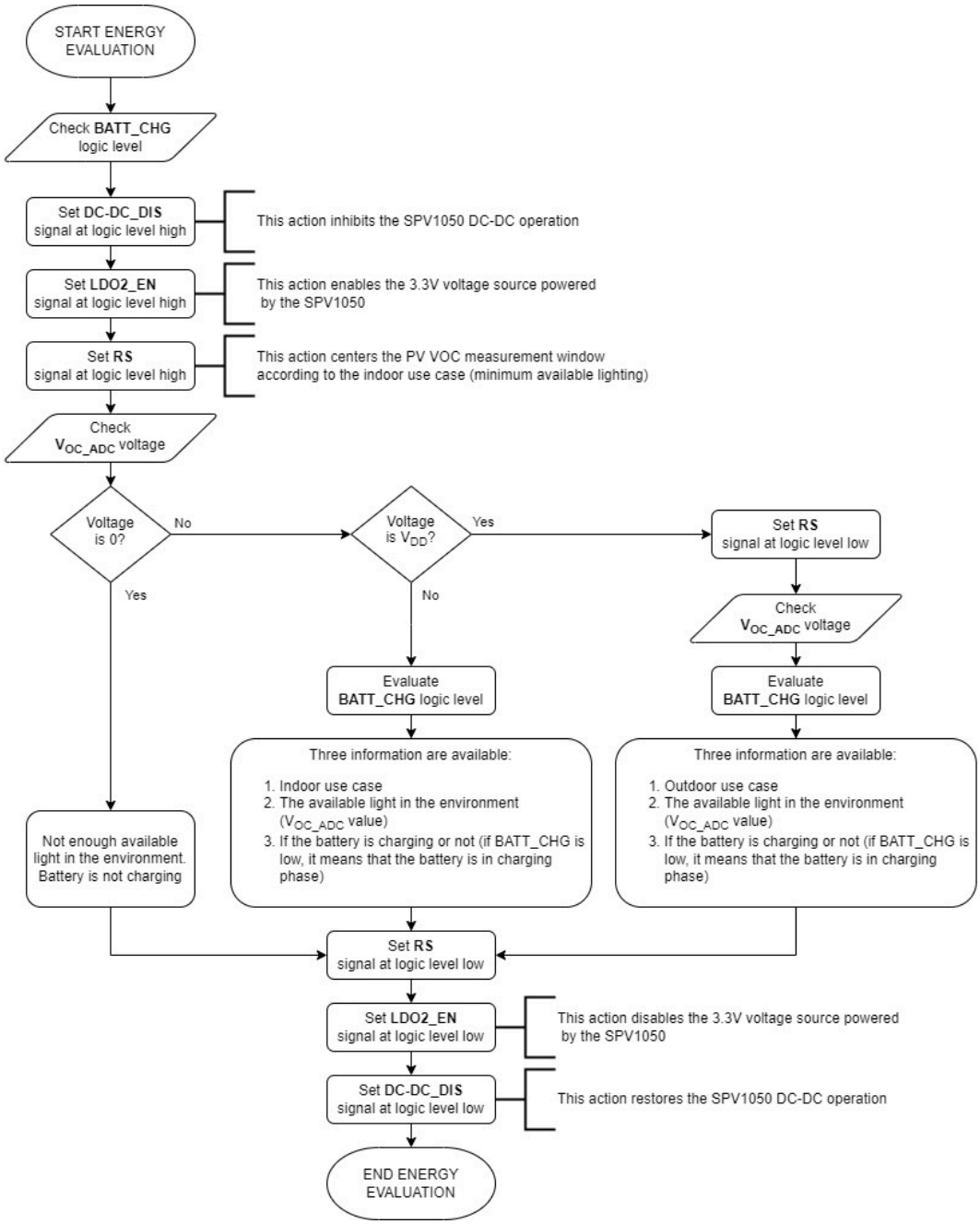


2.6 Algorithm

The STDES-ISV002V1 has been designed to make the user aware of:

- the indoor/outdoor use case
- the available light energy in the environment
- the battery charging status.

Figure 8. Algorithm



As soon as the energy evaluation procedure is started, the BATT_CHG logic level is checked. Then the signals DC-DC_DIS, LDO2_EN, and RS are set. These actions allow inhibiting the SPV1050 DC-DC operation, enabling the 3.3 V voltage source powered by the SPV1050, and cantering the PV VOC measurement window according to the indoor use case (minimum available lighting).

Then the VOC_ADC value is acquired and evaluated. If VOC_ADC voltage is zero or close to zero, it means there is not enough light available in the environment and the battery is therefore not charging.

Otherwise, if VOC_ADC voltage is more than zero and less than V_{DD}, the BATT_CHG logic level that was previously read is evaluated to make three pieces of information available:

- Indoor use case
- The available ambient light (VOC_ADC value)
- Whether the battery is charging or not (according to whether the BATT_CHG level is low or not). If the battery is charging, it means that the battery is connected to V_{STORE} and the BATT_CONN pin is pulled down.

If VOC_ADC voltage is V_{DD}, the PV V_{OC} measurement circuit must be set to accomplish the outdoor use case.

The RS signal is set at logic level low, then VOC_ADC voltage is acquired again and evaluated together with the BATT_CHG logic level. This allows making three pieces of information available:

- Outdoor use case
- The available ambient light (VOC_ADC value)
- Whether the battery is charging or not (according to whether the BATT_CHG level is low or not). If the battery is charging, it means that the battery is connected to V_{STORE} and the BATT_CONN pin is pulled down.

3 Connection with STEVAL-ASTRA1B

3.1 STDES-ISV002V1

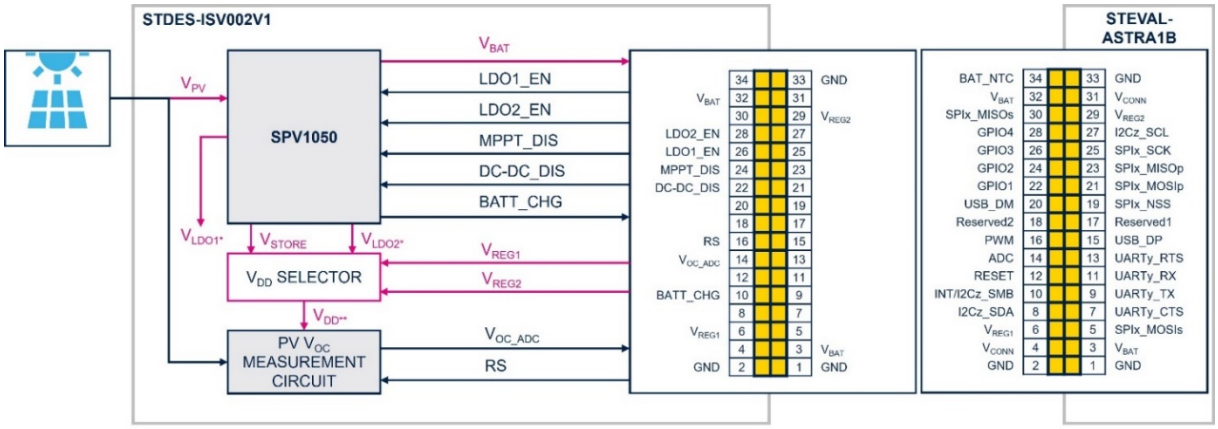
The STEVAI-ASTRA1B expansion connector plays multiple roles. The pinout of this connector was designed to match the application needs as well as to plug further expansion boards such as:

- other sensors or connectivity boards
- OLED/e-ink display
- SD card
- Datalogger
- energy harvesting systems.

Moreover, you can use it to connect flat cables in order to drive remote sensors or devices.

The figure below shows the coupling between the pinout of the STEVAL-ASTRA1B main board and that of the STDES-ISV002V1.

Figure 9. Connection with ASTRA



(*) V_{LDO1} = 1.8V (available but not used in the default configuration) – V_{LDO2} = 3.3V
(**) By default V_{DD} = V_{LDO2}

3.2 PV add-on plastic case

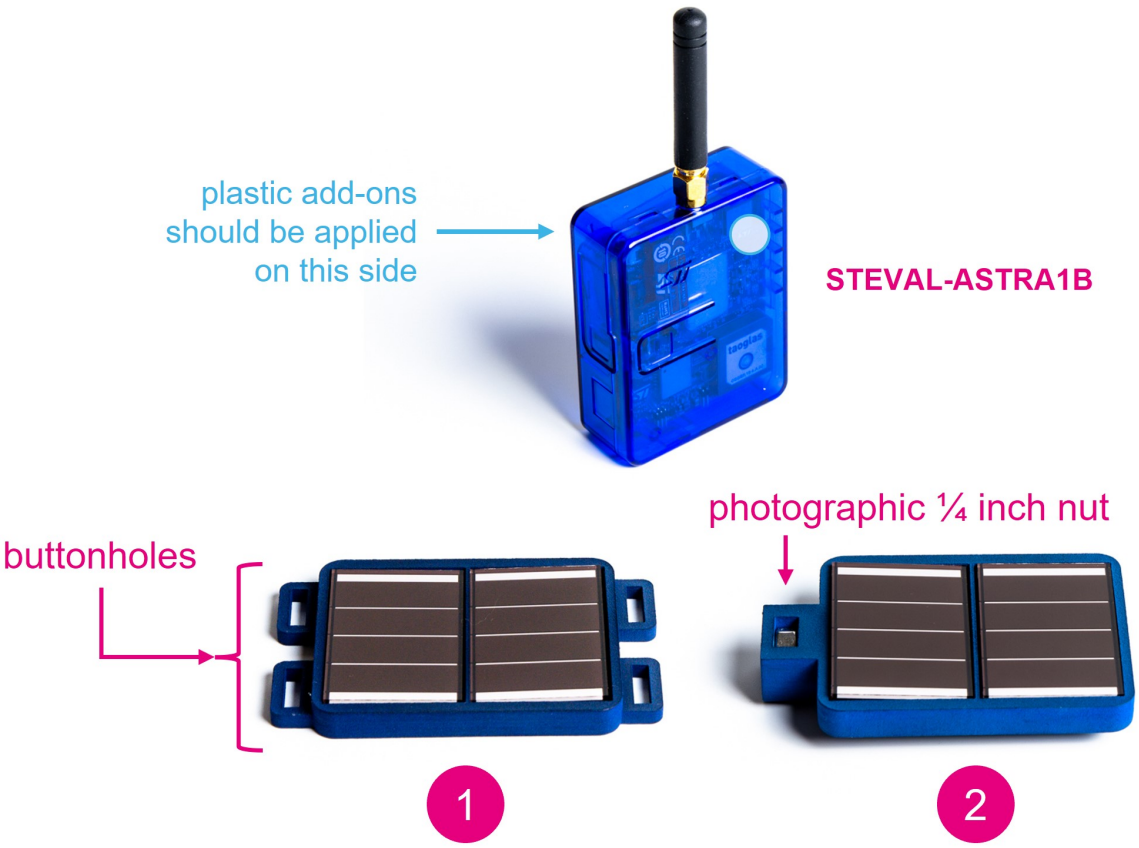
The STDES-ISV002V1 comes with a 3D printed add-on which hold two Panasonic amorphous silicon solar panels, model AM-5412CAR. Two designs are available:

1. 3D printed add-on with button holes that allow secure fixing by means of cable ties
2. 3D printed add-on equipped with a 1/4-inch photographic nut which makes the design compatible with all photographic support and anchoring equipment.

Both 3D printed add-ons can be docked to the STEVAL-ASTRA1B plastic case. They can be secured by means of double-sided tape. Alternatively, the 3D add-on recesses can be used as guides to make M2 holes in the STEVAL-ASTRA1B plastic case. This allows connecting the plastic case and the 3D printed add-on by using M2 screws and nuts.

The two solar panels can be attached to the 3D printed add-on with double-sided tape. The wires of the two photovoltaic panels must be connected to the CN1 connector of the STDES-ISV002V1. Therefore, the wires can pass through the plastic case by means of the STMOD+ opening or through an M3 hole made on the plastic case.

Figure 10. **PV panel plastic add-ons**



4 Compatibility with FP-ATR-ASTRA1

The FP-ATR-ASTRA1 is an STM32Cube function pack that implements a complete asset tracking application, as described in user manual UM3019. It has been developed to be compliant with the STM32Cube architecture and has been structured into a set of abstraction layers.

The hardware abstraction layer (HAL) interfaces with the hardware. It provides the low-level drivers and the hardware interface methods to interact with the upper layers (application, libraries, and stacks). It also provides the APIs for the communication peripherals (I²C, SPI, UART, etc.) for initialization and configuration, data transfer, and communication errors.

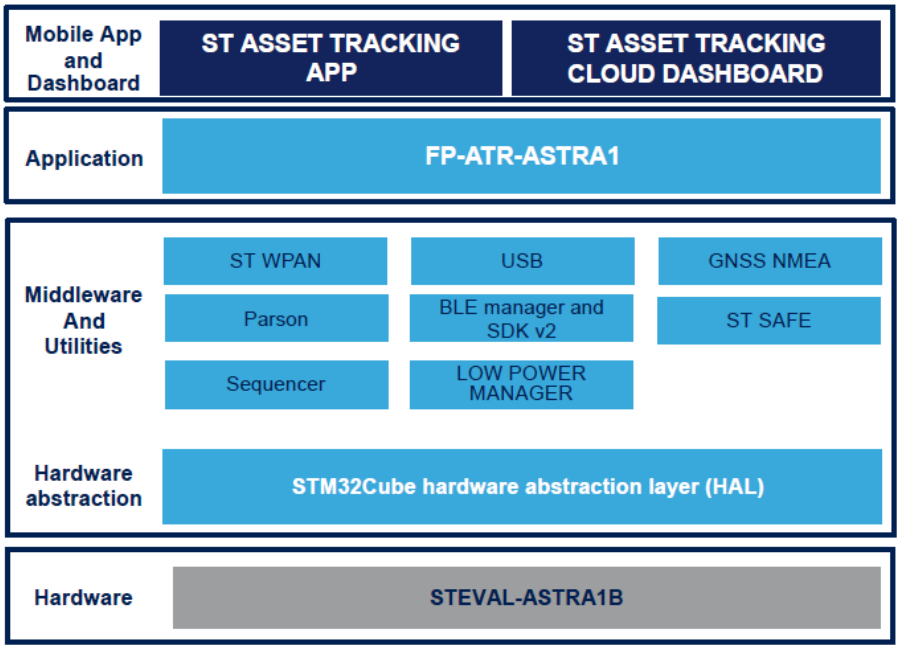
The package provides a board support package (BSP), which deals with the board-specific peripherals and functions (LED, user button, etc.). The BSP structure follows the hardware structure, including a component management layer as well as the specific modules of the board. The modules included in the BSP are selected according to the used hardware configuration.

Middleware and Utilities provide advanced libraries and protocols for USB communication, STM32-WPAN, GNSS NMEA, Bluetooth® Low Energy manager, STSAFE, sequencer, and low-power manager.

The horizontal interaction among the layer components is handled directly by calling the feature APIs. The vertical interaction with the low-level drivers is managed through specific callbacks and static macros implemented in the library system call interface.

On top, the application layer contains functions and procedures that characterize the application and can be changed by the end user.

Figure 11. FP-ATR-ASTRA1 software architecture

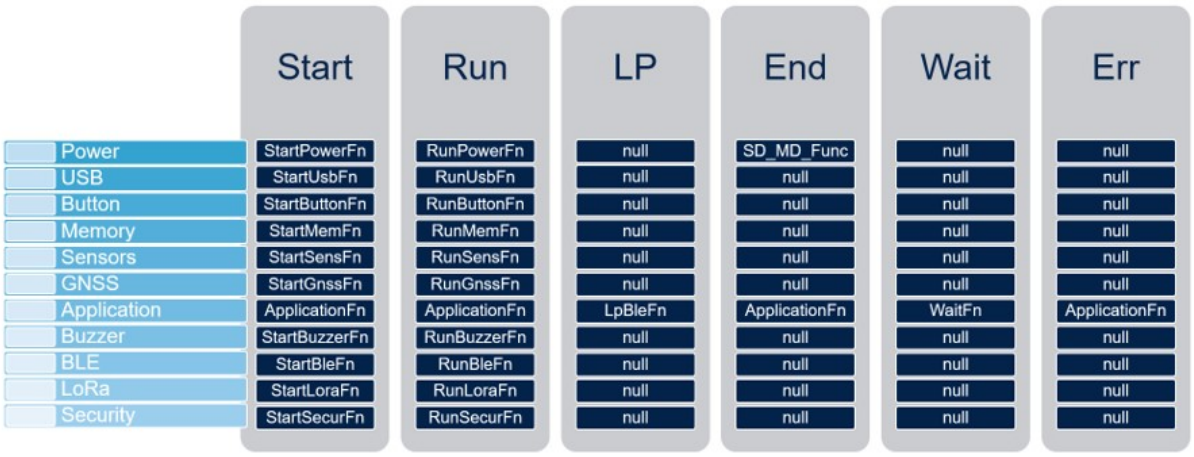


The application runs by means of a state machine. The status changes are based on events and triggers coming from the user buttons, MEMS sensors, as well as the result of specific algorithms or timer expiry. The two main states are: full-run state and low-power state. In the full-run state, everything is on, while in the low-power state, all the components except the MCU are configured in low-power mode. These states are not only related to the MCU power state, but to the whole system condition. The default application firmware provides the following states: “Start", "Run”, "LP", "End", “Wait”, and "Err". However, several further states can also be implemented, balancing system responsiveness and battery life.

The next image intersects the states supported by the state machine (columns) and the firmware modules (rows). It shows which function each module performs with respect to the relative state.

The STDES-ISV002V1 management can be thought of as a new firmware module to be added to the state machine.

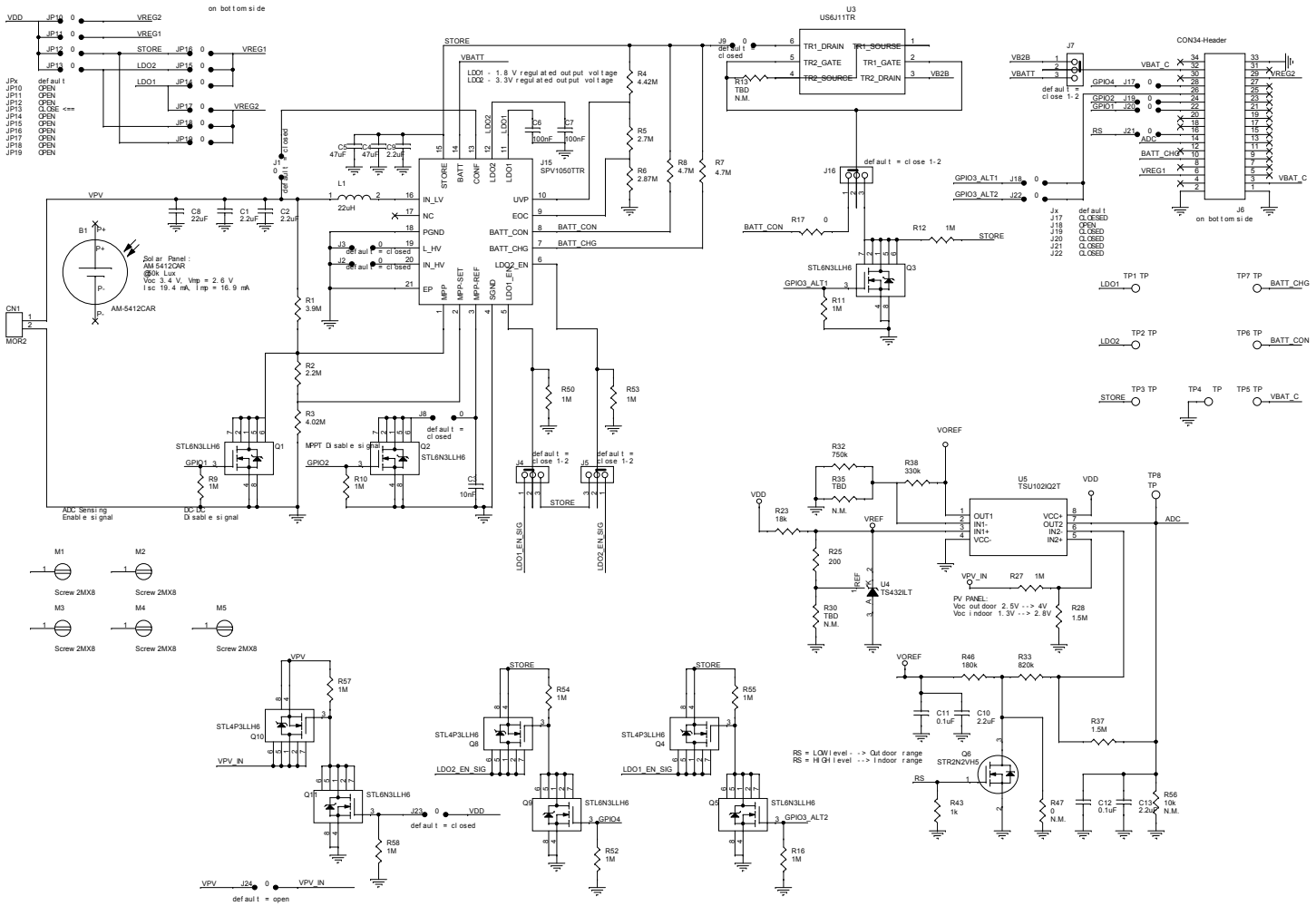
Figure 12. **State description**



More detailed information on how to add a new module in the state machine are described in the FP-ATR-ASTRA1 related documents. However, some files that update the state machine supporting the STDES-ISV002V1 are provided on request.

5 Schematic diagrams

Figure 13. **STDES-ISV002V1 circuit schematic**



Revision history

Table 8. **Document revision history**

Date	Version	Changes
08-Nov-2023	1	Initial release.

Contents

1 **Acronyms** 2
2 **STDES-ISV002V1** 3
2.1 Hardware 3
2.1.1 SPV1050 3
2.1.2 PV V_{OC} measurement circuit 4
2.1.3 V_{DD}, V_{REG1}, and V_{REG2} voltage selection 7
2.2 Photovoltaic modules 8
2.3 Features 9
2.4 Default configuration and customizations 9
2.4.1 LDOs enabling signals 9
2.4.2 Battery voltage to 34-pin connector 9
2.4.3 GPIOs 9
2.4.4 PV VOC measurement circuit 10
2.5 Measures 11
2.6 Algorithm 12
3 **Connection with STEVAL-ASTRA1B** 14
3.1 STDES-ISV002V1 14
3.2 PV add-on plastic case 14
4 **Compatibility with FP-ATR-ASTRA1** 16
5 **Schematic diagrams** 18
Revision history 19

List of figures

Figure 1. STDES-ISV002V1 block diagram . . . 3
Figure 2. PV V_{OC} measurement circuit . . . 5
Figure 3. PV voltage swap - indoor case . . . 6
Figure 4. PV voltage swap - outdoor case . . . 6
Figure 5. PV panel I-V characteristic . . . 8
Figure 6. Test 1 - Outdoor_AM-1_5 . . . 11
Figure 7. Test 2 - OutdoorSS_60000lux . . . 11
Figure 8. Algorithm . . . 12
Figure 9. Connection with ASTRA . . . 14
Figure 10. PV panel plastic add-ons . . . 15
Figure 11. FP-ATR-ASTRA1 software architecture . . . 16
Figure 12. State description . . . 17
Figure 13. STDES-ISV002V1 circuit schematic . . . 18

List of tables

Table 1. List of used acronyms . . . 2
Table 2. Indoor/outdoor cases addressed by RS value . . . 5
Table 3. V_{DD} selection table . . . 7
Table 4. V_{REG1} selection table . . . 7
Table 5. V_{REG2} selection table . . . 7
Table 6. Rated specifications (at 25 ºC) . . . 8
Table 7. Jumpers and solder bridges default configurations . . . 10
Table 8. Document revision history . . . 19