Migrating from STM32H730 and STM32H750 to STM32H7Rx/7Sx MCUs

Introduction

Designers of STM32 microcontroller applications must be able to easily replace one microcontroller type by another in the same product family or products from a different family.

Migrating an application to a different microcontroller is often needed when product requirements grow, putting extra demands on memory size, or increasing the number of I/Os. The objective of cost reduction may also be an argument to switch to smaller components and shrink the PCB area.

This application note analyzes the steps required to migrate from an existing design based on the STM32H730 or STM32H750 MCUs, to the STM32H7Rx/7Sx MCUs.

This document lists the full set of features available for the STM32H730 and STM32H750 devices, and the equivalent features on the STM32H7Rx/7Sx devices. This application note also provides a guideline on both hardware and peripheral migration.

To fully benefit from this application note, the user must be familiar with the STM32 microcontroller family. This application note is a complement to the STM32H730, STM32H750, and STM32H7Rx/7Sx datasheets and reference manuals. For additional information, refer to the product datasheets and reference manuals.

Table 1. Applicable products

Type	Part numbers
Microcontrollers	STM32H730 value line STM32H750 value line STM32H7R7/7S7 product line STM32H7R3/7S3 product line

1 General information

The STM32H730, STM32H750, and STM32H7Rx/7Sx MCUs are STM32 32-bit devices based on Arm® Cortex® processors.

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Reference documents

[1] Reference manual *STM32H7Rx/7Sx Arm®-based 32-bit MCUs* (RM0477)

[2] Reference manual *STM32H723/733, STM32H725/735 and STM32H730 Value line advanced Arm®-based 32-bit MCUs* (RM0468)

[3] Reference manual *STM32H742, STM32H743/753 and STM32H750 Value line advanced Arm®-based 32-bit MCUs* (RM0433)

[4] Datasheet *Arm® Cortex®-M7 32b 550 MHz MCU, 128 KB Flash, 564 KB RAM, Ethernet, USB, 3 × FD-CAN, Graphics, 2 × 16b ADCs, crypto/hash* (DS13315)

[5] Datasheet *Arm®Cortex®-M7 32-bit 480 MHz MCUs, 128 Kbyte flash, 1 Mbyte RAM, 46 com. and analog interfaces, crypto* (DS12556)

[6] Datasheet *Arm®Cortex®-M7 32-bit 600 MHz MCU, 64 KB flash, 620 KB RAM, Ethernet, 2x USB, 2x FD-CAN, advanced graphics and security, 2x 12-bit ADCs* (DS14359)

[7] Datasheet *Arm®Cortex®-M7 32-bit 600 MHz MCU, 64 KB flash, 620 KB RAM, Ethernet, 2x USB, 2x FD-CAN, advanced graphics, 2x 12-bit ADCs* (DS14360)

2 STM32H7Rx/7Sx MCUs overview

The STM32H7Rx/7Sx devices offer extra performance compared to the STM32H730, and the STM32H750 devices without additional complexity.

The STM32H7Rx/7Sx devices, as Cortex®-M7 variants, are compatible with the STM32H7 series devices (for the common packages). This compatibility allows customers to easily migrate from STM32H7Rx/7Sx to STM32H730 and STM32H750 devices, and benefit from their significantly higher performance and their advanced peripherals.

The STM32H7Rx/7Sx devices include a larger set of peripherals with advanced features and optimized power consumption compared to the STM32H730 and STM32H750 devices.

Some of the improved peripherals for the STM32H7Rx/7Sx are:

- Advanced security features
  - Life cycle support (HDPL0/1/2)
  - Root of trust (ST-iROT)
  - Debug authentication
  - Secure firmware install (SFI)
  - Root secure service (RSS)
  - HASH processor (HASH)
  - Cryptographic processor (CRYP)
  - Memory cipher engine (MCE): on-the-fly encryption/decryption (MCE) for OCTOSPI/Hexa-SPI or FMC external memory
  - True random generator (TRNG)
  - Public key accelerator (PKA)
  - Secure AES coprocessor (SAES)
- Advanced graphic peripherals
  - NeoChrom graphic processor (GPU2D) accelerating any angle rotation, scaling, and perspective correct texture mapping
  - Digital camera interface (DCMIPP)
  - Chrom-GRC (GFXMMU)
- External memories:
  - Two XSPI memory interfaces to support:
    - One or two OCTOSPI memories, quad memory
    - One OCTOSPI and one 16-bit SPI memory
- Advanced communication interface
  - Improved inter-integrated circuit (I3C)
  - USB Type-C® connector/USB power delivery interface (UCPD)
  - USB OTG full-speed controller with embedded PHY
  - USB OTG high-speed controller with embedded PHY
- Performance
  - Frequency up to 600 MHz
- Power supply
  - Dedicated external supply inputs for XSPI and USB to allow independent multiple voltage constraints and greater power supply choice
  - Embedded automatic voltage scaling (AVS) mechanism to ensure that the maximum frequency is reached with the minimum power consumption

Note: This document only manages the differences between STM32H730, STM32H750, and STM32H7Rx/7Sx for the common features. The new features of STM32H7Rx/7Sx are more detailed in the reference manual RM0477. The detailed list of available features and packages for each product is available in the respective product datasheet.

Table 2 summarizes the security and graphic IPs availability between STM32H7R3x8, STM32H7S3x8, STM32H7R7x8, and STM32H7S7x8 devices. For more details, refer to each device datasheet.

Table 2. Security and graphics IP availability per product line

IP type	-	STM32H7R3	STM32H7R7	STM32H7S3	STM32H7S7
Graphics	Neo-Chrom (GPU2D)	N	Y	N	Y
	Chrom-ART (DMA2D)	Y			
	Chrom-GRC (GFXMMU)	Y			
	Hardware codec (JPEG)	Y			
	LCD-TFT	N	Y	N	Y
	Parallel display (FMC8/16)	Y			
Security	Life cycle support (HDPL0/1/2)	Y			
	Root of trust (ST-iROT)	N	N	Y	Y
	Debug authentication	Y			
	Secure firmware install (SFI)	Y			
	Root secure service (RSS)	Y			
	HASH accelerator and PKA verification	Y			
	Crypto processor (Crypt, PKA, SAES)	N	N	Y	Y
	On-the-fly encryption/decryption (MCE)	N	N	Y	Y
	True random generator (RNG)	Y			

3 System architecture differences between STM32H7Rx/7Sx, STM32H730, and STM32H750 devices

The STM32H7Rx/7Sx architecture features a 64-bit AXI and 32-bit multilayer AHB bus matrix, and bus bridges that allow interconnecting bus masters with bus slaves, as illustrated in Figure 1.

In STM32H730 and STM32H750 devices, there are three domains: an AXI bus matrix in D1 domain, and two AHB bus matrices in D2 and D3 domain.

The differences in power modes are addressed in Section 6.2.5.

Table 3, Figure 1, Figure 2, and Figure 3 illustrate the system architecture differences between the STM32H7Rx/7Sx devices, STM32H730, and STM32H750 devices.

Table 3. Available bus matrix on STM32H7Rx/7Sx, STM32H730, and STM32H750 devices

Device	AHB bus matrix	AXI bus matrix
STM32H7Rx/7Sx	1	1
STM32H730 and STM32H750	2	1

Figure 1. STM32H7Rx/7Sx devices system architecture

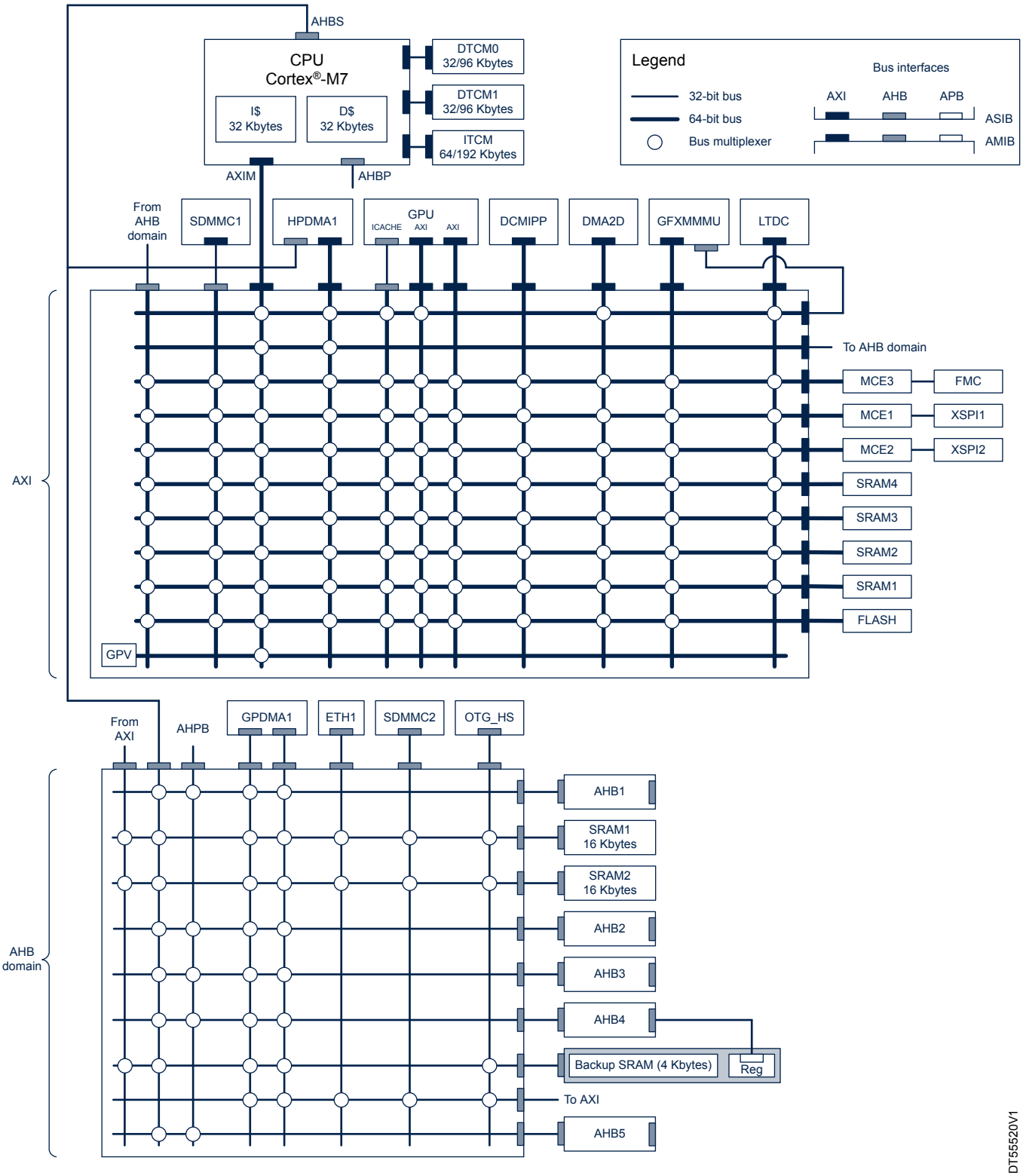


Figure 2. STM32H730 devices system architecture

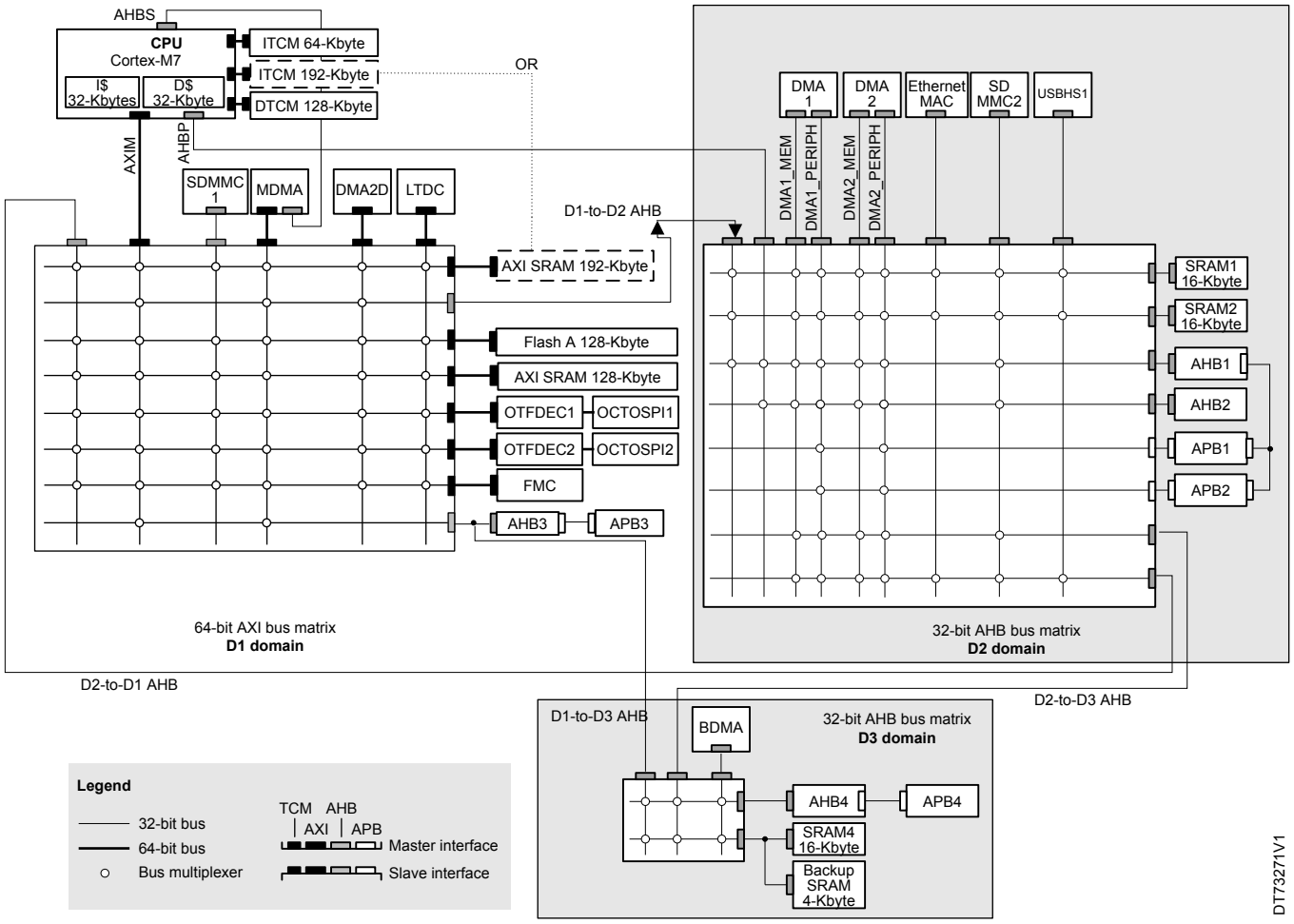
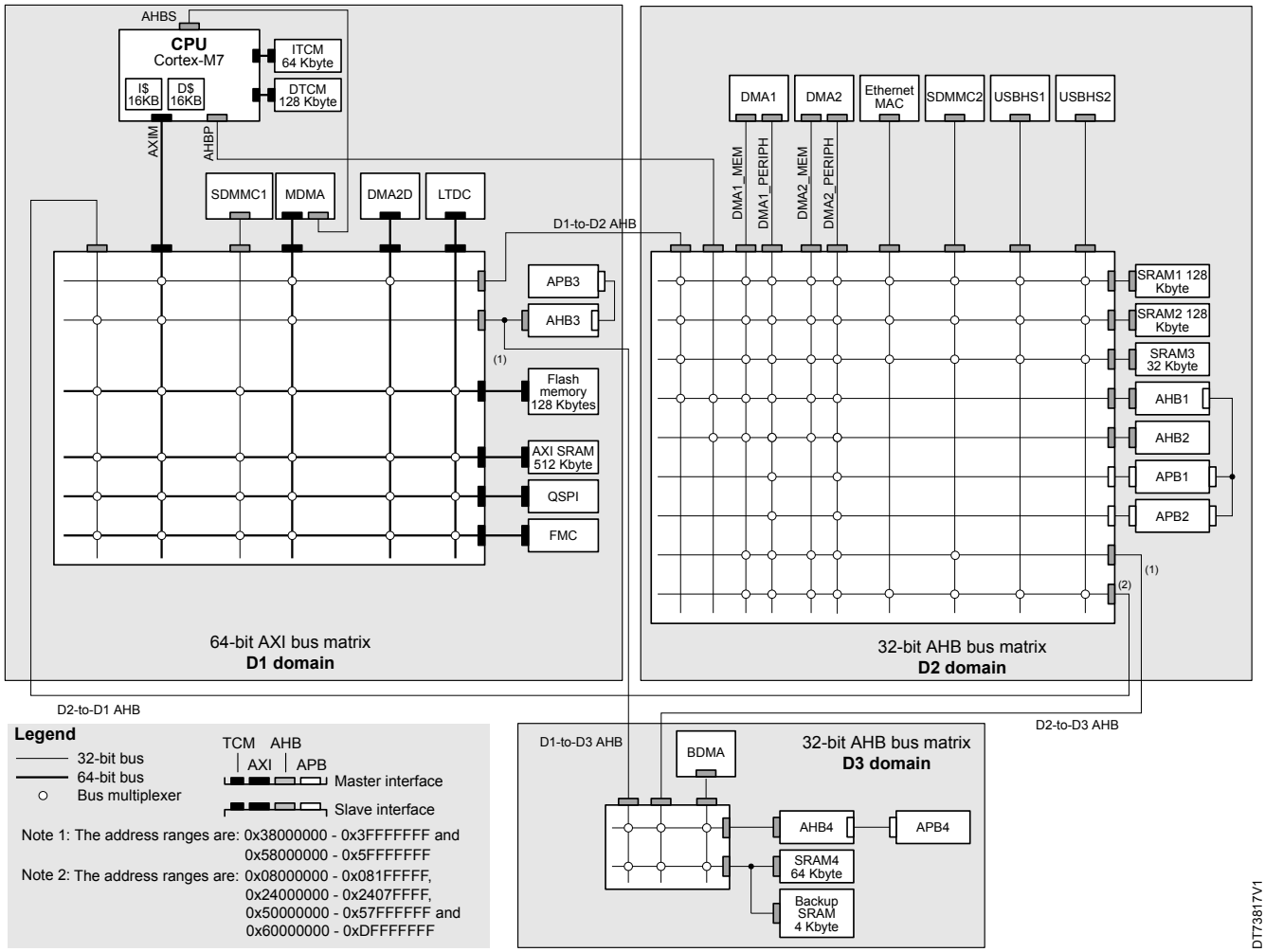


Figure 3. STM32H750 devices system architecture



4 Hardware migration

4.1 Package availability

The available packages on the STM32H7Rx/7Sx, STM32H730, and STM32H750 devices are listed in Table 4. The STM32H730 devices are offered in several packages ranging from 100 to 176 pins/balls. The STM32H7Rx/7Sx devices, on the other hand, are offered in packages ranging from 68 to 225 pins/balls.

The STM32H7Rx/7Sx and STM32H730 devices support the switched-mode power supply (SMPS) step-down converter available in some specific packages, which are not pinout compatible with the legacy packages. See Table 4.

The STM32H750 devices are offered in three packages ranging from 100 pins to 240 pins/balls and support only LDO option supply.

For more details on the pinout, refer to the product datasheets.

Table 4. Available packages on STM32H7Rx/7Sx, STM32H730, and STM32H750 devices

Package	STM32H750	STM32H730	STM32H7Rx/7Sx	Regulator
LQFP100	X	X	X(1)	LDO(3)
TFBGA100	NA	X	NA	
LQFP144	X	X	X(1)	
UFBGA144	NA	X	NA	
LQFP176	X	NA	NA	
UFBGA176+25	X	NA	NA	
TFBGA240+25	X	NA	NA	
VFQFPN68	NA	NA	X(1)	
UFBGA169 SMPS	NA	X	X(1)(2)	LDO/SMPS/ regulator bypass
UFBGA176+25 SMPS	NA	X	X(1)(2)	
LQFP176 SMPS	NA	X	X(1)(2)	
TFBGA100 SMPS	NA	NA	X(1)	
UFBGA144 SMPS	NA	NA	X(1)(2)	
WLCSP SMPS	NA	NA	X(1)(WLCSP101)	
TFBGA225 HEXA SMPS	NA	NA	X(1)(2)	
TFBGA225 OCTO SMPS	NA	NA	X(1)(2)	

1. *GP device package*
2. *GFx device package*
3. *The STM32H750 devices can be used in regulator bypass mode.*

4.2 Pinout compatibility

The STM32H7Rx/7Sx devices differ from the STM32H730 and STM32H750 devices in terms of MCU port assignment to package terminals, meaning their pinout or ballout is not identical. This holds for all common package types of the package listed in Table 4.

5 Boot mode compatibility

5.1 Boot mode selection

In STM32H730 and STM32H750 devices, two different boot spaces can be selected through the BOOT pin and the boot base address programmed in the BOOT_ADD0 or BOOT_ADD1 option bytes as shown in Table 5.

The BOOT_ADD0 and BOOT_ADD1 address option bytes can program any boot memory address from 0x0000 0000 to 0x3FFF 0000, which includes:

- All flash memory address space.
- All RAM address space: ITCM, DTCM RAMs, and SRAMs.
- The TCM-RAM.

Table 5. Boot modes for STM32H730 and STM32H750

Boot mode selection		Boot area
BOOT pin	Boot address option bytes	
0	BOOT_ADD0[15:0]	Boot address defined by user option byte BOOT_ADD0[15:0] STMicroelectronics programmed value: flash memory at 0x0800 0000
1	BOOT_ADD1[15:0]	Boot address defined by user option byte BOOT_ADD1[15:0] STMicroelectronics programmed value: system bootloader at 0x1FF0 0000

For the STM32H7Rx/7Sx devices, the boot memory space is selected by the BOOT pin and the NVSTATE as shown in Table 6. For NVSTATE=OPEN the choice is be made by the BOOT pin. For the NVSTATE=CLOSED, the boot is from the RSS in the system flash

Table 6. Boot modes for STM32H7Rx/7Sx

Boot mode selection		Boot area
NVSTATE	Boot pin	
Open	0	Boot from the user flash memory at 0x0800 0000
	1	Boot from the bootloader
Closed	-	Boot from the RSS in flash memory at 0x1FF0 0080

5.2 System bootloader

The system bootloader is located in the system memory, and programmed by STMicroelectronics during production. The system bootloader permits to reprogram the flash memory using one of the supported serial interfaces. More details are provided in the following table:

Table 7. STM32H7Rx/7Sx, STM32H730, and STM32H750 devices bootloader communication peripherals

System bootloader peripherals	STM32H750 I/O pin	STM32H730 I/O pin	STM32H7Rx/7Sx I/O pin
DFU	USB OTG FS (PA11/PA12) in device mode		USB OTG FS (PM12/PM11) in device mode
USART1	PA9/PA10 PB14/PB15	PA9/PA10	PA9/PA10
USART2	PA2/PA3		
USART3	PB10/PB11	PB10/PB11 PD8 / PD9	PD8/PD9

System bootloader peripherals	STM32H750 I/O pin	STM32H730 I/O pin	STM32H7Rx/7Sx I/O pin
UART4	NA		PD0/PD1
I2C1[1]	PB6/PB9		PB8/PB7
I2C2	PF0/PF1		PB10/PB11
I2C3	PA8/PC9		
SPI1	PA7/PA6/PA5/PA4		
SPI2	PI3/PI2/PI1/PI0	NA	PB15/PB14/PB13/PB12
SPI3	PC12/PC11/PC10/PA15		PC12/PB4/PB3/PA15
SPI4	PE14/PE13/PE12/PE11		NA
FDCANx[2]	NA	PH13/PH14 PD1/PD0	PB5/PB1

1. *Shared with I3C for STM32H7Rx/7Sx*
2. *FDCAN1 (for STM32H730) and FDCAN2 (for STM32H7Rx/7Sx).*

6 Peripheral migration

6.1 Cross-compatibility between STM32 products

The STM32 microcontrollers embed a set of peripherals that can be classified in the following groups:

- Group 1: Peripherals are common to all products.
  These peripherals have the same structure, registers, and control bits. There is no need to perform any firmware change to keep the same functionality at the application level after migration.
  All the features and behavior remain the same.
- Group 2: These peripherals are shared by all products but may have minor differences to support new features. The migration from one product to another is relatively easy and does not require significant new development effort..
- Group 3: Peripherals that have considerable changes from one product to another (for example new architecture or new features). For this group of peripherals, the migration requires a new development at the application level.

Table 8 summarizes the available peripherals in STM32H730 and STM32H750 devices compared to STM32H7Rx/7Sx devices.

All the features and peripherals listed in Table 8 for the STM32H7Rx/7Sx are relative to the package TFBGA225 HEXA SMPS .

Table 8. Peripheral summary for STM32H7Rx/7Sx, STM32H730, and STM32H750 devices

'-' = not available

Peripherals		STM32H750	STM32H730	STM32H7Sxx	STM32H7Rxx
Maximum CPU frequency		480 MHz	550 MHz	600 MHz	
MPU region number		16	16		
Data cache (Kbytes)		16	32	32	
Instruction cache (Kbytes)		16	32	32	
User flash memory (Kbytes)		128 Kbytes	128 Kbytes	64 Kbytes	
SRAMs (Kbytes)		864	Up to 368(1)	Up to 488(2)	
TCM RAM (Kbytes)	ITCM	64	Up to 256(1)	Up to 192(2)	
	DTCM	128	128	Up to 192(2)	
Backup SRAM (Kbytes)		4	4	4	
External memories	FMC	1	1		
	SDMMC	2	2		
	XSPI	1 Quad-SPI interface	2 OCTOSPI interfaces	2 XSPI interfaces	
Timers	High resolution	8 (16 bits)	-		
	General purpose	8 (16 bits)/ 2 (32 bits)	4 (32 bits)/ 10 (16 bits)	4 (32 bits)/ 7 (16 bits)	
	Advanced control (PWM)	2 (16 bits)	2 (32 bits)	1 (16 bits)	
	Basic	2 (16 bits)	2 (16 bits)		
	Low-power	5 (16 bits)	5 (16 bits)	5 (16 bits)	
	GFXTIM	-	-	1	
	SysTick timer	1	1		
	Watchdog	2	2		
	RTC	1	1		

Peripherals		STM32H750	STM32H730	STM32H7Sxx	STM32H7Rxx
Communication interfaces	SPI/I2S	6/3	6/4		
	I2C	4	5	3	
	I3C	-	-	1	
	USART/UART	4/4	5/5	3/4	
	LPUART	1	1		
	SAI	4	2		
	SPDIFRX	4 inputs			
	SWPMI	1	1		
	MDIO	1	1		
	FDCAN/TT-FDCAN	1/1	2/1	2/-	
	USB OTG FS	1	-	1	
	USB OTG HS	1[3]			
	UCPD	-	-	1	
	HDMI-CEC	1	1		
	DFSDM	Yes (8 channels/4 filters)		-	
	ADF	-	-	Yes (1 filter)	
Digital camera interface	Ethernet	1			
	DCMI	Yes	Yes	-	
	DCMIPP	-		Yes	
	PSSI	-	Yes		
Graphics	Chrom-ART Accelerator™ (DMA2D)	Yes			
	JPEG codec	Yes	-	Yes	
	GFXMMU	-	-	Yes	
	ICACHE	-	-	Yes[4]	
	Neo-Chrom (GPU2D)	-	-	Yes[4]	
	LCD-TFT	Yes		Yes[4]	
GPIOs		Up to 168	Up to 128	Up to 152	
DTS (Digital temperature sensor)		-		1	
Analog peripheral	12-bit ADC	-	1 (up to 17 channels)	2 (up to 19 channels)	
	16-bit ADC	3 (up to 36 channels)	2 (up to 20 channels)	-	
	12-bit DAC	2		-	
	Operational amplifier	2		-	
	Ultra-low-power comparator	2		-	
	Temperature sensor (connected to ADC)	1 (ADC3)		1 (ADC1)	
DMA		4 DMA: 2 dual port DMA, 1 MDMA, 1 BDMA		2 dual port DMA: HPDMA, GPDMA	
Cryptographic acceleration		• Random number generator (RNG) • HASH processor		• Random number generator (RNG) • HASH processor • PKA verification	
		Cryptographic processor		Cryptographic processor	-

Peripherals		STM32H750	STM32H730	STM32H7Sxx	STM32H7Rxx
Cryptographic acceleration		-		• Secure AES coprocessor (SAES) • Public key acceleration (PKA)	-
		-	2 × OTFDEC for OCTOSPI memory	3 × MCE for OCTO/ Hexa-SPI memory and FMC	
Security feature		• Configuration protection • Write protection (WRP) • Tamper detection			
		• Global device readout protection (RDP) • Proprietary code readout protection (PC-ROP) • Secure access mode: root secure services (RSS) and secure user memory		• Product life cycle • Debug authentication • Secure access mode: root secure services (RSS) and secure hide protection (HDP)	
				Root of trust (STiRoT or OEMiRoT)	-
Operating temperatures	Ambient temperatures	–40° to +85 °C	–40° to +125 °C(5)	–40° to +85 °C	
	Junction temperatures	–40° to +125 °C VOS0 up to 105 °C	–40° to +140 °C(6) VOS1 up to 140 °C VOS0 up to 105 °C	–40° to +125 °C VOS high up to 105 °C	
Operating voltage		1.62 to 3.6 V(7)		1.71 to 3.6 V	

1. *Includes 192 Kbytes shared between ITCM and AXI.*
2. *Includes 128 Kbytes shared between ITCM and AXISRAM1 and 128 Kbytes shared between DTCM and AXISRAM3 and 72 Kbytes shared between ECC and AXISRAM4.*
3. *USB OTG high-speed interface with full-speed capability.*
4. *Not available in STM32H7R3/S3x8.*
5. *125 °C can be reached only for part numbers in temperature range 3. For part numbers in temperature range 6, this value must be decreased to 85 °C.*
6. *140 °C can be reached only for part numbers in temperature range 3. For part numbers in temperature range 6, this value must be decreased to 125 °C.*
7. *V_{DD} can drop down to 1.62 V by using an external power supervisor and connecting PDR_ON pin to VSS. Otherwise, the supply voltage must stay above 1.71 V with the embedded power voltage detector enabled.*

6.2 System peripherals

6.2.1 Embedded flash memory (FLASH)

Table 9 compares the flash memory interface between the STM32H7Rx/7Sx, STM32H730, and STM32H750 devices.

For more information on programming, erasing, and protection, refer to the corresponding product reference manual.

Table 9. Flash memory differences

Flash memory	STM32H750	STM32H730	STM32H7Rx/7Sx
Main/program memory	128 Kbytes		64 Kbytes
	One bank and one sector of 128 Kbytes.		One bank divided in 8 sectors of 8 Kbytes each.
Feature	• Programming granularity: 256 bits • Single flash word write: 256-bit granularity		• Programming granularity: 128 bits

Flash memory	STM32H750	STM32H730	STM32H7Rx/7Sx
	• Read operations supporting multiple lengths (64 bits, 32 bits, 16 bits, or one byte) • Sector erase, bank erase		• Single flash word write: 128-bit granularity • Read operations supporting multiple lengths (64 bits, 32 bits, 16 bits, or one byte) • Sector erase, bank erase
ECC error code correction (ECC)	• One error detection/correction or two error detections per 256-bit. • Flash memory word using 10 ECC bits.		One error detection/correction or two error detections per 128-bit flash memory word using 9 ECC bits.
Wait-states	Up to four (depending on the core voltage and frequency).	Up to three (depending on the core voltage and frequency).	Up to seven (depending on the core voltage and frequency).
User option bytes	Yes		
One time programmable (OTP) memory	-		One Kbyte
Protection mechanisms	• Configuration protection • Write protection		
	• Global device readout protection (RDP) • Proprietary code readout protection (PCROP) • Secure access mode areas		• Temporal isolation management (HDPL) • Product life cycle management (product state) • Secure access mode areas • OTP locking

6.2.2 SRAMs

Table 10 shows the difference of RAM size between STM32H7Rx/7Sx, STM32H730, and STM32H750 devices.

All devices feature a RAM ECC monitoring unit (RAMECC). It provides a mean for application software to verify the ECC status and execute service routines when an error occurs.

The RAM ECC monitoring unit includes the following features:

- RAM ECC monitoring per domain
- RAM failing address/data identification

Internal SRAM data are protected by ECC. It supports single-error and double-error detection, as well as single-error correction:

- 7 ECC bits are added per 32-bit word.
- 8 ECC bits are added per 64-bit word.

For STM32H7Rx/7Sx devices, the ECC is enabled/disabled by the user option byte `ECC_ON_SRAM` (refer to Flash memory option byte word 2 status register (FLASH_OBW2SR) in RM0477 for more details).

Table 10. Comparison of RAM size between STM32H7Rx/7Sx, STM32H730, and STM32H750 devices

Memory		STM32H750	STM32H730	STM32H7Rx/7Sx	Units
TCM-RAM	ITCM-RAM (instruction)	64	64 to 256(1)	64 to 192(2)	Kbytes
	DTCM-RAM (data)	128	128	64 to 192(2)	
AXI-SRAM	AXI-SRAM1	Up to 512	128 to 320(1)	0 to 128(2)	
	AXI-SRAM2	-	-	128	
	AXI-SRAM3	-	-	0 to 128(3)	
	AXI-SRAM4	-	-	0 to 72(4)	
	Total AXI-SRAM	Up to 512	Up to 320	Up to 456	
AHB_SRAM	SRAM1	128 (D2 domain)	16 (D2 domain)	16	
	SRAM2	128 (D2 domain)	16 (D2 domain)	16	
	SRAM3	32 (D2 domain)	-	-	
	SRAM4	64 (D3 domain)	16 (D3 domain)	-	
	Total AHB-SRAM	352	48	32	
Backup SRAM		4			
Total		1060	564	620	
ECC		TCM and SRAMs	TCM and SRAMs	AXISRAM1, AXISRAM3, BKPSRAM, and TCM	-

1. *Includes 192 Kbytes shared between ITCM and AXI SRAM.*
2. *Includes 128 Kbytes shared between ITCM / AXI SRAM1.*
3. *Includes 128 Kbytes shared between DTCM/AXI-SRAM3.*
4. *72 Kbytes SRAM shared with ECC.*

6.2.3 Direct memory access controller (DMA)

The STM32H7Rx/7Sx, STM32H730 and STM32H750 devices have different DMA architecture and features.

The STM32H730 and STM32H750 DMA controllers are high-speed general-purpose master direct memory access controllers (MDMA), dual-port DMAs with FIFO and request router capabilities, and basic DMA with request router capabilities (BDMA).

The STM32H7Rx/7Sx devices DMA controllers are general-purpose direct memory access controllers (GPDMA), and high-performance direct memory access (HPDMA) with FIFO and linked-listed support.

All the devices also embed a Chrom-ART Accelerator (DMA2D), a specialized DMA dedicated to image manipulation.

Table 11. DMA features

-	STM32H750/STM32H730			STM32H7Rx/7Sx	
Instance	Dual-port DMA	BDMA	MDMA	HPDMA	GPDMA
Number of instances	2	1			
Number of masters	Dual AHB master	single AHB master	AXI/AHB master	AXI/AHB master	Dual AHB master
Number of channels	8		16		
Data transfers from source to destination	Peripheral-to-memory, memory-to-peripheral, memory-to-memory and peripheral-to-peripheral data transfers				
Privileged/ unprivileged support	-			Yes	
Linked-list	-		Yes		

6.2.4 Reset and clock control (RCC)

The table below presents the main differences related to the RCC (reset and clock controller) between the STM32H7Rx/7Sx, STM32H730, and STM32H750 devices.

Table 12. RCC features

Source clock		STM32H750	STM32H730	STM32H7Rx/7Sx
Internal oscillators	HSI	64 MHz		
	HSI48	48 MHz		
	CSI	4 MHz		
	LSI	32 KHz		
External oscillators	HSE	4-50 MHz		
	LSE	32.768 KHz		
PLLs		Three PLLs: • One for system clock, two for kernel clocks. • Input frequency range: – 1 to 2 MHz when VCOL is used. – 2 to 16 MHz when VCOH is used.		
		VCO frequency range: • VCOH: 192 to 836 MHz • VCOL: 150 to 420 MHz		VCO frequency range: • VCOH: 384 to 1672 MHz before the divider • VCOL: 150 to 420 MHz
AXI and AHB max frequency		240 MHz	275 MHz	300 MHz
APB max frequency		120 MHz	137.5 MHz	150 MHz
RTC clock source		LSE, LSI, or HSE/32		
Kernel clock		Independent kernel clock for each IP, allowing frequency scaling without any impact on the communication interfaces.		
System clock source		HSI, CSI, HSE, or PLL1		
Clock security system		CSS on HSE CSS on LSE		
MCO clock source		MCO1 pin (PA8): HSI, LSE, HSE, PLL1, or HSI48 MCO2 pin (PC9): SYSCLK, PLL2, HSE, PLL1, CSI, or LSI		

Peripheral clock configuration

The peripheral clocks are the clocks provided by the RCC to the peripherals. Two kinds of clocks are available:

- The bus interface clocks
- The kernel clocks

On STM32H7Rx/7Sx, STM32H730, and STM32H750 devices, the peripherals generally receive:

- One or several bus clocks.
- One or several kernel clocks.

The following table describes an example of peripheral clock distribution for STM32H730, STM32H750 and STM32H7Rx/7Sx devices. For more details about peripheral clock distribution, refer to the peripheral clock distribution summary of the product reference manual.

Table 13. Peripheral clock distribution example

Peripherals	STM32H750	STM32H730	STM32H7Rx/7Sx
I3C1	NA		rcc_pclk1 pll3_r_ck hsi_ker_ck csi_ker_ck
FDCAN	hse_ck pll1_q_ck pll2_q_ck rcc_pclk1		hse_ker_ck pll1_q_ck pll2_p_ck rcc_pclk1
FMC	rcc_hclk3 pll1_q_ck pll2_r_ck per_ck		rcc_hclk5 pll1_q_ck pll2_r_ck hsi_ker_ck rcc_aclk
MCE1, MCE2, MCE3	NA		rcc_aclk rcc_hclk5
GPU2D, GFXMMU	NA		rcc_hclk5 rcc_aclk
DTS	rcc_pclk4		lse_ck rcc_pclk4
GFXTIM	NA		pclk5
HASH	rcc_hclk2		rcc_hclk3
RNG	hsi48_ck pll1_q_ck lse_ck lsi_ck rcc_hclk2		hsi48_ker_ck hclk3

6.2.5 Power (PWR)

Table 14 presents the PWR controller differences between STM32H750, STM32H730, and STM32H7Rx/7Sx devices. Figure 4, Figure 5, and Figure 6 present the different supply configurations for these devices.

The STM32H7Rx/7Sx uses an automatic voltage scaling (AVS) mechanism which is automatically selected when using an internal power supply. The AVS setting is die dependent, and cannot be modified. All values given in this document are derived and guaranteed for an internal supply with LDO or SMPS only, and not when a bypass mechanism is used.

The STM32H750 devices embed an LDO regulator (LDO) with configurable scalable output to supply the digital circuitry. The different supply configurations is controlled by software at system start-up.

The STM32H7Rx/7Sx and STM32H730 devices embed two regulators: LDO and SMPS to provide the V_{CORE} supply for digital peripherals, SRAMs (except BKPSRAM), and embedded flash memory. These regulators can provide different voltages (voltage scaling) and can operate in Stop modes.

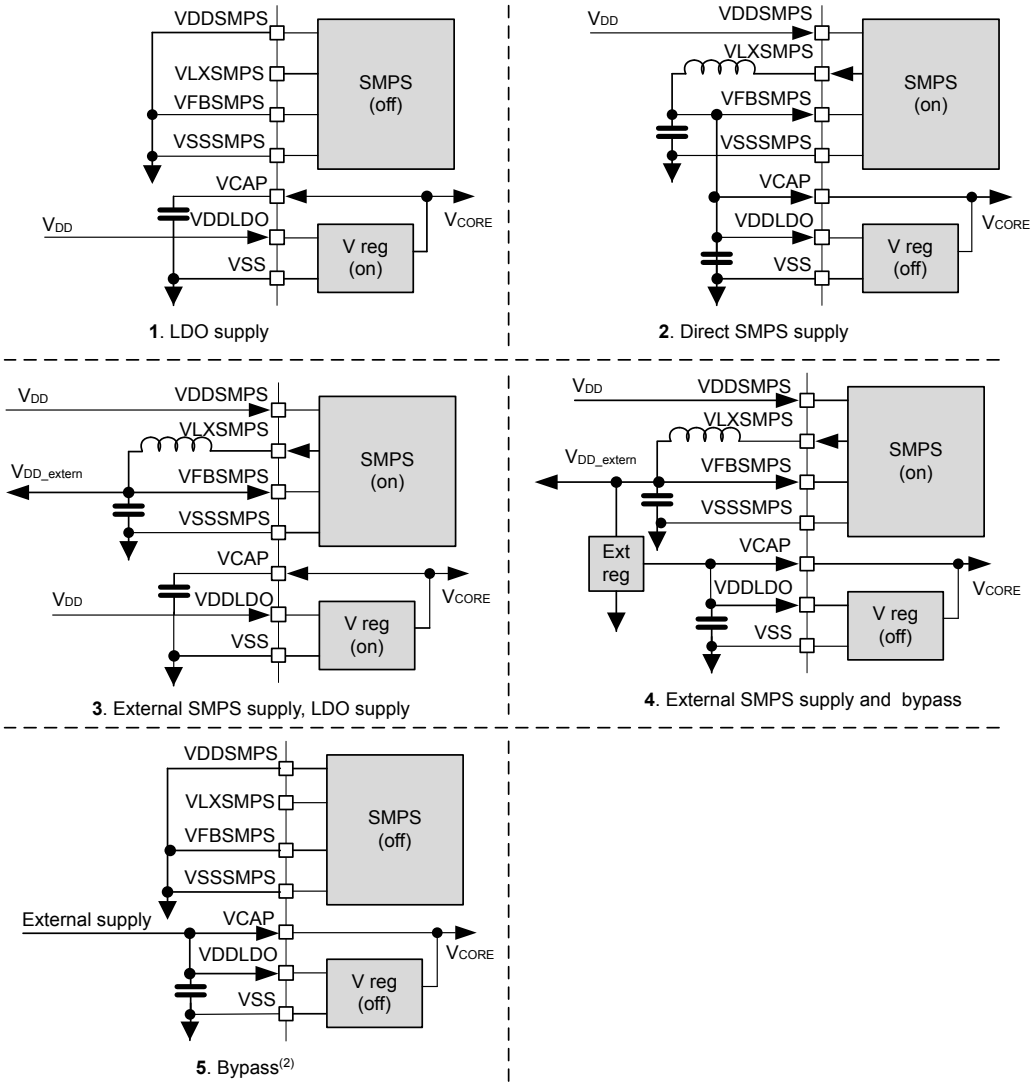
For the STM32H730 and STM32H7Rx/7Sx devices, there is no dedicated pin that defines if the regulator is in bypass mode or which regulator(s) is/are used. It is done through software at system startup. Both LDO and SMPS regulators are enabled by default during startup and the user software defines if the LDO or the SMPS or both are switched off.

Table 14. PWR controller differences between the STM32H7Rx/7Sx, STM32H730 and STM32H750 devices

Peripherals			STM32H750	STM32H730	STM32H7Rx/7Sx
Low-power modes			• CSleep (CPU clock stopped) • CStop (CPU subsystem clock stopped) • DStop (domain bus matrix clock stopped) • Stop (system clock stopped) • DStandby (domain powered down) • Standby (system powered down)		• Sleep (CPU clock stopped and still in Run mode) • Stop (system clock stopped) • Standby (system powered down)
System supply voltage regulation		SMPS	NA	Yes	Yes
		LDO	Yes	Yes	Yes
		SMPS supplies LDO	NA	Yes	NA
		External (bypass)	Yes	Yes	Yes
Voltage scaling		Run mode	VOS0 to VOS3		• VOS low • VOS high
		Stop mode	SVOS3 to SVOS5		• SVOS low • SVOS high
Power supplies	External power supply for I/Os		V_{DD} = 1.62 to 3.6 V		V_{DD} = 1.71 to 3.6 V
	Internal regulator (LDO) supplying V_{CORE}		V_{DDLDO} = 1.62 to 3.6 V		V_{DDLDO} = 1.71 to 3.6 V
	Step-down converter (SMPS) supplying V_{CORE}		NA	• V_{DDSMPS} = 1.62 to 3.6 V • V_{LXSMPS} = V_{CORE} or 1.8 V • V_{FBSMPS} = V_{CORE} or 1.8 V	V_{DDSMPS} = 1.71 to 3.6 V V_{LXSMPS} = V_{CORE} or 1.8 V V_{FBSMPS} = V_{CORE} or 1.8 V
	External analog power supply		V_{DDA} = 1.62 to 3.6 V		V_{DDA} = 1.71 to 3.6 V
	USB power supply		$V_{DD33USB}$ = 3.0 to 3.6 V $V_{DD50USB}$ = 4.0 to 5.5 V		$V_{DD33USB}$ = 3.0 to 3.6 V $V_{DD50USB}$ = 4.0 to 5.5 V
	Backup domain		V_{BAT} = 1.2 to 3.6 V		V_{BAT} = 1.2 to 3.6 V
	XSPI power supply		NA		$V_{DDXSPI1}$ = 1.62 to 3.6 V $V_{DDXSPI2}$ = 1.62 to 3.6 V
	V_{CORE} supplies		0.7 V ≤ V_{CAP} ≤ 1.35 V		0.74 V ≤ V_{CAP} ≤ 1.36 V
	Reg bypass: must be supplied from an external regulator on V_{CAP} pins.		V_{OS0} = 1.38 V		$V_{OS\ high}$ = 1.38 V
			V_{OS1} = 1.2 V		
			V_{OS2} = 1.1 V		$V_{OS\ low}$ = 1.23 V
			V_{OS3} = 1.03 V		
Peripheral supply regulation			USB regulator		USB regulator
Power supply supervision			• POR/PDR monitor • BOR monitor • PVD monitor • AVD monitor(1) • V_{BAT} thresholds(2) • Temperature thresholds(3)		

1. *Analog voltage detector (AVD): Monitor the V_{DDA} supply by comparing it to a threshold selected by the ALS[1:0] bits in the PWR_CR1 register. The AVD is enabled by setting the AVDEN bit in the PWR_CR1 register.*
2. *Battery voltage thresholds (V_{BAT} thresholds): Indicate if V_{BAT} is higher or lower than the threshold. The V_{BAT} supply monitoring (available only in V_{BAT} mode) can be enabled/disabled via the MONEN bit in the PWR_CR2 register.*
3. *Temperature thresholds: Indicates whether the device temperature is higher or lower than the threshold. The temperature monitoring can be enabled/disabled via the MONEN bit in the PWR_CR2 register.*

Figure 4. System supply configuration on STM32H7Rx/7Sx



Notes:
The mode SMPS supplies LDO is not supported in STM32H7Rx/Sx.
The SMPS step-down converter is not available on all packages, and the Bypass mode is available only when the SMPS is available.

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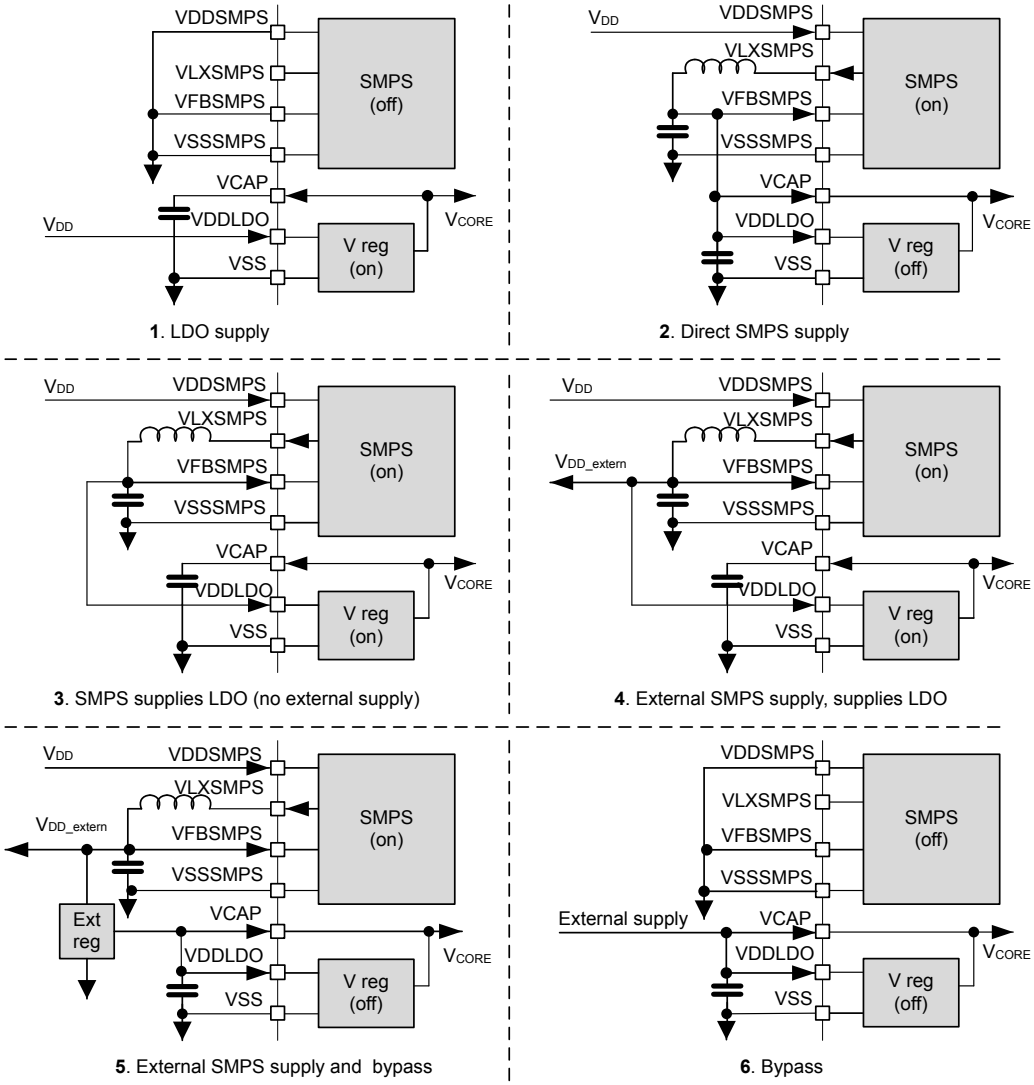
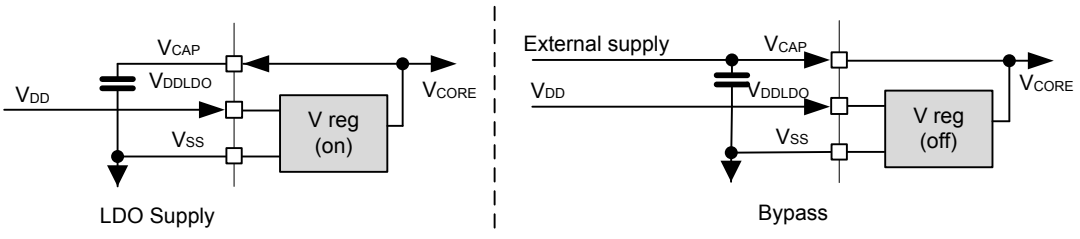
Figure 5. System supply configuration on STM32H730



Note: The SMPS step-down converter is not available on all packages, and the Bypass mode is available only when the SMPS is available.

Figure 6. System supply configuration on STM32H750



6.2.6 General-purpose I/Os (GPIO)

The STM32H7Rx/7Sx devices implement the same GPIO features than the STM32H730 and STM32H750 devices, but with main differences. For the STM32H7Rx/7Sx devices, each GPIO port has:

- Four 32-bit configuration registers:
  - `GPIOx_MODER`
  - `GPIOx_OTYPER`
  - `GPIOx_OSPEEDR`
  - `GPIOx_PUPDR`
- Two 32-bit data registers:
  - `GPIOx_IDR`
  - `GPIOx_ODR`
- A 16-bit reset register:
  - `GPIOx_BRR`
- A 32-bit set/reset register:
  - `GPIOx_BSRR`
- A 32-bit locking register:
  - `GPIOx_LCKR`
- Two 32-bit alternate function selection registers:
  - `GPIOx_AFRH`
  - `GPIOx_AFRL`

All GPIO registers in STM32H7Rx/7Sx can be read and written by privileged and unprivileged access, whatever the security state (secure or nonsecure).

High-speed low-voltage mode (HSLV)

All the I/Os of the STM32H7Rx/7Sx devices have the capability to increase their maximum speed at low voltage by configuring them in high-speed low-voltage mode (HSLV). The I/O HSLV bit controls whether the I/O output speed is optimized to operate at 3.3 V (default setting) or at 1.8 V (HSLV = 1).

Caution: *The I/O HSLV configuration bit must not be set if the I/O supply (VDD) is above 2.7 V. Setting it while the voltage is higher than 2.7 V can damage the device. There is no hardware protection associated to this feature so it is recommended to use it only as a static configuration for fixed I/O supply.*

Caution: *The GPIOs are all programed with the same HSLV setting, except those from dedicated power rails (OCTO, HEXA, and USB):*

- *XSPIM2 rail: PN[0:12]*
- *XSPIM1 rail: PO[0:5], PP[0:15]*
- *USB no software compensation setting*

Note: For more information about the procedure to set the HSLV mode, refer to the general-purpose I/Os (GPIO) section of the reference manual.

6.2.7 Extended interrupt and event controller (EXTI)

6.2.7.1 EXTI main features in STM32H7Rx/7Sx devices

The extended interrupt and event controller (EXTI) manages wake-up through configurable and direct event inputs. It provides wake-up requests to the power control, generates interrupt requests to the CPU NVIC, and events to the CPU event input.

The asynchronous event inputs are classified in two groups:

- Configurable events:
  - Active edge selection
  - Dedicated pending flag
  - Triggerable by software
  - Individual interrupt and event generation mask

- Direct events (interrupt and wake-up sources from other peripherals, requiring to be cleared in the peripheral) with the following features:
  - Fixed rising edge active trigger
  - No interrupt pending status register bit in the EXTI (the interrupt pending status is provided by the peripheral generating the event)
  - Individual interrupt and event generation mask
  - No software trigger possibility

Table 15 describes the difference of EXTI features between STM32H7Rx/7Sx, STM32H730, and STM32H750 devices.

Table 15. EXTI features

EXTI	STM32H750	STM32H730	STM32H7Rx/7Sx
Main features	• All event inputs allow the CPU to wake up and generate a CPU interrupt and/or a CPU event. • Two groups of event input: configurable events and direct events.		
	Some event inputs allow the user to wake up the D3 domain for autonomous Run mode and generate an interrupt to the D3 domain.		NA
	Up to 78 independent event/ interrupt lines	Up to 80 independent event/ interrupt lines	Up to 61 independent event/ interrupt lines

6.2.7.2 *EXTI block diagram in STM32H7Rx/7Sx*

As shown in Figure 7, the EXTI consists of:

- A register block accessed via an APB interface.
- An event input trigger block.
- A masking block.

The register block contains all the EXTI registers. The event input trigger block provides event input edge trigger logic.

Figure 7. EXTI block diagram on STM32H7Rx/7Sx

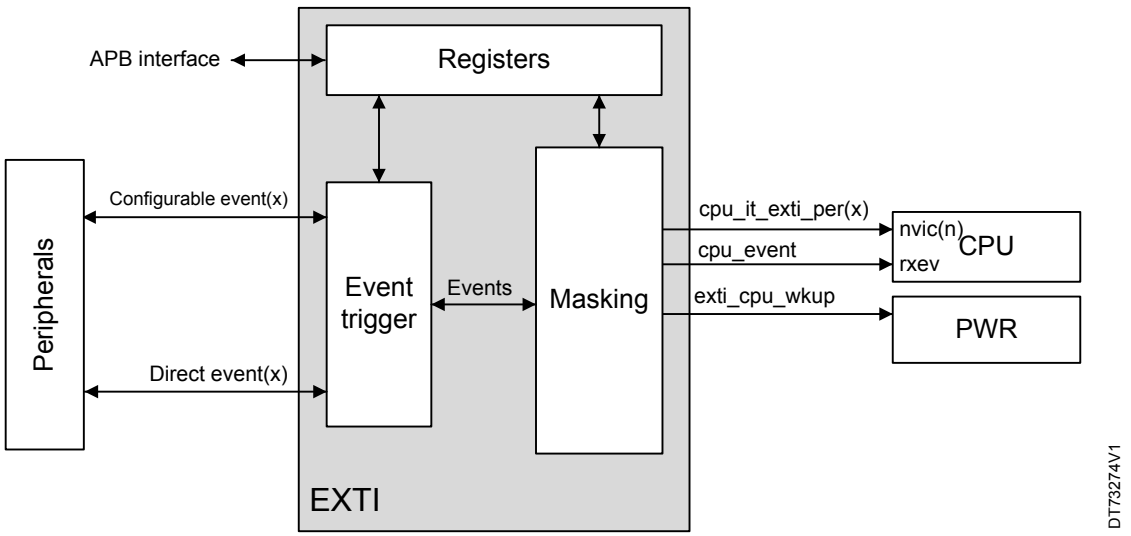


Table 16 presents the EXTI line differences between STM32H7Rx/7Sx, STM32H730, and STM32H750 devices:

Table 16. EXTI line differences

EXTI line	STM32H750	STM32H730	STM32H7Rx/7Sx
0 - 15	EXTI[15:0]		
16	PVD and AVD		
17	RTC alarms		
18	RTC tamper, RTC timestamp, LSE_CSS		
19	RTC wake-up timer		
20	COMP1		VBUS_FS_PLUG_UNPLUG
21	COMP2		VBUS_HS_PLUG_UNPLUG
22	I2C1 wake-up		
23	I2C2 wake-up		
24	I2C3 wake-up		
25	I2C4 wake-up		I3C1 wake-up
26	USART1 wake-up		
27	USART2 wake-up		
28	USART3 wake-up		
29	USART6 wake-up		Reserved
30	UART4 wake-up		
31	UART5 wake-up		
32	UART7 wake-up		
33	UART8 wake-up		
34	LPUART1 RX wake-up		ADF wake-up
35	LPUART1 TX wake-up		LPUART1 wake-up
36	SPI1 wake-up		
37	SPI2 wake-up		
38	SPI3 wake-up		
39	SPI4 wake-up		
40	SPI5 wake-up		
41	SPI6 wake-up		
42	MDIO wake-up		
43	USB1 wake-up		USB_OTG_FS wake-up
44	USB12 wake-up	Reserved	USB_OTG_HS wake-up
45	Reserved		UCPD wake-up
46	Reserved		ETH_ wake-up
47	LPTIM1 wake-up		
48	LPTIM2 wake-up		
49	LPTIM2 output		LPTIM2 CH1
50	LPTIM3 wake-up		
51	LPTIM3 output		LPTIM3 CH1
52	LPTIM4 wake-up		
53	LPTIM5 wake-up		
54	SWPMI wake-up		HDMI-CEC wake-up

EXTI line	STM32H750	STM32H730	STM32H7Rx/7Sx
55	WKUP1		
56	WKUP2		
57	WKUP3	Reserved	WKUP3
58	WKUP4		
59	WKUP5	Reserved	WGLS wake-up
60	WKUP6		Reserved
61	RCC interrupt		Reserved
62	I2C4 event interrupt		Reserved
63	I2C4 error interrupt		Reserved
64	LPUART1 global interrupt		Reserved
65	SPI6 interrupt		Reserved
66	BDMA CH0 interrupt		Reserved
67	BDMA CH1 interrupt		Reserved
68	BDMA CH2 interrupt		Reserved
69	BDMA CH3 interrupt		Reserved
70	BDMA CH4 interrupt		Reserved
71	BDMA CH5 interrupt		Reserved
72	BDMA CH6 interrupt		Reserved
73	BDMA CH7 interrupt		Reserved
74	DMAMUX2 interrupt		Reserved
75	ADC3 interrupt		Reserved
76	SAI4 interrupt		Reserved
77	Reserved	HSEM0 interrupt	DTS wake-up
78	Reserved		
79	Reserved		
80	Reserved		
81	Reserved		NA
82	Reserved		NA
83	Reserved		NA
84	Reserved		NA
85	HDMI-CEC wake-up		NA
86	Ethernet wake-up		NA
87	HSECSS interrupt		NA
88	Reserved	TEMP wake-up	NA
89	NA	UART9 wake-up	NA
90	NA	USART10 wake-up	NA
91	NA	I2C5 wake-up	NA

Note: For more details about the EXTI event input mapping, refer to EXTI event input mapping section of the RM0433, RM0468, and RM0477 reference manuals.

6.3 Security peripherals

6.3.1 Crypto engines

Different cryptographic operations are available in STM32H7Sx:

Two AES accelerators: One is side-channel attack protected (SAES), while the second is more performance oriented (CRYP).

Three memory cipher engines (MCEs): on-the-fly encryption and decryption on external nonvolatile or volatile memories.

6.3.1.1 Cryptographic processor

The STM32H7Sx, STM32H750, and STM32H730 devices embed a cryptographic processor that supports the advanced cryptographic algorithms usually required to ensure confidentiality, authentication, data integrity and nonrepudiation when exchanging messages.

Table 17 compares the cryptographic processor implementation on STM32H7Sx, STM32H750, and STM32H730 devices

Table 17. Cryptographic processor difference between STM32H7Sx, STM32H750, and STM32H730 devices

-	STM32H750	STM32H730	STM32H7Sx
Features	• Compliant implementation of the following standards: – NIST FIPS publication 46-3, Data Encryption Standard (DES) – ANSI X9.52, Triple DATA Encryption Algorithm Modes op Operation (TDES) – NIST FIP publication 197, Advanced Encryption Standard (AES) • Multiple key sizes and chaining mode: – DES/TDES chaining mode ECB and CBC, supporting standard 56-bit keys with 8-bit parity per key – AES chaining mode ECB, CBCn CTR, CGM, GMAC, CCM for key sizes of 128, 192, or 256 bits		• Compliant implementation of the following standards: – NIST FIPS publication 197, Advanced Encryption Standards (AES) • Multiple key sizes and chaining mode: – AES chaining mode ECB, CBC, CTR, GCM, GMAC, CCM for key sizes of 128, 192, or 256 bits
	• A 32-bit AHB peripheral • Supports DMA transfers for incoming and outgoing data • Includes input and output FIFOs (each eight words deep) for better performance		
	NA		Supports key sharing with SAES co-processor

6.3.1.2 Secure AES co-processor

The STM32H7Sx embeds one secure AES coprocessor (SAES) to encrypts or decrypts data. The SAES is a new feature in STM32H7Sx devices which implements countermeasures and mitigations against power and electromagnetic side-channel attacks. The SAES is not available in STM32H750 and STM32H730 devices.

The SAES peripheral is connected with the TAMP backup registers (BHK – boot hardware key) and with the flash memory interface (AHK - application hardware key). Clocked by the AHB bus clock, the SAES offers very good performance for a DPA resistant hardware accelerator. It shares the key with the CRYP peripheral. The table below compares the Cryp processor to SAES.

Table 18. CRYP versus SAES features

Modes or features(1)	CRYP	SAES
ECB CBC chaining	X	X
CTR, CCM, GCM chaining	X	X
AES 128-bit ECB encryption in cycles	14	480

Modes or features(1)	CRYP	SAES
DHUK and BHK key selection	-	X
Resistance to side-channel attacks	-	X
Shared key between SAES and CRYP	X	X
Key sizes in bits	128, 192, 256	128, 256

1. *X = supported*

The SAES main features are:

- Fully compliant with the advanced encryption standard (AES).
- Encryption and decryption with multiple chaining modes: ECB,CBC,CTR,GCM,GMAC,CCM for key sizes of 128 or 256 bits
- Incorporates a protection against side-channel attacks (SCA), including differential power analysis (DPA)
- Hardware secret key encryption/ decryption (Wrapped-key mode)
- Using a dedicated key bus, optional key sharing with faster CRYP peripheral (shared key mode), controlled by SAES
- Integrated key scheduler to compute the last round key for ECB/CBC decryption
- Security context enforcement for keys
- AMBA AHB slave peripheral accessible through 32-bit single accesses only.
- Supports DMA single transfers for incoming and outgoing data (two DMA channels required).
- Hardware-linked with the true random number generator (TRNG) and with the CRYP peripheral.
- 128-bit of registers for storing initialization vectors (four 32-bit registers)
- 32-bit buffer for data input and output
- Automatic data flow control supporting two
- Data-swapping logic to support 1-, 8-, 16-, or 32-bit data

When an unexpected hardware fault occurs, an output tamper event is triggered, and the SAES automatically clears the key registers. A reset is required for the SAES to be usable again.

6.3.1.3 *Memory cipher engine (MCE)*

STM32H7Sx devices embed three MCEs for on-the-fly encryption (for writing) and decryption (for reading) on external memories. The Table 19 describes the implementation and the main features of MCE1, MCE2, and MCE3 instances.

Note: The MCE is only available on STM32H7Sx. STM32H730 devices embed OTFDEC for external OCTOSPI memories decryption.

Table 19. MCE features

-	MCE1	MCE2	MCE3
External memory interface	XSPI1/2	XSPI1/2	FMC
Cipher engines	AES x2	12 rounds Noekeon x2	
Encryption modes	Block, fast block, stream	Block, fast block	
Number of regions	Four with 4-Kbyte granularity		
Cipher context(s)	2	0	
Derive key function	Normal, fast		
Master key	2		
Features	• Automatic key-erase in case of tamper. • AHB configuration port, privileged aware. • AXI system bus master/slave interfaces (64-bit). • Optimization for XSPI data prefetching mechanism (stream cipher only). • One set of write-only and lockable master key registers per block cipher (normal, fast).		

-	MCE1	MCE2	MCE3
	• For AES, two sets of lockable cipher contexts (128-bit key, IV), usable for stream and block ciphers.		

Note: When MCE is used in conjunction with XSPI, it is mandatory to access the flash memory using the memory map mode of the flash memory controller.

6.3.2 Random number generator (RNG)

The STM32H7Rx/7Sx, STM32H750, and STM32H730 devices embed an RNG that delivers 32-bit random numbers generated by an integrated analog circuit. The table below presents the RNG features of STM32H7Rx/7Sx, STM32H750, and STM32H730 devices.

Table 20. RNG features

-	STM32H750	STM32H730	STM32H7Rx/7Sx
Features	• RNG delivers 32-bit true random numbers. • AHB slave peripheral, accessible through 32-bit word single access only. • Can be used as an entropy source to construct a nondeterministic random bit generator (NDRBG) • Can be disabled to reduce power consumption • Can be enabled with an automatic low-power mode		
	• Can be used as an entropy source to construct NIST compliant deterministic random bit generator (DRBG) • Allows embedded continuous basic health tests with associated error management.	• Is a NIST SP 800-90B compliant entropy source that can be used to construct a nondeterministic random bit generator (NDRBG). • Embeds start-up and NIST SP800-90B approved continuous health tests with specific error management	
	-	-	• Transparently used by SAES and PKA: for key generation and key erase • Entropy enhancement.

6.3.3 Hash processor (HASH)

Table 21 shows the differences between HASH features in STM32H7Rx/7Sx, STM32H750, and STM32H730 devices.

Table 21. HASH features

Hash	STM32H750	STM32H730	STM32H7Rx/7Sx
Features	• Secure HASH algorithm (SHA-1 and SHA-2 family) • Digital signature standard (DSS) • MD5 (message-digest algorithm 5) hash algorithm • HMAC (keyed-hash message authentication code) algorithm		• Secure HASH algorithm (SHA-1, SHA-2 family) • HMAC (keyed-hash message authentication code) algorithm • Digital Signature Standard (DSS)
	Fast computation of SHA-1, SHA-224, SHA-256, and MD5.		Fast computation of SHA-1, SHA2-224, SHA2-256, SHA2-384, and SHA2-512.
	8x 32-bit words (H0 to H7) for output message digest.		8x 32-bit words (H0 to H15) for output message digest.

Hash	STM32H750	STM32H730	STM32H7Rx/7Sx
Features	• Single 32-bit input register associated to an internal input FIFO, corresponding to one block size. • Automatic data flow control supporting direct memory access (DMA) using one channel. • Support for both single and fixed DMA burst transfers of four words. • AHB slave peripheral. • Corresponding 32-bit words of the digest from consecutive message blocks are added to each other to form the digest of the whole message. • Automatic padding to complete the input bit string. • Interruptible message digest computation.		

6.3.4 Public key accelerator (PKA)

The PKA is a new feature in the STM32H7Rx/7Sx devices and is not embedded in the STM32H730 and STM32H750 devices.

All needed computations are performed within the accelerator, so no further hardware/software elaboration is needed to process the inputs or the outputs.

It is intended for the computation of cryptographic public key primitives, specifically those related to RSA, Diffie-Hellmann, or ECC (Elliptic Curve Cryptography) over GF(p) (Galois fields). When manipulating secrets, the PKA incorporates a protection against side-channel attacks (SCA), including differential power analysis (DPA), certified SESIP, and PSA security assurance level 3.

The PKA is an AHB slave peripheral, accessible through 32-bit word single access only and is able to handle operands up to 4160 bits for RSA/DH and 640 bits for ECC.

6.4 Communication peripherals

6.4.1 Improved inter-integrated circuit (I3C)

The STM32H7Rx/7Sx devices implement a new feature compared to STM32H730 and STM32H750 devices, which is the I3C peripherals. An I3C bus is a two-wire, serial single-ended, multidrop bus, intended to improve a legacy I2C bus.

In STM32H7Rx/7Sx devices, I3C is shared with I2C. Refer to the I3C section in the reference manual for more details.

The I3C main features are:

- Support MIPI® I3C specification v1.1.
- I3C SCL bus clock frequency up to 12.5 MHz.
- Registers configuration from the host application via the APB slave port.
- Support queued data transfers and queued control/status transfers.
- Frame-level management and programmable bus timing.
- Target-initiated request management.
- Bus error management.
- Individual programmable event-based management.
- Wake-up from Stop mode as the controller is on an in-band interrupt without payload, on a hot-join request or on a controller-role request.
- Wake-up from Stop mode(s), as the target is on a reset pattern or on a missed start.
- Multiclock domain management.

6.4.2 Controller area network (CAN)

The main differences related to CAN between the STM32H7Rx/7Sx, STM32H750, and STM32H730 devices are presented in Table 22.

Table 22. CAN features

-	STM32H750	STM32H730	STM32H7Rx/7Sx
Features	2 × FDCAN (FDCAN1 supports TTCAN)	3 × FDCAN (FDCAN1 supports TTCAN)	Instances: 2 × FDCAN

-	STM32H750	STM32H730	STM32H7Rx/7Sx
Features	• Conform with CAN protocol version 2.0 part A, B, and ISO 11898-1: 2015, -4. • CAN FD with maximum 64 data bytes supported. • CAN error logging. • AUTOSAR and J1939 support. • Improved acceptance filtering. • Separate signaling on reception of high priority messages. • Configurable transmit FIFO/queue. • Programmable loopback test mode. • Maskable module interrupts. • Two clock domains: APB bus interface and CAN core kernel clock. • Power down support.		
	• TTCAN (11898-4) protocol level 1 and level 2 completely in hardware (FDCAN1 only) • Event synchronized time-triggered communication supported (FDCAN1 only) • Up to 64 dedicated receive buffers • Up to 32 dedicated transmit buffers • 10 Kbytes of shared RAM between instances • Up to 128 filters (11 bits) and 64 (29 bits) shared between instances • Two configurable receive FIFOs • Configurable transmit event FIFO		For each instance: • 3 transmit buffers • 1-Kbyte RAM • 28 filters (11 bits) and 28 filters (29 bits) • Two receive FIFOs • Transmit event FIFO

6.4.3 Universal serial bus interface (USB)

The STM32H7Rx/7Sx devices implement a USB Type-C®/USB power delivery controller (UCPD), a USB OTG full-speed controller with embedded PHY and a USB OTG high-speed controller with embedded PHY that can be used for either full-speed or high-speed operation.

The USB Type-C®/USB power delivery interface can be assigned to one of the two USB controllers. The main features are:

- It is compliant with USB Type-C® specification release 2.3, and USB Power Delivery specifications revision 2.0 and 3.2.
- Stop mode low-power operation support.
- Built-in analog PHY.
- Digital controller.

The STM32H730 devices embed a USB OTG high-speed peripheral that supports both full-speed and high-speed operations. It integrates the transceivers for full-speed operation and a UTMI low-pin interface (ULPI) for high-speed operation. When using the USB OTG_HS interface in HS mode, an external PHY device (also known as a transceiver) is connected to the ULPI.

The STM32H750 devices embed two USB OTG high-speed peripheral: OTG-HS1 supports both full-speed and high-speed operations, while OTG-HS2 supports only full-speed operations. They both integrate the transceivers for full-speed operation. OTG-HS1 features a UTMI low-pin interface (ULPI) for high-speed operation. When using the USB OTG-HS1 in HS mode, an external PHY device (also known as a transceiver) connected to the ULPI is required.

The main USB differences between STM32H7Rx/7Sx, STM32H750, and STM32H730 devices are listed in Table 23.

Table 23. USB OTG implementation in STM32H7Rx/7Sx, STM32H750, and STM32H730 devices

"X" = supported, "-" = not supported, "FS" = supported in FS mode, "HS" = supported in HS mode.

-	STM32H750		STM32H730	STM32H7Rx/7Sx	
Instance	OTG_HS1(1)	OTG_HS2(2)	OTG_HS	OTG_FS	OTG_HS
Device bidirectional endpoints (including EP0)	9		9	6	9
Host mode channels	16		16	12	16
Size of dedicated SRAM	4 Kbytes		4 Kbytes	1.2 Kbytes	4 Kbytes
USB 2.0 link power management (LPM) support	X		X		
OTG revision supported	2.0				
Battery charging detection (BCD) support	X				
Integrated PHY	FS (X1)	FS (X1)	FS (X1)	FS (X1)	HS (X1)
ULPI available to primary IOs via muxing	X1	-	X1	-	
Dedicated digital power supply for OTG_HS DVDD	-		-	-	Yes Connected to VCAP when used, and to GND when not used.
DMA availability	X		X	-	X

1. *OTG_HS1 compatible with high speed operation*
2. *OTG_HS2 is incompatible with high speed operation*

6.5 External memory interface peripherals

6.5.1 Flexible memory controller (FMC)

The STM32H7Rx/7Sx devices implement the same FMC features than STM32H730 and the STM32H750 devices.

The FMC controller main features are the following:

- Interface with static-memory mapped devices including:
  - Static random-access memory (SRAM).
  - NOR flash memory memory/one NAND flash memory.
  - PSRAM (four memory banks).
  - NAND flash memory with ECC hardware to check up to eight Kbytes of data.
- Interface with synchronous DRAM (SDRAM/Mobile LPSDR SDRAM) memories.
- 8, 16, 24-bit data bus width.
- Independent chip select control for each memory bank.
- Independent configuration for each memory bank.
- Write FIFO.
- Read FIFO for SDRAM controller.
- The maximum FMC_CLK/FMC_SDCLK frequency for synchronous accesses is the FMC kernel clock divided by two.

6.5.2 Quad/Octo/Hexa-SPI memory interface

6.5.2.1 *Extended-SPI interface (XSPI)*

The XSPI is a specialized communication interface targeting single, dual, quad, octal, or 16-bit SPI memories. The STM32H7Rx/7Sx devices embed two separate XSPI interfaces. Each XSPI interface supports single/dual/quad/octal and 16-bit SPI formats.

XSPI is relative to the OCTOSPI interface in STM32H730 and to QUADSPI interface in STM32H750. In STM32H750, a single quad SPI memory interface embedded targeting single, dual, or quad-SPI flash memories. All the features supported by QUADSPI are also supported by OCTOSPI.

In STM32H730, two separate OCTOSPI interfaces are embedded. Each OCTOSPI instance supports single/dual/quad/octal SPI formats.

All the features supported by OCTOSPI interface in the STM32H730 devices are also supported by XSPI in the STM32H7Rx/7Sx devices.

The main differences related to this interface between the STM32H7Rx/7Sx and the STM32H730 devices are detailed in Table 24.

Table 24. XSPI difference between STM32H7Rx/7Sx and STM32H730 devices

STM32H730		STM32H7Rx/7Sx
Interface	Two OCTOSPI	Two XSPI
SPI memories	Up to two OCTOSPI memories.	Up to two OCTOSPI memories or one OCTOSPI and 16-bit -SPI memory(1)
Signals interfacing with memory	Up to 12 signals: • NCS • CLK, NCLK • DQS • IO[3:0]: data bus LSB • IO[7:4]: data bus MSB	Up to 22 signals: • NCS1(2), NCS2(2) • CLK, NCLK, • DQS0, DQS1 • IO[3:0]: data bus LSB • IO[7:4]: data bus MSB • IO[15:8]: data bus MSB(1)
Features	NA	• Dual-octal configuration • XSPI mode accessing a single 16-bit memory • High-speed interface • Dual chip select support • Additional DQS for data strobe (DQS0 for D[0:7] and DQS1 for D[8:15]). • Register calibration added in the interface: CALMR / CALSOR / CALSIR.
	• Asynchronous AXI bus clock versus kernel clock. • Dual-quad configuration. • Support for single, dual, quad, and octal communication. • HyperBus standard compliant. • Dual-quad configuration. • Xccela standard compliant. • XSPI (JEDEC251ES) standard compliant. • AMBA® AXI compliant data interface. • Functional modes: indirect, automatic status-polling, and memory-mapped. • Read and write support in memory-mapped mode. • SDR (single-data rate) and DTR (double-transfer rate). • Fully programmable opcode. • Fully programmable frame format. • Support wrapped-type access to memory in read direction. • Integrated FIFO for reception and transmission. • 8, 16, and 32-bit data access. • Interrupt on FIFO threshold, timeout, operation complete, and access error. • Compliant with dual-XSPI arbiter (communication regulation). • Extended CSHT timeout. • Memory-mapped write. • Refresh counter.	

STM32H730	STM32H7Rx/7Sx
Features	• Data strobe support. • DMA protocol support.

1. *Depending on the package and only available on Port 1 of XSPIM manager.*
2. *Only one of these two signals is active at a given moment in time.*

6.5.2.2 *XSPI I/O manager (XSPIM)*

The STM32H7Rx/7Sx devices embed XSPI I/O manager which is a low-level interface that enables an efficient XSPI pin assignment with a full I/O matrix (before alternate function map), and multiplex of single/dual/quad/octal/16-bit SPI interfaces over the same bus.

Up to two interfaces are available where up to 16-bit external memory on the port 1, and up to 8-bit external memory on the port 2 and this depending on the package.

XSPIM is relative to the OCTOSPI I/O manager in the STM32H730 devices with some differences resumed in Table 25. The STM32H750 does not support this peripheral. Most features supported by OCTOSPIM in the STM32H730 devices are also supported by the XSPIM in the STM32H7Rx/7Sx devices.

Table 25. XSPIM difference between STM32H7Rx/7Sx and STM32H730 devices

Feature	STM32H730	STM32H7Rx
Supports up to two single/dual/quad interfaces	Yes	Yes
Fully I/O multiplexing capability	Yes	Yes
Supports time-multiplexed mode	Yes	Yes
Supports high-speed interface	NA	Yes
Chip select selection if XSPI provides dual chip select	NA	Yes
Supports 16-bit data interface and dual-octal mode	NA	Yes(1)
Supply for XSPI I/O manger Port 1/2 ($V_{DDXSPI1}$, $V_{DDXSPI2}$)	NA	Yes

1. *Package dependent.*

6.6 Graphics peripherals

6.6.1 Digital camera interface pixel pipeline (DCMIPP)

The STM32H7Rx/7Sx devices embed a DCMIPP which is the pixel pipeline section of a high-resolution camera subsystem. It gets pixels from a parallel interface, and after some processing (such as decimation, cropping), dumps them to the memory.

A first common part of the DCMIPP selects the input exclusively from the parallel interface. Data go to a dedicated pipeline(s) before they are sent to memory for further processing or display purposes. The DCMIPP main features are the following:

- Pixel rate: up to 16 bits in parallel, 100 Mpixel/s (typically 1080p30, maximum 2048x2048 on processing pipelines after decimation).
- Pixel format: RGB565, RGB888, YUV422, raw Bayer/Mono 8/10/12/14, and ByteStream (JPEG)
- Programmable polarity for the input pixel clock and synchronization signals
- Parallel data communication can be 8-, 10-, 12-, 14- or 16-bit
- Supports continuous mode or snapshot (a single frame) mode
- Capability to automatically crop the image

The digital camera interface (DCMI) is available for STM32H730 and STM32H750 devices.

For more details about DCMIPP, refer to the DCMIPP section of the RM0477 reference manual

6.6.2 Chrom-ART Accelerator (DMA2D)

The DMA2D is available on the STM32H7Rx/7Sx, STM32H750, and STM32H730 devices. The DMA2D main features are the following:

- Single AXI master bus architecture.
- AHB slave programming interface supporting 8/16/32-bit accesses (except for CLUT accesses, which are 32-bit).
- User programmable working area size.
- User programmable offset for sources and destination areas.
- User programmable sources and destination addresses on the whole memory space.
- Up to two sources with blending operation.
- Alpha value can be modified (source value, fixed value, or modulated value).
- User programmable source and destination color format.
- Up to 12 color formats supported from 4-bit up to 32-bit per pixel with indirect or direct color coding.
- Block based (8x8) YCbCr support with 4:4:4, 4:2:2 and 4:2:0 chroma subsampling factors.
- Two internal memories for CLUT storage in indirect color mode.
- Automatic CLUT loading or CLUT programming via the CPU.
- User programmable CLUT size.
- Internal timer to control AXI bandwidth.
- Operating modes:
  - Register-to-memory
  - Memory-to-memory
  - Memory-to-memory with pixel format conversion
  - Memory-to-memory with pixel format conversion and blending
  - Memory-to-memory with pixel format conversion, blending and fixed color foreground
  - Memory-to-memory with pixel format conversion, blending and fixed color background.
- Area filling with a fixed color.
- Copy from an area to another.
- Copy with pixel format conversion between source and destination images.
- Copy from two sources with independent color format and blending.
- Output buffer byte swapping to support refresh of displays through a parallel interface.
- Abort and suspend of DMA2D operations.
- Watermark interrupt on a user-programmable destination line.
- Interrupt generation on bus error or access conflict.
- Interrupt generation on process completion.

6.6.3 Neo-Chrom graphic processor GPU2D

The STM32H7Rx/7Sx devices embed a GPU2D. The GPU2D is a dedicated graphics processing unit accelerating numerous 2.5D graphics applications such as graphical user interface (GUI), menu display or animations.

The GPU2D is not available on the STM32H730 and STM32H750 devices. The following table describes the GPU2D features on STM32H7Rx/7Sx. For more information about GPU2D, refer to the GPU2D section of the product reference manual.

Table 26. GPU2D features

Features	STM32H7Rx/7Sx
-	• Multi-threaded fragment processing core with a VLIW (very-long instruction word) instruction set. • Fixed point functional units. • Command list based DMAs to minimize CPU overhead. • Two 64-bit AXI master interfaces for texture and frame buffer access. • Dedicated 64-bit AXI master interface for command list. • 32-bit AHB slave interface for register bank access.

Features	STM32H7Rx/7Sx
	• Up to four general-purpose flags for system-level synchronization. • Texture decompression unit with TSC™4 and TSC™6/TSC™6a support.
2D drawing features	• Pixel/line drawing. • Filled rectangles. • Triangles, quadrilateral drawing. • Anti-aliasing 8xMSAA (multi-sample anti-aliasing).
Image transformations	• 3D perspective correct projections. • Texture mapping with bilinear filtering or point sampling.
Blit support	• Rotation, mirroring, stretching (independently on x and y axis). • Source and/or destination color keying. • Pixel format conversions.
Text rendering support	• A1, A2, A4, and A8 bitmap anti-aliased. • Subsampled anti-aliased.
Color formats	• ABGR8888, ARGB8888, BGRA8888, RGBA8888 • xBGR8888, xRGB8888, BGRx8888, RGBx8888, RGB888, BGR888 • BGR565, RGB565 • RGB322, BGR322 • TSC4, TSC6, TSC6A • L1, L2, L4, L8 (grayscale) • A1, A2, A4, A8
Full alpha blending with hardware blender	• Programmable blending modes. • Source/destination color keying.

6.6.4 JPEG codec (JPEG)

The JPEG codec is only available on the STM32H7Rx/7Sx and STM32H750 devices. It can encode and decode a JPEG stream as defined in the ISO/IEC10918-1 specification. It provides a fast and simple hardware compressor and decompressor of JPEG images with full management of JPEG headers. The JPEG codec main features are the following:

- High-speed fully synchronous operation.
- Configurable as encoder or decoder.
- Single-clock-per-pixel encode/decode.
- RGB, YCbCr, YCMK, and BW (grayscale) image color space support.
- 8-bit depth per image component at encode/decode.
- JPEG header generator/parser with enable/disable.
- Four programmable quantization tables.
- Single-clock Huffman coding and decoding.
- Fully programmable Huffman tables (two AC and two DC).
- Fully programmable minimum coded unit (MCU).
- Concurrent input and output data stream interfaces.

6.6.5 Chrom-GRC (GFXMMU)

The GFXMMU is only available on the STM32H7Rx/7Sx devices. The GFXMMU is a graphical oriented memory management unit aimed at:

- Optimizing memory usage according to the display shape.
- Up to four virtual buffers.
- Packing and unpacking operation to store 32-bit pixel data into 24-bit packed.

A virtual memory space is provided that is visible to all system masters and can be physically mapped to any system memory. An interrupt can be generated in case of a buffer overflow or memory transfer error.

For more information about GFXMMU, refer to the Chrom-GRC (GFXMMU) section of the RM0477 reference manual.

6.6.6 LCD-TFT display controller (LTDC)

The STM32H7Rx/7Sx, STM32H730 and STM32H750 devices embed an LCD-TFT (liquid crystal display - thin film transistor) display controller with the same basic features. The controller provides a 24-bit parallel digital RGB (Red, Green, Blue), and delivers all signals to interface directly to a broad range of LCD and TFT panels up to XGA (1024x768) resolution with the following main features:

- Two display layers with dedicated FIFO (64x32-bit).
- Color look-up table (CLUT) up to 256 colors (256x24-bit) per layer.
- Up to eight input color formats selectable per layer.
- Flexible blending between two layers using alpha value (per pixel or constant).
- Flexible programmable parameters for each layer.
- Color keying (transparency color).
- Up to four programmable interrupt events.
- AXI master interface with burst of 16 words.

Revision history

Table 27. **Document revision history**

Date	Version	Changes
11-Mar-2024	1	Initial release.
12-Jun-2024	2	Updated: • Section 2: STM32H7Rx/7Sx MCUs overview • Figure 1. STM32H7Rx/7Sx devices system architecture
12-Dec-24	3	Updated: • Figure 1. STM32H7Rx/7Sx devices system architecture • Figure 4. System supply configuration on STM32H7Rx/7Sx

Contents

1 General information 2
2 STM32H7Rx/7Sx MCUs overview 3
3 System architecture differences between STM32H7Rx/7Sx, STM32H730, and STM32H750 devices 5
4 Hardware migration 9
4.1 Package availability 9
4.2 Pinout compatibility 9
5 Boot mode compatibility 10
5.1 Boot mode selection 10
5.2 System bootloader 10
6 Peripheral migration 12
6.1 Cross-compatibility between STM32 products 12
6.2 System peripherals 14
6.2.1 Embedded flash memory (FLASH) 14
6.2.2 SRAMs 15
6.2.3 Direct memory access controller (DMA) 16
6.2.4 Reset and clock control (RCC) 17
6.2.5 Power (PWR) 18
6.2.6 General-purpose I/Os (GPIO) 22
6.2.7 Extended interrupt and event controller (EXTI) 22
6.3 Security peripherals 26
6.3.1 Crypto engines 26
6.3.2 Random number generator (RNG) 28
6.3.3 Hash processor (HASH) 28
6.3.4 Public key accelerator (PKA) 29
6.4 Communication peripherals 29
6.4.1 Improved inter-integrated circuit (I3C) 29
6.4.2 Controller area network (CAN) 29
6.4.3 Universal serial bus interface (USB) 30
6.5 External memory interface peripherals 31
6.5.1 Flexible memory controller (FMC) 31
6.5.2 Quad/Octo/Hexa-SPI memory interface 32
6.6 Graphics peripherals 33
6.6.1 Digital camera interface pixel pipeline (DCMIPP) 33
6.6.2 Chrom-ART Accelerator (DMA2D) 34

6.6.3 Neo-Chrom graphic processor GPU2D 34
6.6.4 JPEG codec (JPEG) 35
6.6.5 Chrom-GRC (GFXMMU) 35
6.6.6 LCD-TFT display controller (LTDC) 36
Revision history 37
List of tables 40
List of figures 41

List of tables

Table 1. Applicable products . . . 1
Table 2. Security and graphics IP availability per product line . . . 4
Table 3. Available bus matrix on STM32H7Rx/7Sx, STM32H730, and STM32H750 devices . . . 5
Table 4. Available packages on STM32H7Rx/7Sx, STM32H730, and STM32H750 devices . . . 9
Table 5. Boot modes for STM32H730 and STM32H750 . . . 10
Table 6. Boot modes for STM32H7Rx/7Sx . . . 10
Table 7. STM32H7Rx/7Sx, STM32H730, and STM32H750 devices bootloader communication peripherals . . . 10
Table 8. Peripheral summary for STM32H7Rx/7Sx, STM32H730, and STM32H750 devices . . . 12
Table 9. Flash memory differences . . . 14
Table 10. Comparison of RAM size between STM32H7Rx/7Sx, STM32H730, and STM32H750 devices . . . 16
Table 11. DMA features . . . 16
Table 12. RCC features . . . 17
Table 13. Peripheral clock distribution example . . . 18
Table 14. PWR controller differences between the STM32H7Rx/7Sx, STM32H730 and STM32H750 devices . . . 19
Table 15. EXTI features . . . 23
Table 16. EXTI line differences . . . 24
Table 17. Cryptographic processor difference between STM32H7Sx, STM32H750, and STM32H730 devices . . . 26
Table 18. CRYP versus SAES features . . . 26
Table 19. MCE features . . . 27
Table 20. RNG features . . . 28
Table 21. HASH features . . . 28
Table 22. CAN features . . . 29
Table 23. USB OTG implementation in STM32H7Rx/7Sx, STM32H750, and STM32H730 devices . . . 31
Table 24. XSPI difference between STM32H7Rx/7Sx and STM32H730 devices . . . 32
Table 25. XSPIM difference between STM32H7Rx/7Sx and STM32H730 devices . . . 33
Table 26. GPU2D features . . . 34
Table 27. Document revision history . . . 37

List of figures

Figure 1. STM32H7Rx/7Sx devices system architecture . . . 6
Figure 2. STM32H730 devices system architecture . . . 7
Figure 3. STM32H750 devices system architecture . . . 8
Figure 4. System supply configuration on STM32H7Rx/7Sx . . . 20
Figure 5. System supply configuration on STM32H730 . . . 21
Figure 6. System supply configuration on STM32H750 . . . 21
Figure 7. EXTI block diagram on STM32H7Rx/7Sx . . . 23