Migrating from STM32F446 to STM32H523/533 MCUs

Introduction

The designers of STM32 microcontroller applications must have the possibility to easily replace one microcontroller type with another one from the same product family or products from a different family. The reasons for migrating an application to a different microcontroller can be for example:

- To fulfill higher product requirements, extra demands on memory size, or an increased number of I/Os.
- To meet cost reduction constraints that require a switch to smaller components and shrink the PCB area.

This application note details the steps required to migrate from an existing design based on the STM32F446 MCUs to one based on the STM32H523/533 MCUs.

This document provides the full set of features available for the STM32F446 devices, and the equivalent features on the STM32H523/533 product lines. This document also provides guidelines on both hardware and peripheral migration.

To better understand the information inside this application note, the user must be familiar with the STM32 microcontroller family.

This application note is a complement to the STM32F446 and STM32H523/533 datasheets and reference manuals. For additional information, refer to the product datasheets and reference manuals.

1 General information

STM32F446 and STM32H523/533 MCUs are 32-bit microcontrollers based on the Arm® Cortex® processor.

Note: Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

Table 1. Reference documents

Document number	Title
[1]	*STM32F446xx advanced Arm®-based 32-bit MCUs* reference manual (RM0390)
[2]	*STM32H523/33, STM32H562/63, and STM32H573 Arm®-based 32-bit MCUs* reference manual (RM0481)
[3]	*Arm® Cortex®-M4 32-bit MCU+FPU, 225 DMIPS, up to 512 KB Flash/128+4 KB RAM, USB OTG HS/FS, seventeen TIMs, three ADCs and twenty communication interfaces* datasheet (DS10693)
[4]	Arm® Cortex®-M33 32-bit MCU+TrustZone®+FPU, 375 DMIPS 250 MHz, 512-Kbyte flash memory, 272-Kbyte RAM, math accelerators datasheet (DS14539 and DS14540)

2 STM32H523/533 MCUs overview

2.1 Main features

STM32H523/533 MCUs include a larger set of peripherals, with more advanced features compared to STM32F446 MCUs.

Some of the new peripherals for STM32H523/533 are:

- Security
  - TrustZone®-aware and securable peripherals
  - Active tamper, secure firmware installation, secure firmware upgrade support, and secure data storage with hardware unique key
  - Preconfigured immutable root of trust (ST-iROT)
  - Flexible life cycle scheme with secure debug authentication
  - Up to eight configurable SAU regions
  - Additional encryption accelerator engine
    - Advanced encryption hardware accelerator (AES)
    - Public key accelerator (PKA)
    - Secure AES coprocessor (SAES)
    - On-the-fly decryption engine on OCTOSPI (OTFDEC)
- Performance
  - Frequency up to 250 MHz
  - Direct access to flash interface through ICACHE
  - ICACHE for internal and external memories
  - DCACHE for external memories
- New communication interface
  - I3C, FDCAN, LPUART, USB Type-C® connector/USB power delivery interface (UCPD), PSSI

Note: This document only manages the differences between STM32F446 and STM32H523/533 for the common features. The new features of STM32H523/533, mainly linked to TrustZone® support, are not covered. The detailed list of available features and packages for each product is available in the respective product datasheets.

The table below summarizes the memory availability of the STM32F446 and STM32H523/533 MCUs.

Table 2. Memory availability

Products	Flash memory		RAM size (Kbytes)				Feature level
	Size	Dual bank	SRAM1	SRAM2	SRAM3	BKPSRAM	
STM32H533	Up to 512 Kbytes	Yes	128	80	64	2	With hardware crypto: AES, PKA, SAES, and OTFDEC
STM32H523	Up to 512 Kbytes	Yes	128	80	64	2	Without hardware crypto
STM32F446	Up to 512 Kbytes	No	112	16	NA	4	NA

2.2 System architecture

The STM32H523/533 MCUs embed:

- High-speed memories: 512 Kbytes of dual bank flash memory and 272 Kbytes of SRAM.
- A flexible external memory controller (FMC) for devices with packages of 100 pins and more.
- One Octo-SPI memory interface (one Octo-SPI available on all packages) and an extensive range of enhanced I/Os and peripherals connected to three APB buses.
- Three AHB buses and a 32-bit multi-AHB bus matrix.

The following table illustrates the bus matrix differences between STM32F446 and STM32H523/533.

Table 3. Bus matrix

Bus type	STM32F446	STM32H523/533
AHB bus matrix masters	**Up to 7 masters**: CPU I-bus, D-bus and S-bus, DMA1 memory bus, DMA2 memory bus, DMA2 peripheral bus, USB OTG_HS DMA bus	**Up to 11 masters**: Fast C-bus, slow C-bus, CPU S-bus for internal memories, CPU S-bus for external memories, GPDMA1 (featuring two controller ports), GPDMA2 (featuring two controller ports), SDMMC1
AHB bus matrix slaves	**Up to 7 slaves**: Internal flash memory ICode bus, internal flash memory DCode bus, SRAM1, SRAM2, AHB1 peripherals (including AHB to APB bridges and APB peripherals), AHB2 peripherals, FMC/ QUADSPI	**Up to 10 slaves**: Internal flash memory, SRAM1, SRAM2, SRAM3, AHB1 peripherals (including APB1 and APB2), backup RAM, AHB2 peripherals, FMC, OCTOSPI, AHB3 peripherals, AHB4 peripherals

The bus matrix provides access from a controller to a target, enabling concurrent access and efficient operations even when several high-speed peripherals work simultaneously.

The figures below show the system architectures of STM32F446 and STM32H523/533.

Figure 1. STM32F446 system architecture

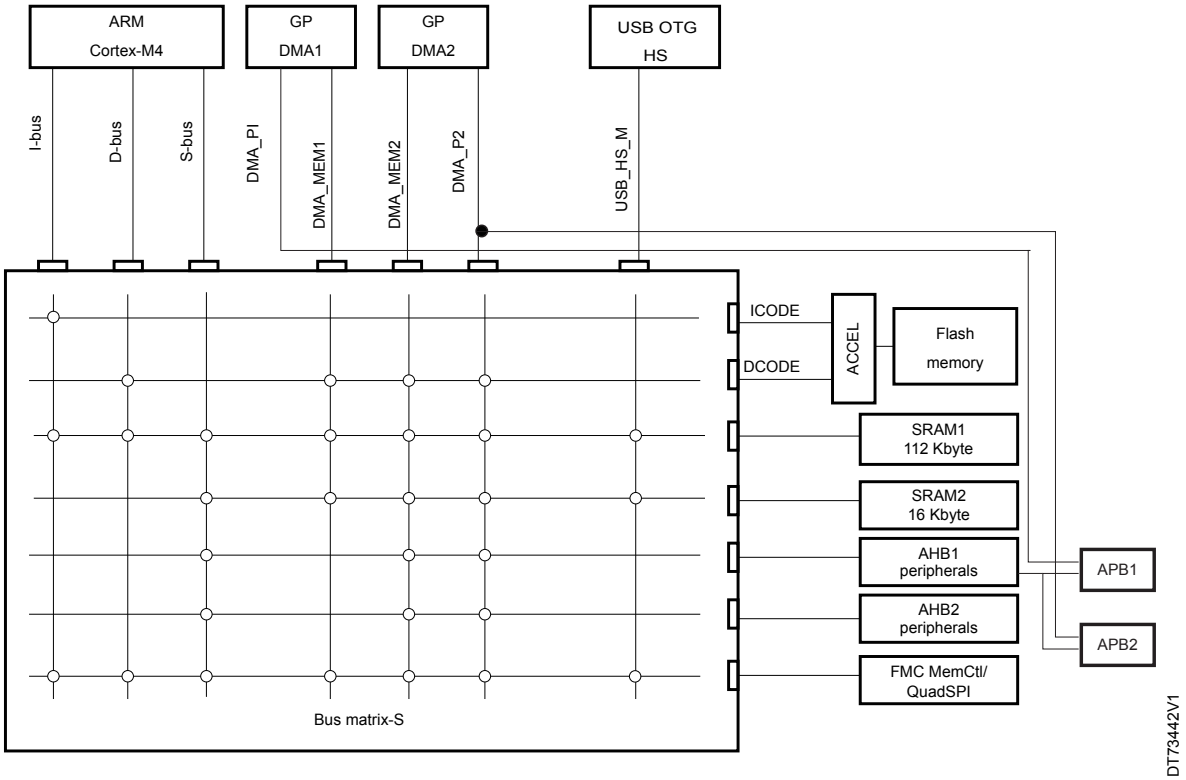
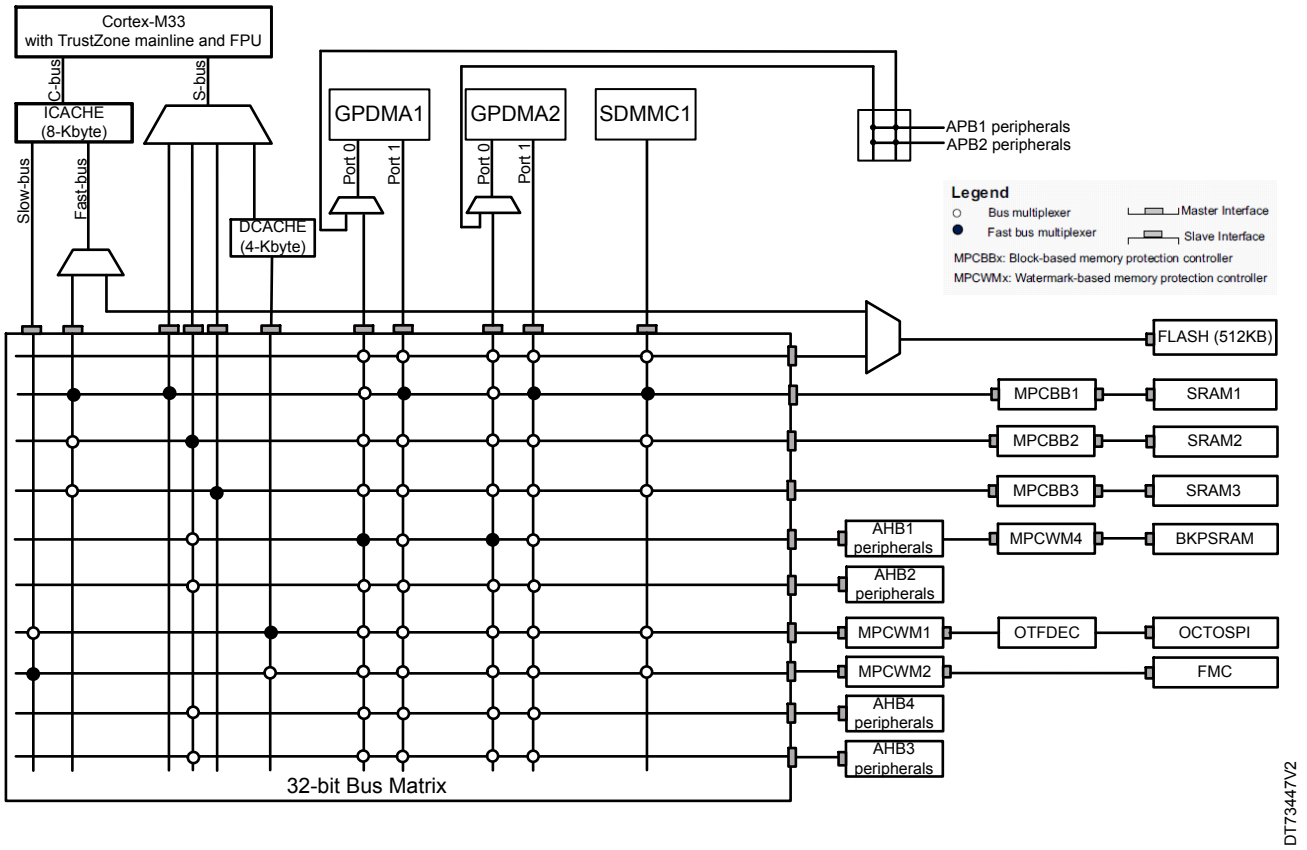


Figure 2. **STM32H523/533 system architecture**



3 Hardware migration

This section presents the package and pinout compatibility details for the hardware migration.

3.1 Package availability

STM32H523 and STM32H533 devices offer eight packages from 39 to 144 pins.

The table below lists the available packages on STM32H523 and STM32H533 devices compared to STM32F446 devices.

Table 4. Available packages

Package(size in mm x mm)	STM32F446	STM32H523/533
LQFP144 (20 x 20 mm)	X	X
LQFP100 14 x 14 mm)	X	X
LQFP64 (10 x 10 mm)	X	X
LQFP48 (7 x 7 mm)	NA	X
UFBGA144 (10 x 10 mm, 0,80 mm pitch)	X	X
UFBGA144 (7 x 7 mm, 0,50 mm pitch)	X	NA
UFBGA100 (7 x 7 mm, 0,50 mm pitch)	NA	X
UFQFPN48 (7 x 7 mm)	NA	X
WLCSP	WLCSP81	WLCSP39

1. *X = available, NA = not available*

3.2 Pinout compatibility

STM32F446 devices are not identical to STM32H523/533 devices in terms of MCU port assignment to package terminals, that is, in terms of pinout. This holds for all common package types of the packages listed in Table 4. Available packages.

For the LQFP144 package, in STM32H523/533 devices, the VCAP_1 and VCAP_2 pins are replaced with a VSS and VDDUSB pin, respectively.

The following sections show the packages pinout figures and difference tables.

3.2.1 LQFP100 package

Figure 3. **STM32H523/533 LQFP100 pinout**

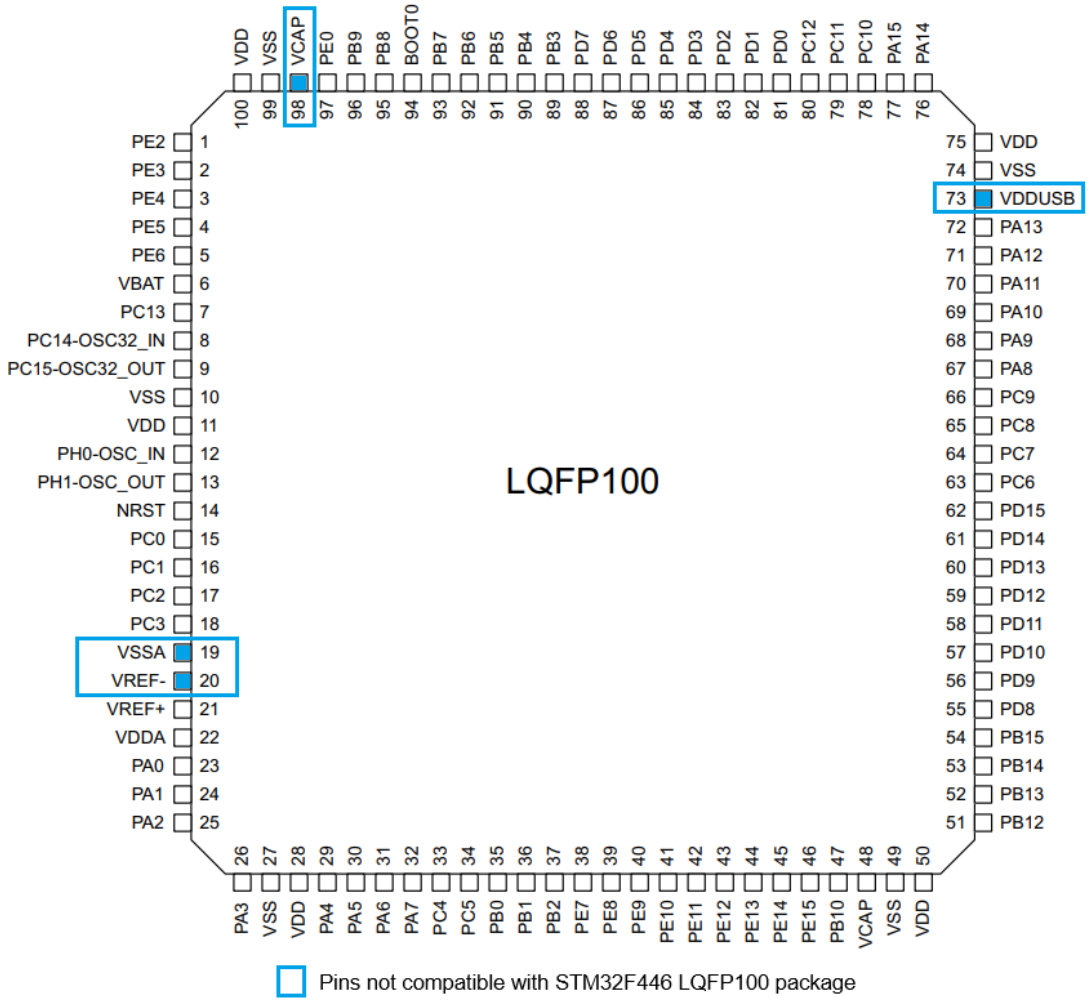


Table 5. **LQFP100 pinout differences**

LQFP100 pin number	STM32F446 pinout	STM32H523/533 pinout
19	VDD	VSSA
20	VSSA/VREF-	VREF-
73	VCAP_2	VDDUSB
98	PE1	VCAP

3.2.2 LQFP144 package

Figure 4. **STM32H523/533 LQFP144 pinout**

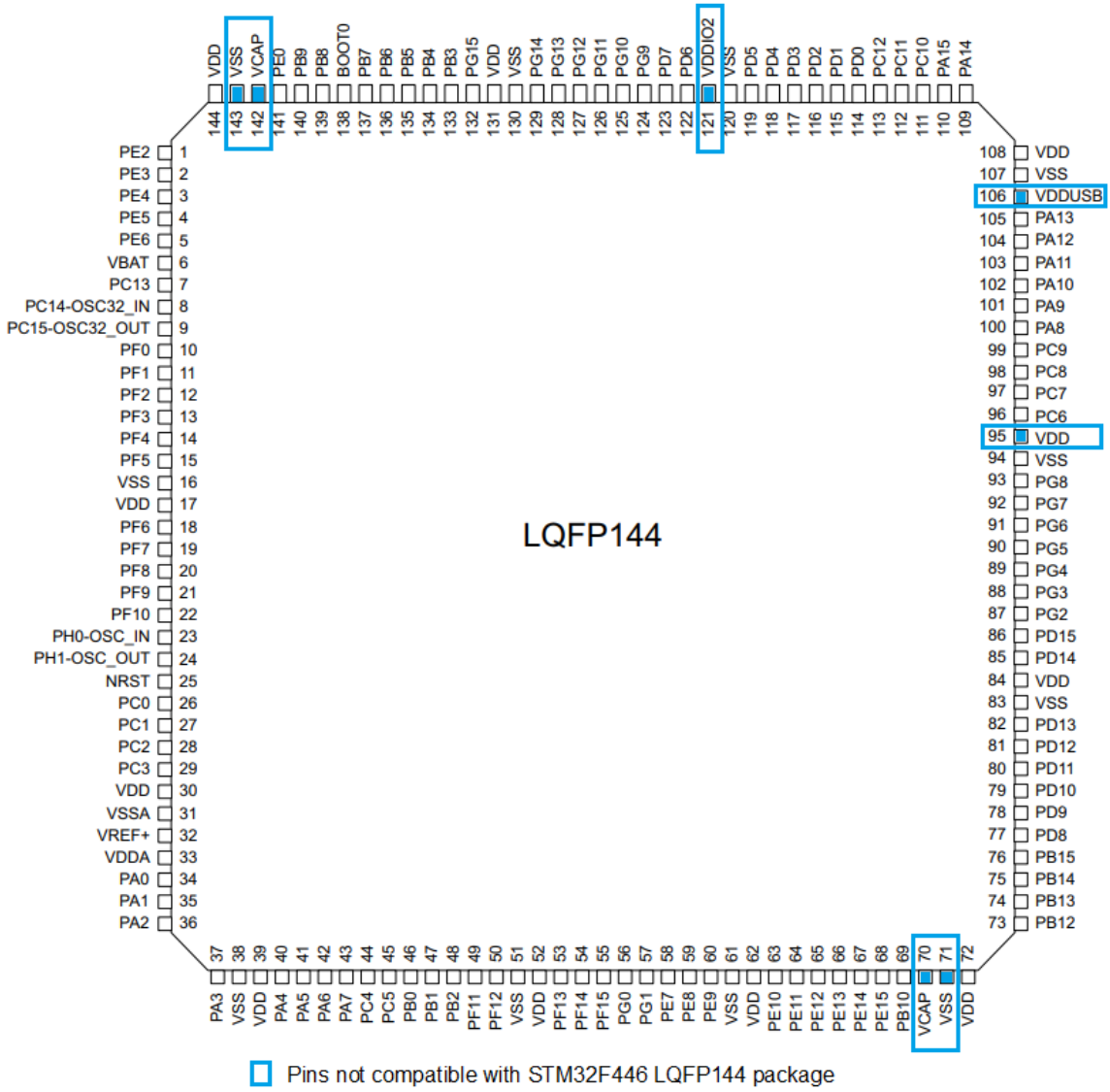


Table 6. **LQFP144 pinout differences**

LQFP144 pin number	STM32F446 pinout	STM32H523/533 pinout
70	PB11	VCAP
71	VCAP_1	VSS
95	VDDUSB	VDD
106	VCAP_2	VDDUSB
121	VDD	VDDIO2
142	PE1	VCAP
143	PDR_ON	VSS

3.2.3 LQFP64 package

Figure 5. **STM32H523/533 LQFP64 pinout**

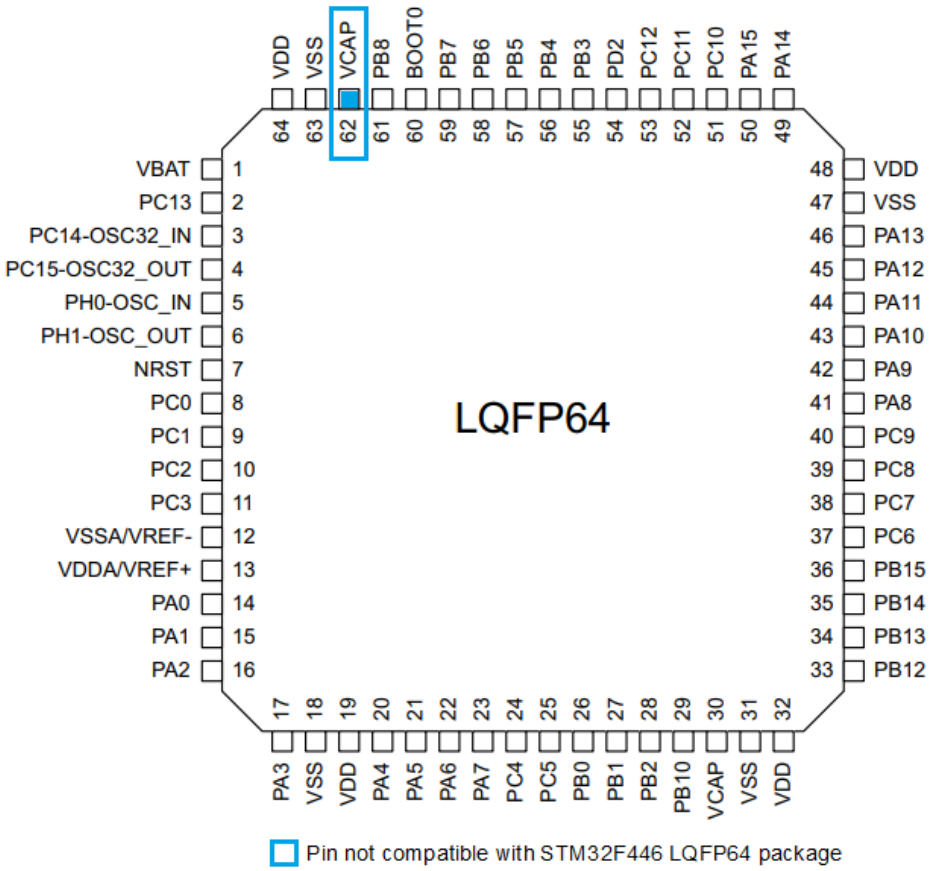


Table 7. **LQFP64 pinout differences**

LQFP64 pin number	STM32F446 pinout	STM32H523/533 pinout
62	PB9	VCAP

3.2.4 UFBGA144 package

For the UFBGA144 package, STM32F446 devices are not compatible with STM32H523/533 devices.

4 Boot mode compatibility

4.1 Boot mode selection

In STM32F446, three different boot modes can be selected through the BOOT[1:0] pins as shown in the table below.

Table 8. Boot modes for STM32F446

Boot mode selection pins		Boot mode	Aliasing
BOOT1	BOOT0		
X	0	Main flash memory	The main flash memory is selected as the boot space.
0	1	System memory	The system memory is selected as the boot space.
1	1	Embedded SRAM	The embedded SRAM is selected as the boot space.

STM32H523/533 embed an SBS peripheral that controls boot and security features. For these devices, the main boot control actions are listed below:

- Run the product with or without TrustZone® enabled.
- Choose between ST-iROT or OEM-iROT (refer to the reference manual for more details).
- Boot when launching a debug authentication sequence.
- Select boot between the bootloader or the user flash memory boot.
- Initialize the HDPL boot value.

For STM32H523/533 devices, the boot configurations are chosen based on the product settings:

- **BOOT0**: to select booting on user flash memory or RSS (root secure services).
- **BOOT_UBE**: option byte to select the iROT between ST-iROT and OEM-iROT.
- **TZEN**: option byte to activate/deactivate the TrustZone®.
- **sbs_boot_addresses**: list of addresses defined by the flash memory:
  - NSBOOTADD: nonsecure boot address
  - SECBOOTADD: secure boot address
- **PRODUCT_STATE**: option byte to activate the different security mechanisms depending on the product use.
- **sbs_dbg_req:** used to launch the debug authentication protocol when booting.

The tables below present the STM32H533 boot modes, with TrustZone® either disabled or enabled.

Table 9. STM32H533 boot modes when TrustZone® is disabled (TZEN=0xC3)

PRODUCT_STATE	BOOT0 pin	BOOT_UBE FLASH_OPTSR[29:22]	Boot address option-byte selection	Boot area	STMicroelectronics default programmed value
Open	0	NA	NSBOOTADD[31:8]	Boot address defined by user option byte NSBOOTADD[31:8]	Flash: 0x0800 0000
	1	NA	NA	Bootloader	Bootloader
Provisioning	x	NA	NA	RSS	RSS
Provisioned, Closed, Locked	x	NA	NSBOOTADD[31:8]	Boot address defined by user option byte NSBOOTADD[31:8]	Flash: 0x0800 0000

Table 10. STM32H533 boot modes when TrustZone® is enabled (TZEN=0xB4)

PRODUCT_STATE	BOOT0 pin	BOOT_UBE FLASH_OPTSR[29:22]	Boot address option-byte selection	Boot area	STMicroelectronics default programmed value
Open	0	x	SECBOOTADD[31:8]	Boot address defined by user option byte SECBOOTADD[31:8]	Flash: 0x0C00 0000
	1	0xB4	NA	Bootloader	Bootloader
	1	0xC3	NA	ST-iROT	ST-iROT
Provisioning	x	NA	NA	RSS	RSS
Provisioned, TZ_Closed, Closed, Locked	x	0xC3	ST-iROT	ST-iROT	ST-iROT
	x	0xB4	SECBOOTADD[31:8]	Boot address defined by user option byte SECBOOTADD[31:8]	Flash: 0x0C00 0000

The tables below illustrate the STM32H523 boot modes, with TrustZone® either disabled or enabled.

Table 11. STM32H523 boot mode when TrustZone® is disabled (TZEN=0xC3)

PRODUCT_STATE	BOOT0 pin	Boot address option-byte selection	Boot area	STMicroelectronics default programmed value
Open	0	NSBOOTADD[31:8]	Boot address defined by user option byte NSBOOTADD[31:8]	Flash: 0x0800 0000
	1	NA	Bootloader	Bootloader
Provisioning	x	NA	RSS	RSS
Provisioned, Closed, Locked	x	NSBOOTADD[31:8]	Boot address defined by user option byte NSBOOTADD[31:8]	Flash: 0x0800 0000

Table 12. STM32H523 boot mode when TrustZone® is enabled (TZEN=0xB4)

PRODUCT_STATE	BOOT0 pin	Boot address option-byte selection	Boot area	STMicroelectronics default programmed value
Open	0	SECBOOTADD[31:8]	Boot address defined by user option byte SECBOOTADD[31:8]	Flash: 0x0C00 0000
	1	NA	Bootloader	Bootloader
Provisioning	x	NA	RSS	RSS
Provisioned, TZ_Closed, Closed, Locked	x	SECBOOTADD[31:8]	Boot address defined by user option byte SECBOOTADD[31:8]	Flash: 0x0C00 0000

4.2 System bootloader

The system bootloader is located in the system memory, programmed by STMicroelectronics in production.

It is used to reprogram the flash memory using one of the serial interfaces.

The following table shows the supported communication peripherals by the system bootloader. For more details, refer to the application note *STM32 microcontroller system memory boot mode* (AN2606).

Table 13. Bootloader communication peripherals

System bootloader peripherals	STM32F446xx I/O pin	STM32H523/533 I/O pin
DFU[1]	PA11/PA12	
USART1	PA10/PA9	
USART2	NA	PA3/PA2
USART3	PB10/PB11 and PC10/PC11	PD9/PD8[2]
CAN	CAN2 (PB5/PB13)	FDCAN2(PB5/PB13)[3]
I2C1	PB6/PB9	PB8/PB9[4]
I2C2	PF1/PF0	NA
I2C3	PA8/PC9	PA8/PC9[5]
I3C1	NA	PB6[6]/PB7
SPI1	PA7/PA6/PA5/PA4	PA7/PA6/PA5/PA4
SPI2	PB15/PB14/PC7/PB12	PC1[7]/PB14/PB10/PB12
SPI3	NA	PC12/PC11/PC10/PA15[4]
SPI4	PE14/PE13/PE12/PE11	NA

1. *On STM32H5, the USB DFU bootloader does not need an external quartz. It uses internal HSI48.*
2. *Only for LQFP100, LQFP144, UFBGA144 and UFBGA100*
3. *On STM32H5xx, the FDCAN bootloader does not use an external quartz. It uses HSI and PLL.*
4. *Not available for LQFP48, UFQFN48, WLCSP39*
5. *PC9 is replaced by PB4 on LQFP48, UFQFN48 and WLCSP39*
6. *PB6 is replaced by PB8 on LQFP48, UFQFN48 and WLCSP39*
7. *PC1 is replaced by PB15 on LQFP48, UFQFN48 and WLCSP39*

5 Peripheral migration

5.1 Cross compatibility between STM32 products

STM32 microcontrollers embed a set of peripherals that can be classified in the following groups:

- Group 1: peripherals common to all products by definition.
  These peripherals are identical, so they have the same structure, registers, and control bits. There is no need to perform any firmware changes to keep the same functionality at the application level after migration. All features and behaviors remain the same.
- Group 2: peripherals shared by all products, but with minor differences (to support new features, in general).
  The migration from one product to another is easy and does not require any significant new development efforts.
- Group 3: peripherals that have considerable changes from one product to another (new architecture or new features, for example).
  For this group of peripherals, the migration requires a new development at the application level.

For STM32H523/533, all of the following can be configured as trusted or untrusted: each GPIO or peripheral, DMA channel, clock configuration register, ICACHE, DCACHE, and small part of the flash memory or SRAM. The following table summarizes the available peripherals in STM32F446 compared to STM32H523/533.

Table 14. STM32 peripheral compatibility between products

Peripherals		STM32F446(1)	STM32H523/533(1)
Core		Cortex®-M4	Cortex®-M33 with TrustZone® mainline and FPU
ST immutable Root Of Trust (STiROT)		No	Yes
Maximum CPU frequency		Up to 180 MHz	Up to 250 MHz
Flash memory		Up to 512 Kbytes	Up to 512 Kbytes, with high-data-cycle capability
SRAMs	System	128 Kbytes (112+16)	272 Kbytes (128+80 (w/ECC)+64)
	Backup	4 Kbytes	2 Kbytes
Timers	General purpose	2 (32 bits) and 8 (16 bits)	2 (32 bits) and 4 (16 bits)
	Advanced control	2(16 bits)	2 (16 bits)
	Basic	2 (16 bits)	2 (16 bits)
	Low power(2)	No	2 (16 bits)
	SysTick timer	1	2
	Watchdog timers (independent, window)	2	2
Communication interfaces	**SPI/I2S**	Up to 4 SPIs, 3 with muxed full-duplex I2S	Up to 4 SPIs, including three muxed full-duplex I2S, and up to 4 additional SPIs from 3xUSART when configured in Synchronous mode (one additional SPI with Octo-SPI)
	I2C	Up to 4 I2C interfaces (SMBus/PMBus)	3 (Sm, Fm, and Fm+ interfaces (SMBus/PMBus)
	I3C(2)	No	2
	USART/UART	4/2	4/2
	LPUART(2)	No	1
	USB	USB OTG_FS and USB OTG_HS	USB FS

Peripherals		STM32F446[1]	STM32H523/533[1]
Communication interfaces	UCPD [2]	No	Yes
	CAN	2	2 FDCAN[2]
	SAI	2	No
	SDIO	1	1
	DCMI	Yes	Yes
	PSSI[2]	No	Yes
	SPDIFRX	Yes	No
Flexible memory controller (FMC)		Yes (8-, 6-bit data bus width); with SDRAM	Yes (8-, 16-bit data bus width); no SDRAM
Octo-SPI[2]		No	1
Quad SPI memory interface (Quad-SPI)		Yes	Yes (Octo-SPI in quad-mode)
HDMI-CEC		Yes	Yes
CRC		Yes	Yes
DMA		DMA1-DMA2 (8 streams each)	2 GPDMA [2](featuring two controller ports), TrustZone® support/linked-list
Real-time clock (RTC)		Yes	Yes
Random number generator (RNG)		No	Yes
SAES, AES[2]		No	Yes
Public key accelerator[2] (PKA)		No	Yes
HASH (SHA-512)		No	Yes
On-the-fly decryption engine[2] (OTFDEC)		No	Yes[3]
GPIOs		Up to 114	Up to 112
ADC (12 bits)	Count	3 (12-bit ADC 2.4 MSPS and 7.2 MSPS in triple interleaved mode); up to 24 channels	2 (12-bit ADC with up to 5 MSPS); up to 20 channels
DAC (12 bits)	Count	1 (two channels)	1 (two channels)
Digital temperature sensor		No	Yes
Operating temperatures		Ambient temperature: : -40 to +85°C /-40 to +105°C Junction temperature: -40 to +125°C	Ambient operating temperature: -40 to +85°C/-40 to +125°C Junction temperature: -40 to +130°C
Operating voltage		1.7 to 3.6 V	1.71 to 3.6 V
Internal voltage reference buffer		No	Yes

1. *For more details, refer to the product datasheets.*
2. *New versus STM32F446.*
3. *Only for STM32H533xx devices.*

5.2 Migration of system peripherals

5.2.1 Embedded flash memory (FLASH)

The following table compares the flash memory interface on STM32F446 and STM32H523/533 devices.

Table 15. FLASH features

Flash memory	STM32F446	STM32H523/533
Main/program memory	• Up to 512 Kbytes • 4 sectors of 16 Kbytes • 1 sector of 64 Kbytes • 3 sectors of 128 Kbytes	• Up to 512 Kbytes (dual bank) • Flash memory read operations supporting multiple lengths: 128 bits, 64 bits, 32 bits, 16 bits, or one byte • 8 Kbytes sector erase, bank erase and dual-bank mass erase
Dual bank	No	Read while write (RWW) and flash bank swapping
Error code correction (ECC)	No	One error detection/correction or two error detections per 128-bit flash memory word using 9 ECC bits
Wait states	Up to 8 (depending on the supply voltage and frequency)	Up to 6 (depending on the supply voltage and frequency)
One time programmable (OTP) memory	512 bytes (OTP) for user data	2 Kbytes (OTP) area
FLASH security and protections	• Read protection (RDP) • Write protections • Proprietary code readout protection (PCROP)	• TrustZone® backed watermark and block security protection • HDP protection providing temporal isolation • Configuration protection • Write protection • Device nonvolatile security life cycle and application boot state management
User option bytes (1)	nRST_STDBY nRST_STOP WDG_SW BOR_LEV OPTSTRT OPTLOCK nWRP RDP USER SPRMOD	NRST_STBY NRST_STOP IWDG_SW WWDG_SW IWDG_STBY, IWDG_STOP BOR_LEV BORH_EN BOOT_UBE OPTSTRT OPTLOCK WRPSG PRODUCT_STATE IO_VDDIO2_HSLV SWAP_BANK

1. *Refer to the "Option-byte organization" table in the reference manual that provides all user option bytes.*

5.2.2 SRAMs

The RAMCFG controller, a new peripheral available on STM32H523/533, is dedicated to control SRAM1, SRAM2, SRAM3, and BKPSRAM. Refer to the *RAMs configuration controller* section in the corresponding reference manual for more details.

Table 16. SRAM features

Features	STM32F446	STM32H523/533
Size	Up to 128 Kbytes: • Main internal SRAM1 (112 KB) – Auxiliary internal SRAM2 (16 KB) • 4 Kbytes of backup SRAM	Up to 274 Kbytes: • 128-Kbyte SRAM1 • 80-Kbyte SRAM2 w/ECC • 64-Kbyte SRAM3 • 2-Kbyte BKPSRAM

Features	STM32F446	STM32H523/533
Access by DMA and CPU	• Bytes, half-words (16 bits), or full words (32 bits) possible access.	• Bytes, half-words (16 bits), or full words (32 bits) possible access.
CPU access bus	• System bus or I-Code/D-Code buses.	• System bus or C-bus. • BKPSRAM (only system bus).
Retention	BKPSRAM: • Optional retention in Standby mode. • Optional retention in VBAT mode.	
Security	NA	• When the TrustZone® security is enabled, all SRAMs are secure after reset. • The SRAMs can be programmed as nonsecure, using the MPCBB with a block granularity of 512 bytes.
Hardware and software erase conditions	• The backup SRAM is not mass erased by a tamper event. • Backup SRAM is only erased when the RDP changes from level 1 to 0.	• SRAM1 and SRAM2 erase can be requested by executing a specific software sequence, detailed in section *RAMCFG* of the product reference manual. • SRAM2 and optional backup SRAM are protected by the tamper detection circuit, and erased by hardware in case of tamper detection. • SRAM2 is erased in case of regression.
System reset erase	NA	• SRAM2 can be erased with a system reset using the option bit SRAM2_RST option bit in the flash memory user option bytes. • SRAM1 and SRAM3 are erased when a system reset occurs if the SRAM13_RST option bit is selected in the flash memory user option bytes.
Error detection and correction	NA	• Single error detection and correction with interrupt generation. • Double error detection with interrupt or NMI generation. • The ECC is supported by SRAM2 and BKPSRAM when enabled with the SRAM2_ECC and BKPRAM_ECC user option bits. • ECC: 7 bits are added per 32 bits. • Interrupts are generated when single- and/or double-ECC errors are detected: – Two ECC RAMCFG interrupts. – One ECC NMI interrupt.
Write protection	NA	• SRAM2 can be write-protected with a page granularity of 1 Kbyte. • Each 1-Kbyte page can be write-protected by setting its corresponding PxWP (x = 0 to 63) bit in RAMCFG registers.

5.2.3 System configuration controller

The table below illustrates the main differences in the system configuration controller (SYSCFG) between STM32F446 and STM32H523/533 devices.

Note: For the STM32H5 series, SYSCFG is integrated in the system configuration, boot, and security (SBS).

Table 17. System configuration features

STM32F446	STM32H523/533
Managing the I/O compensation cell	
• Remap the memory accessible in the code area. • Manage the external interrupt line connection to the GPIOs.	NA
NA	• Enabling/disabling the FMP high-drive mode of some I/Os and voltage booster for the I/O analog switches. • Configuring TrustZone® security register access. • Tracking the PVT conditions to control the current slew-rate and output impedance in the I/O buffer through compensations cells.

STM32F446	STM32H523/533
	• Two compensation cells are embedded, one for the I/Os supplied by the VDDIO power rail, and one for the I/Os supplied by the VDDIO2 power rail.

5.2.4 Instruction and data caches (ICACHE/DCACHE)

STM32H523/533 devices embed an ICACHE (8 Kbytes) and a DCACHE (4 Kbytes), which allow a more efficient use of the external memory through Octo-SPI and FMC ports.

STM32F446 devices embed an ART Accelerator with cache.

5.2.5 Direct memory access controller (DMA)

STM32F446 and STM32H523/533 have different DMA architectures and features.

All devices embed two DMA controllers:

- DMA1 (eight channels) and DMA2 (eight channels) for STM32F446.
  Each channel has dedicated management of the memory access requests from one or more peripherals. The devices also embed an arbiter for handling the priorities among the DMA requests.
- GPDMA1 (eight channels) and GPDMA2 (eight channels) for STM32H523/533. Each GPDMA instance has the same channel-based implementation and is connected to the same requests and triggers.

The following table illustrates the main differences between DMA requests in STM32F446 and STM32H523/533.

Table 18. DMA features

Peripherals	STM32F446		STM32H523/533	
	DMA1	DMA2	GDMA1	GDMA2
Architecture	Each instance of DMA controllers can access memory and peripherals			
Number of instances	1	1	1	1
Number of controllers	Dual AHB controller bus	Dual AHB controller bus	Dual bidirectional AHB controller	
Number of channels	8	8	8	8
TrustZone® security	NA		Yes	
Privileged/unprivileged DMA				
Linked-List				

5.2.6 Reset and clock control (RCC)

The table below presents the main differences related to the RCC (reset and clock controller) between STM32F446 and STM32H523/533 devices.

Table 19. RCC features

RCC	STM32F446	STM32H523/533
HSI	16 MHz RC oscillator	64 MHz RC oscillator
CSI	NA	CSI: low-power RC oscillator that can be used directly as a system clock, peripheral clock, or PLL input: low-cost clock source since no external crystal is required faster startup time than HSI (a few microseconds) very low-power consumption. The CSI provides a clock frequency of about 4 MHz.
HSI48	NA	48 MHz RC oscillator HSI48 can drive USB and RNG.
LSI	32 kHz RC Lower consumption, higher accuracy	

RCC	STM32F446	STM32H523/533
HSE	From 4 to 26 MHz	From 4 to 50 MHz
LSE	32.768 kHz Configurable drive/consumption	32.768 kHz Configurable drive/consumption
PLL	Three PLLs: • PLLI2S and PLLSAI generate an accurate clock • A main PLL clocked by the HSE or HSI oscillator and featuring three different output clocks: – One output generates the high-speed system clock (up to 180 MHz) – One output for USB OTG_FS, or SDIO – One output for the I2S1 and I2S2 clocks, the SPDIFRX clock, or the high speed system clock	Three PLLs: • Main PLL (PLL1) provides clocks for CPU and some peripherals • PLL2 and PLL3 generate the kernel clock for peripherals Each PLL offers three outputs with postdividers. Input frequency range: • 2 to 16 MHz for the VCO in wide-range mode • 1 to 2 MHz for the VCO in low-range mode
AHB frequency	Up to 180 MHz	Up to 250 MHz
APB1 frequency	42 MHz	Up to 250 MHz
APB2 frequency	84 MHz	Up to 250 MHz
RTC clock source	LSE, LSI, or HSE/ 32	
Kernel clock	Yes	Independent kernel clock for each peripheral, allowing frequency scaling without impact on communication interfaces
System clock source	HSI, HSE, two main PLL	HSI, CSI, HSE, or PLL1
Clock security system	CSS on HSE	CSS on HSE CSS on LSE
MCO clock source	• MCO1 pin (PA8): HSI, LSE, HSE, or PLL • MCO2 pin (PC9): HSE, PLL, SYSCLK, or PLLI2S	• MCO1 pin (PA8): HSI, LSE, HSE, PLL1, or HSI48 • MCO2 pin (PC9): SYSCLK, PLL2, HSE, PLL1, CSI, or LSI

Peripheral clock configuration

The peripherals presented below have a dedicated clock source that is used to generate the clock required for their operations. This section presents the differences between STM32F446 and STM32H523/533 devices, for peripherals with different clock sources.

Table 20. Peripherals with different clock sources

Peripherals	STM32F446	STM32H523/533
SAI	PLLI2S_Q PLLSAI_Q PLL_R HSI/HSE depends on PLLSRC (only for SAI2) External clock mapped on I2S_CKIN pin (only for SAI1)	pll1_q_ck pll2_p_ck pll3_p_ck AUDIOCLK per_ck
U(S)ART	APB1 or APB2 clock: PCLK2 (only for USART1 and USART6) PCLK1 (for other USARTs)	rcc_pclk1(1) rcc_pclk2(2) pll2_q_ck

Peripherals	STM32F446	STM32H523/533
		pll3_q_ck hsi_ker_ck csi_ker_ck lse_ck
I2Cs	APB1 clock (PCLK1)	rcc_pclk1(3) rcc_pclk3(4) pll3_r_ck hsi_ker_ck
SPI	APB clock (PCLK)	rcc_pclk2(5) rcc_pclk3 pll2_q_ck(5) pll3_q_ck(5) hsi_ker_ck(5) hse_ck(5) csi_ker_ck(5) pll1_q_ck(6) pll2_p_ck(6) pll3_p_ck(6) AUDIOCLK(6) per_ck(6)
I2S	PLLI2S_R External clock mapped on I2S_CKIN pin PLL_R HSI/HSE depends on PLLSRC bit	pll1_q_ck pll2_p_ck pll3_p_ck AUDIOCLK per_ck
CAN	APB clock (PCLK)	hse_ck pll1_q_ck pll2_q_ck
ADC	APB2 clock (PCLK2)	rcc_hclk sys_ck pll2_r_ck hse_ck hsi_ker_ck csi_ker_ck
USB FS	PLL 48 MHz derived from main PLL VCO (PLLQ clock)	hsi48_ker_ck pll1_q_ck pll3_q_ck
SDIO/SDMMC	SDIO: PLL48CLK or system clock	SDMMC1: pll1_q_ck pll2_r_ck
IWDG	LSI	

1. *Only for UARTx (x=4,5,7,8,9,12) and USARTx (x=2,3,6,10,11).*
2. *Only for USART1.*

3. *Only for I2Cx (x=1,2).*
4. *Only for I2C3.*
5. *Only for SPI4.*
6. *Only for SPIx (x=1,2,3).*

5.2.7 Power (PWR)

The table below presents the PWR controller differences between STM32F446 and STM32H523/533 devices. Both dynamic and static power consumption were optimized for STM32H523/533 devices.

Table 21. PWR features

PWR	STM32F446	STM32H523/533
Power supplies	**VDD = 1.7 to 3.6 V**: external power supply for I/Os and the internal regulator (when enabled), provided externally through VDD pins.	**VDD = 1.71 V to 3.6 V**: external power supply for the I/Os, the internal regulator, and the system analogs such as reset, power management, and internal clocks. It is provided externally through the VDD pins.
	VDDA = 1.7 to 3.6 V: external analog power supplies for ADC, DAC, reset blocks, RCs, and PLL. VDDA must be connected to VDD.	**VDDA = 1.62 V ADCs/1.8 V (DAC), 2.1 V (VREFBUF) to 3.6 V**: external analog power supply for ADC, DAC, and voltage reference buffer. The VDDA voltage level is independent from the VDD voltage.
	V12: voltage source through VCAP_1 and VCAP_2 pins/ around **1.2 V**	**VCAP = 1.0 V to 1.35 V**: power supply for digital peripherals, SRAMs (except BKPSRAM), and embedded flash memory
	VBAT = 1.65 to 3.6 V: when VDD is not present, VBAT is the power supply for RTC, external clock 32 kHz oscillator, and backup registers	**VBAT = 1.2 V to 3.6 V**: when VDD is not present, VBAT is the power supply for RTC, the external clock 32 kHz oscillator, backup registers, and optional backup SRAM
	VDDUSB = 3.0 V to 3.6 V: can be connected either to VDD or an external independent power supply for USB transceivers	**VDDUSB = 3.0 V to 3.6 V**: external independent power supply for USB transceivers. The VDDUSB voltage level is independent from the VDD voltage.
	NA	**VDDIO2 = 1.08 V to 3.6 V**: external power supply for 10 I/Os (PD6, PD7, PG9:14, PB8, PB9). This voltage is independent from the VDD voltage.
Battery backup domain	RTC with backup registers LSE Backup SRAM when the low-power backup regulator is enabled. PC13 to PC15 I/Os	RTC with backup registers (128 bytes) LSE LSE, backup SRAM when the low-power backup regulator is enabled PC13 to PC15 I/Os
Power supply supervisor	POR, PDR, BOR, PVD	
	NA	AVD Backup domain voltage and temperature monitoring
Sleep mode wake-up sources	Any peripheral interrupt/wakeup event	
Standby mode, wake-up sources	WKUP pin rising edge RTC alarm (alarm A and alarm B), RTC wake-up, tamper event, time stamp event, external reset in NRST pin IWDG reset External reset in NRST pin	WKUPx pin edge, RTC event, external reset in NRST pin, IWDG reset, BOR reset

PWR	STM32F446	STM32H523/533
Stop mode, wake-up sources	Any EXTI line (configured in the EXTI registers, internal and external lines)	Any EXTI line (configured in the EXTI registers) Specific peripheral events
Wake-up system clock	Stop: HSI RC oscillator	Stop: CSI when STOPWUCK = 1 in RCC_CFGR HSI with the frequency before entering the Stop mode, up to 64 MHz, when STOPWUCK Standby: HSI clock at 64 MHz
Low-power modes	Sleep mode	Sleep mode
	Stop mode	Stop mode: To further optimize the power consumption, the unused RAMs can be totally or partially shut off.
	Standby mode	Standby mode

STM32H523/533 devices embed an LDO regulator to provide the VCORE supply for digital peripherals, SRAM1, SRAM2, SRAM3, and the embedded flash memory. This regulator can provide four different voltages (voltage scaling) and can operate in Stop modes.

The following figures present the power supply for STM32F446 and STM32H523/533 devices. The differences are summarized in the previous table.

Figure 6. STM32H523/533 power supply overview

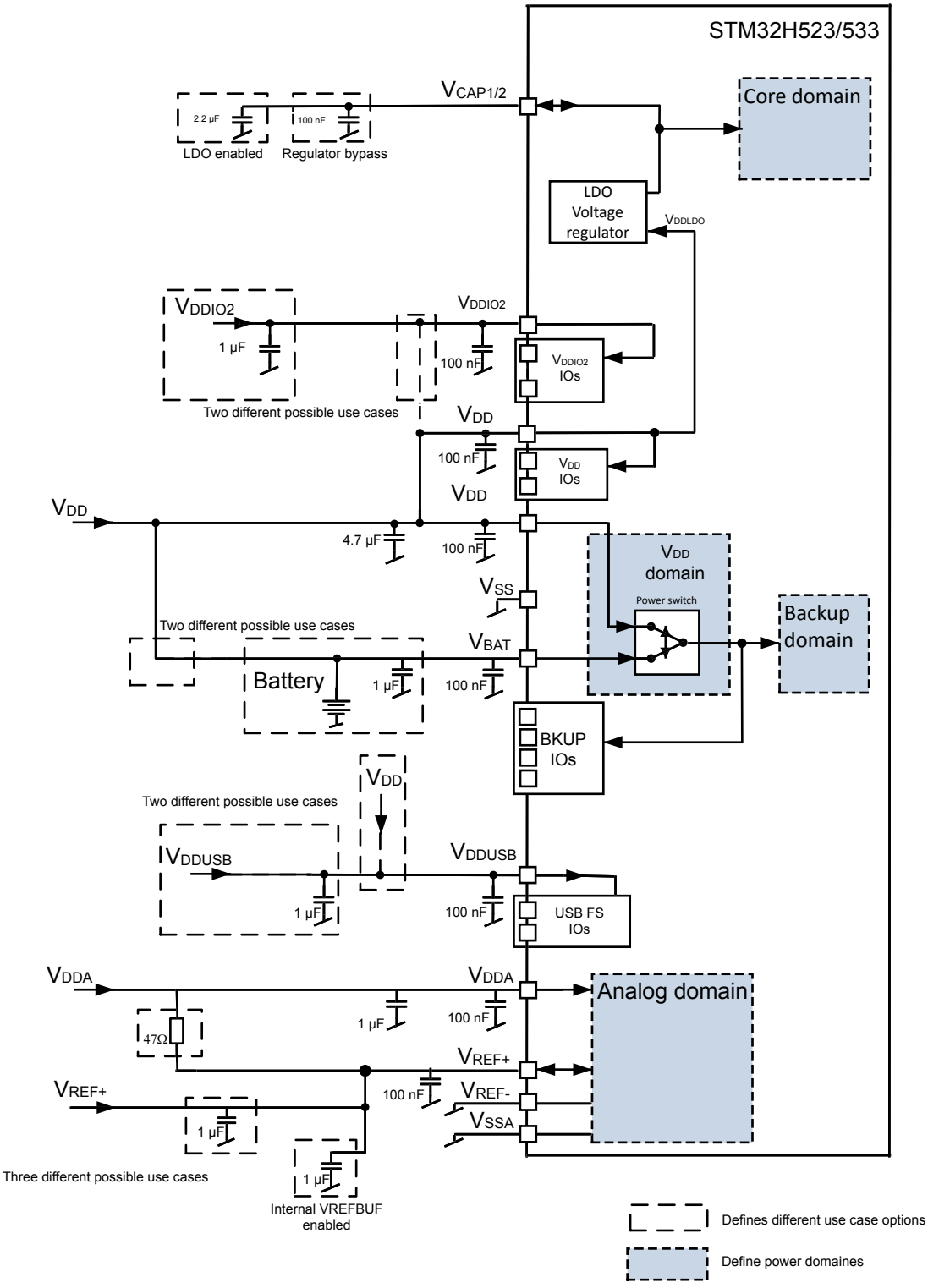
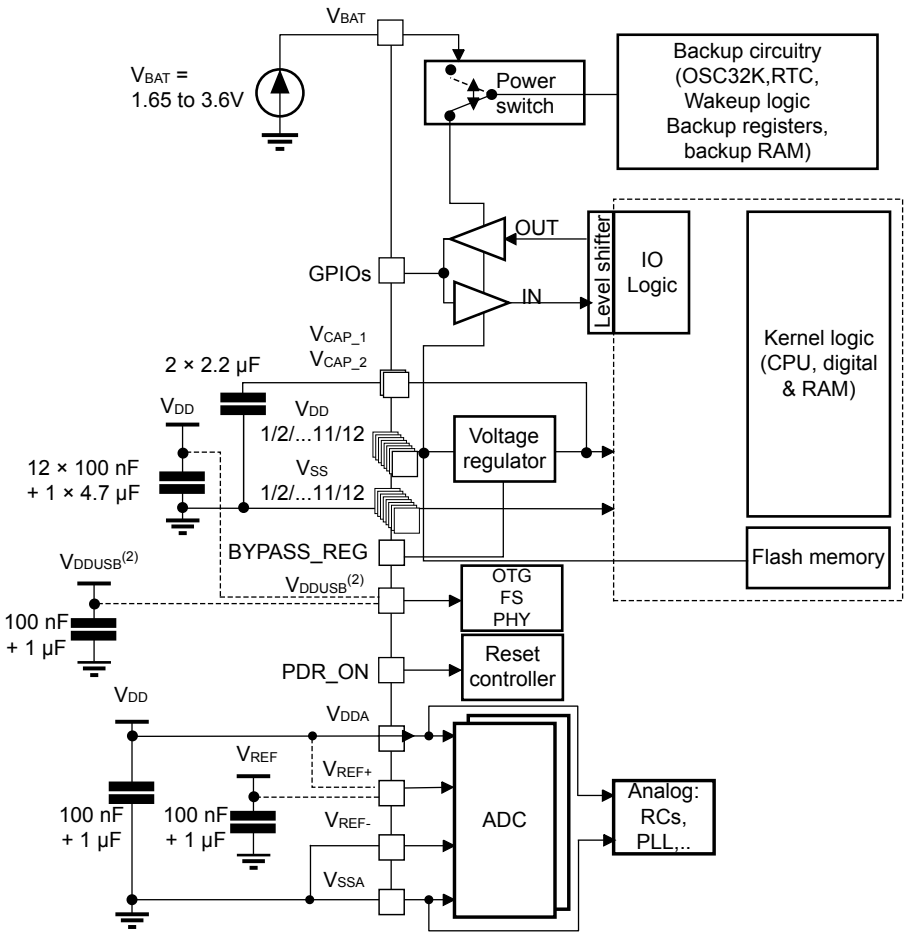


Figure 7. Power supply overview for STM32F446xx



5.2.8 General-purpose I/Os (GPIO)

STM32H523/533 implement the same GPIO features as STM32F446, but with a few differences.

For STM32H523/533, each GPIO port has four 32-bit configuration registers (GPIOx_MODER, GPIOx_OTYPER, GPIOx_OSPEEDR, and GPIOx_PUPDR), two 32-bit data registers (GPIOx_IDR and GPIOx_ODR), a 16-bit reset register (GPIOx_BRR) and a 32-bit set/reset register (GPIOx_BSRR).

In addition, all GPIOs have a 32-bit locking register (GPIOx_LCKR), two 32-bit alternate function selection registers (GPIOx_AFRH and GPIOx_AFRL), a secure configuration register (GPIOx_SECCFGR) and a high-speed low-voltage register (GPIOx_HSLVR).

Each general-purpose I/O pin of the GPIO port in STM32H523/533 can be configured individually as secure through the GPIOx_SECCFGR register. After a reset, all GPIO ports are secure.

All GPIO registers can be read and written by privileged and unprivileged access, whatever the security state (secure or nonsecure).

- Additional TrustZone® security support. The TrustZone® security is activated by the TZEN option byte in the FLASH option byte register. When TrustZone® is active (TZEN = 0xB4), each I/O pin of the GPIO port can be individually configured as secure through the GPIOx_SECCFGR register.
- I/Os state retention during Standby mode. In Standby mode, the I/Os in STM32H523/533 are in floating state by default. If the IORETEN bit in the PWR_IORETR register is set, the I/Os state is sampled during standby entry. The state of the I/Os is applied to the pin via pull-up and pull-down resistors. The pull-up and pull-down resistors remain applied after Standby wake-up until the software clears the IORETEN bit in the PWR_IORETR register.
- High-speed low-voltage mode (HSLV). Some I/Os are able to increase their maximum speed at low voltage by configuring them in HSLV mode. The I/O HSLV bit controls whether the I/O output speed is optimized to operate at 3.3 V (default setting) or at 1.8 V (HSLV = 1).

For more information about the STM32H523/533 GPIO and TrustZone® security, refer to the *General-purpose I/Os (GPIO)* section of the reference manual and to the product datasheet, which both contain a detailed description of the pinout and alternate function mapping.

5.2.9 Extended interrupt and event controller (EXTI)

5.2.9.1 EXTI main features in STM32H523/533

The extended interrupts and event controller (EXTI) manages the individual CPU and system wake-up through configurable event inputs. It provides wake-up requests to the power control and generates an interrupt request to the CPU NVIC and events to the CPU event input. For the CPU, an additional event generation block (EVG) is needed to generate the CPU event signal.

STM32H523/533 devices feature TrustZone® security support and privileged/unprivileged mode selection, and do not feature direct event inputs.

EXTI security protection

When security is enabled for an input event, the associated input event configuration and control bits can only be modified and read by a secure access. A nonsecure write access is discarded and a read returns 0.

EXTI privilege protection

When privilege is enabled for an input event, the associated input event configuration and control bits can only be modified and read by a privileged access. An unprivileged write access is discarded and a read returns 0.

The table below describes the difference of EXTI features between STM32F446 and STM32H523/533 devices.

Table 22. EXTI features

EXTI	STM32F446	STM32H523/533
Features	Generation of up to 23 software event/interrupt requests	• 58 input events supported • TrustZone® support • Privileged/unprivileged mode

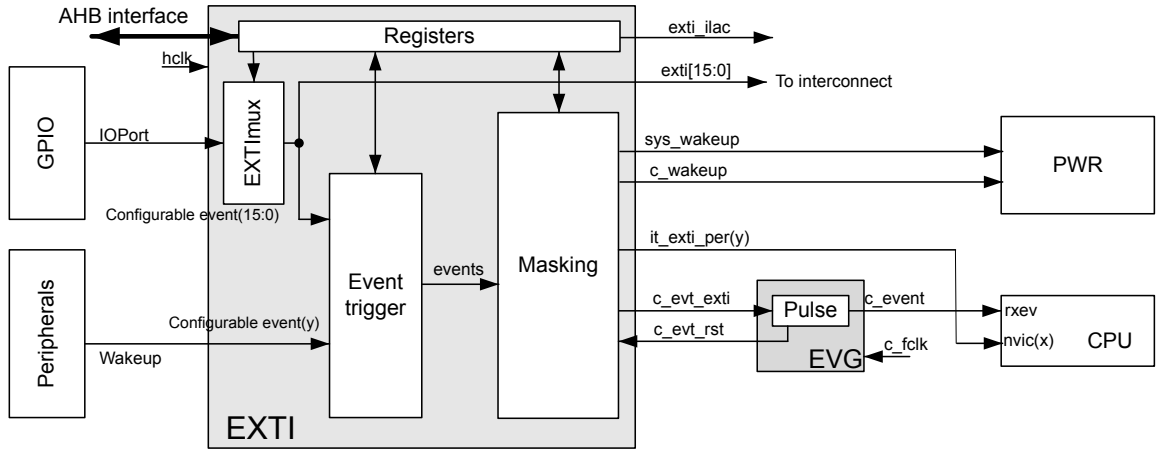
5.2.9.2 EXTI block diagram in STM32H523/533

As shown in the figure below, EXTI consists of:

- A register block, accessed via an AHB interface
- An event input trigger block
- A masking block, and EXTI mux as shown in the figure below

The register block contains all the EXTI registers. The event input trigger block provides event input edge trigger logic.

Figure 8. **EXTI block diagram on STM32H523/533**



The table below presents the EXTI line differences between STM32F446 and STM32H523/533 devices.

Table 23. **EXTI line differences**

EXTI line	STM32F446	STM32H523/533
0-15	16 external interrupt lines	GPIO
16	PVD output	PVD/AVD output
17	RTC alarm event	RTC nonsecure
18	USB OTG_FS wake-up event	RTC secure
19	NA	TAMP nonsecure
20	USB OTG_HS (configured in FS) wake-up event	TAMP secure
21	RTC tamper and time stamp events.	I2C1 wake-up
22	RTC wake-up event	I2C2 wake-up
23	NA	I2C3 wake-up
24		I3C wake-up
25		USART1 wake-up
26		USART2 wake-up
27		USART3 wake-up
28		UART4 wake-up
29		UART5 wake-up
30		USART6 wake-up
31		Reserved
32		Reserved
33		Reserved
34		Reserved
35		Reserved
36		Reserved
37		LPUART1 wake-up
38		LPTIM1
39		LPTIM2

EXTI line	STM32F446	STM32H523/533
40	NA	SPI1 wake-up
41		SPI2 wake-up
42		SPI3 wake-up
43		SPI4 wake-up
44		Reserved
45		Reserved
46	NA	Reserved
47		USB FS wake-up
48		USBPD1 wake-up
49		LPTIM2 CH1
50		DTS wake-up
51		HDMI-CEC wake-up
52		Reserved
53		UVM output
54		Reserved
55		Reserved
56		Reserved
57		Reserved

5.2.10 CRC calculation unit

The table below presents the CRC differences between STM32F446 and STM32H523/533 devices.

Table 24. CRC features

CRC	STM32F446	STM32H523/533
Features	• Uses CRC-32 (Ethernet) polynomial • Single input/output 32-bit data register • CRC computation is done in 4 AHB clock cycles (HCLK) for the 32-bit data size • General-purpose 8-bit register (can be used for temporary storage)	
	Handles 32-bit data size	• Handles 8-,16-, 32-bit data size fully programmable polynomial with programmable size (7, 8, 16, 32 bits) • Programmable CRC initial value • Input buffer to avoid bus stall during calculation • Reversibility option on I/O data • Accessed through an AHB target peripheral by 32-bit words only, except for the CRC_DR register, which can be accessed by words, right-aligned half words, and right-aligned bytes
CRC registers	CRC data register (CRC_DR) CRC independent data register (CRC_IDR) CRC control register (CRC_CR)	
	-	CRC initial value (CRC_INIT) CRC polynomial (CRC_POL)

5.3 Migration of security peripherals

5.3.1 Random number generator (RNG)

STM32H523/533 devices embed an RNG that delivers 32-bit random numbers generated by an integrated analog circuit.

In STM32H523/533, the RNG is transparently used by SAES and PKA.

When the RNG finds an unexpected error, an internal tamper event is triggered in the TAMP peripheral, and the RNG stops delivering random data. When this event occurs, the secure application needs to reset the RNG peripheral, using either central reset management or the global SoC reset. After this, another proper initialization of the RNG is required.

Note: RNG is not supported by STM32F446.

5.3.2 Hash processor (HASH)

STM32H523/533 devices embed a hash processor (HASH).

HASH is a fully compliant implementation of the secure hash algorithm (SHA-1/SHA-2 family) and the HMAC (keyed-hash message authentication code) algorithm. HMAC is suitable for applications requiring message authentication.

Note: HASH is not supported by STM32F446.

5.3.3 On-the-fly decryption engine (OTFDEC)

The OTFDEC decrypts in real-time the encrypted content stored in the external OCTOSPI memories used in Memory-mapped mode. The OTFDEC uses the AES-128 algorithm in counter mode (CTR).

STM32H533 devices embed one OTFDEC peripheral.

Note: This peripheral is not supported by STM32F446.

5.3.4 Public key accelerator (PKA)

STM32H523/533 devices embed one PKA peripheral, intended for the computation of cryptographic public key primitives within the Montgomery domain.

All needed computations are performed within the accelerator, so no further hardware/software elaboration is needed to process the inputs or the outputs.

Note: The PKA peripheral is not supported by STM32F446.

5.3.5 AES and SAES hardware accelerators

STM32H523/533 devices embed two AES accelerators: one secure AES (SAES) and a faster AES. SAES is a new feature in STM32H523/533.

In STM32H523/533, SAES with a hardware-unique key embeds a protection against differential power analysis (DPA) and related side channel attacks.

When an unexpected hardware fault occurs, an output tamper event is triggered, and AES automatically clears the key registers. A reset is required for AES to function again.

The AES peripheral can use the SAES peripheral as a security coprocessor. In this case, the secure application performs two actions:

- It prepares the key in the robust SAES peripheral.
- When the key is ready, AES can load it through a dedicated hardware key bus.

5.3.6 Global TrustZone® controller (GTZC)

The security architecture of STM32H523/533 is based on Arm® TrustZone® with the Armv8-M mainline extension.

Each GPIO, peripheral, DMA channel, clock configuration register, DCACHE/ICACHE, or small part of the flash memory or SRAM can be configured as trusted or untrusted.

The GTZC embedded in STM32H523/533 is used to configure secure TrustZone® and privileged attributes within the full system. A detailed description of GTZC is available in the product reference manual.

This controller is a new feature in STM32H523/533 devices.

Note: GTZC is not supported by STM32F446.

5.4 Migration of communication peripherals

5.4.1 Serial peripheral interface (SPI)

This section highlights the SPI features(1) implemented in STM32F446 and STM32H523/533 devices.

Table 25. SPI features

SPI	STM32F446	STM32H523/533
Instances	4x SPIs	Up to 4x SPIs
Speed	Up to 45 Mbit/s	Max 50 Mbps
Features	SPI + I2S	
	3 with muxed I2S	Including 3 muxed with full-duplex I2S
Full-duplex synchronous transfer on three lines	X	X
Half-duplex	X	X
Simplex synchronous transfer on two lines	With a unidirectional data line	With a unidirectional data line
Data size	8- or 16-bit transfer frame format selection	From 4-bit up to 32-bit data size selection or fixed to multiply of 8-bit
Multimaster mode capability	X	X
Baud rate prescalers	8 controller mode baud rate prescalers (fPCLK/2 max.)	Baud rate prescaler up to kernel frequency/2 or bypass from RCC in controller mode
Protection of configuration and settings	NA	X
Target Select (SS) management	NSS management by hardware or software for both controller and target: dynamic change of controller/target operations	Hardware or software management of SS for both controller and target
Configurable SS signal polarity and timing	NA	Configurable SS signal polarity and timing, MISO x MOSI swap capability
Programmable transaction data	NA	Programmable number of data within a transaction to control SS and CRC
Programmable data order with MSB-first or LSB-first shifting	X	X
Programmable clock polarity and phase	X	X
Dedicated transmission and reception flags with interrupt capability	X	X
SPI Motorola and TI format support	X	X
Hardware CRC features for reliable communication: • **CRC value can be transmitted as the last byte in Tx mode** • **Automatic CRC error checking for last-received byte**	X	X

SPI	STM32F446	STM32H523/533
Interrupt events and error detection with interrupt capability	Interrupts: • Transmit Tx buffer ready to be loaded • Data received in Rx buffer • Controller mode fault event • Overrun error • CRC error flag • TI frame format error	Interrupts: • TxFIFO ready to be loaded • Data received in RxFIFO • Both TXP and RXP are active • Transmission transfer filled • Overrun error • Underrun error • TI frame format error • CRC error • Mode fault • End of transfer • Controller mode suspended • TxFIFO transmission complete All the interrupt events are capable of waking up the system from Sleep mode at each instance
Configurable behavior at slave-underrun condition	NA	X (support of cascaded circular buffers)
FIFOs	NA	• Two multiples of 8-bit embedded Rx and Tx FIFOs (FIFO size depends on instance) • Configurable FIFO thresholds (data packing)
RDY status pin	NA	Optional status pin RDY signalizes that the target device is ready to handle the data flow

1. *X = available, NA = not available.*

5.4.2 Inter-integrated circuit (I2C)

STM32H523/533 devices implement the same I2C features as STM32F446 devices, but with some enhancements. The main differences are stated in the table below.

Table 26. I2C differences

I2C	STM32F446	STM32H523/533
Instances	x4 (I2C1, I2C2, I2C3, I2C4)	x3(I2C1, I2C2, and I2C3)
Features	• 7-bit and 10-bit addressing mode • SMBus/PMBus • Standard mode (up to 100 Kbit/s) • Fast mode (up to 400 Kbit/s)	
	Single clock source	• Fm+ (up to 1 MHz) I2C bus • Wake-up from Stop mode only (no autonomous mode) • Independent clock

5.4.3 Improved inter-integrated circuit (I3C)

STM32H523/533 devices implement a new feature compared to STM32F446 devices: I3C peripherals.

5.4.4 Universal synchronous/asynchronous receiver transmitter (USART)

STM32H523/533 devices implement several new features of U(S)ART compared to STM32F446 devices. The following table shows the U(S)ART differences.

Table 27. U(S)ART features

USART	STM32F446	STM32H523/533
Instances	• 4 USARTs • 2 UARTs	• 4 USARTs • 2 UARTs • 1 LPUART
Baud rate	Up to 4x 11.25 Mbit/s	Depends on the frequency (oversampling by 16 or by 8)(1)
Clock	Single clock domain	Dual clock domain and wake-up from low-power mode
Data	Word length: programmable (8 or 9 bits)	• Word length: programmable (7, 8 or 9 bits) • Programmable data order with MSB-first or LSB-first shifting
Interrupt	10 interrupt sources with flags	23 interrupt sources with flags
Others features	Hardware flow control (CTS/RTS)	• RS232 hardware flow control • RS485 hardware control mode
	• LIN mode • IrDA SIR encoder block • Continuous communication using DMA • Multiprocessor communications • Single-wire half-duplex communication	
	NA	• Modbus communication: Timeout feature, CR/LF character recognition • Two internal FIFOs for transmit and receive data • Receiver timeout interrupt (except LPUART) • Auto baud rate detection (except LPUART) • Driver enable • Swappable Tx/Rx pin configuration • Wake-up from Stop mode
	• Smartcard mode: has to be implemented by software • Number of stop bits: 0.5, 1, 1.5, 2	• Smartcard mode: Support the T=0 and T=1 asynchronous protocols • Number of stop bits: 0.5, 1, 1.5, 2

1. *Refer to the USART section in the reference manual.*

5.4.5 Serial audio interface (SAI)

The serial audio interface offers a wide set of audio protocols due to its flexibility and wide range of configurations. Many stereo or mono audio applications may be targeted (such as I2S standards, LSB- or MSB-justified, PCM/DSP, TDM, and AC'97 protocols).

Note: SAI is only available on STM32F446 devices.

5.4.6 Digital camera interface (DCMI)

The DCMI is available on STM32F446 and STM32H523/533 devices.

The main features of DCMI are:

- 8-, 10-, 12-, or 14-bit parallel interface
- Embedded/external line and frame synchronization
- Continuous or snapshot mode
- Crop feature

Supported data formats:

- 8-, 10-, 12-, and 14-bit progressive video (either monochrome or raw Bayer)
- YCbCr 4:2:2 progressive video
- RGB 565 progressive video
- Compressed data JPEG

5.4.7 Parallel synchronous slave interface (PSSI)

PSSI is only available on STM32H523/533 devices.

DCMI and PSSI use the same circuitry, and when they are both implemented on a device, they cannot be used at the same time. When using PSSI, the DCMI registers cannot be accessed, and vice versa. In addition, PSSI and DCMI share the same alternate functions and interrupt vector.

The main features of the PSSI peripheral are:

- Target mode operation
- 8- or 16-bit parallel data input or output
- 8-word (32 byte)
- Data enable (PSSI_DE) alternate function input and ready (PSSI_RDY) alternate function output.

5.4.8 Controller area network (CAN)

The main differences related to CAN between STM32F446 and STM32H523/533 are presented in the table below.

Table 28. CAN features

CAN	STM32F446	STM32H523/533
Instances	x2	x2 FDCAN
Features	• Supports CAN protocol version 2.0 A, B active • Bit rates up to 1 Mbit/s • Supports the time triggered communication option • Tx: 3 transmit mailboxes, configurable transmit priority, time stamp on SOF transmission • Rx: 2 receive FIFOs with three stages, scalable filter banks, identifier list feature, configurable FIFO overrun, and time stamp on SOF reception • Time-triggered communication option: disable automatic retransmission mode, 16-bit free running timer, and time stamp sent in the last two data bytes • Management: – Maskable interrupts – Software-efficient mailbox mapping at a unique address space • Dual CAN: • – CAN1: controller bxCAN for managing the communication between a target bxCAN and the 512-byte SRAM memory – CAN2: target bxCAN, with no direct access to the SRAM memory	• Conform with CAN protocol version 2.0-part A, B, and ISO 11898-1: 2015, -4 • CAN FD with maximum 64 data bytes supported • CAN error logging • AUTOSAR and J1939 support • Improved acceptance filtering • Two receive FIFOs of three payloads each (up to 64 bytes per payload) • Separate signaling on reception of high priority messages • Configurable transmit FIFO/queue of three payloads (up to 64 bytes per payload) • Transmit event FIFO • Programmable loop-back test mode • Maskable module interrupts • Two clock domains: APB bus interface and CAN core kernel clock • Power down support

5.4.9 Universal serial bus interface (USB)

The STM32F446 and STM32H523/533 devices have different USB peripherals:

- STM32F446 devices implement USB OTG_HS and USB OTG_FS.
- STM32H523/533 devices implement a USB FS and USB Type-C® connector/USB power delivery interface (UCPD)

Most features supported by STM32F446 devices are also supported by the STM32H5 series. The main differences in the USB peripheral between STM32F446 and STM32H523/533 are listed in the table below.

Table 29. USB differences

USB	STM32F446	STM32H523/533
General	Full support for the USB on-the-go (USB OTG)	USB FS with clock recovery
	• One bidirectional control endpoint • 5[FS]/8[HS] IN endpoints (bulk, interrupt, isochronous) • 5[FS]/8[HS] OUT endpoints (bulk, interrupt, isochronous) • 6[FS]/9[HS] bidirectional endpoints (including EP0) • 12[FS]/16[HS] host mode channels	Up to 8 bidirectional endpoints
	USB internal connect/disconnect feature with an internal pull-up resistor on the USB D + (USB_DP) line	USB connect/disconnect capability (controllable, embedded pull-up resistor on USB_DP line)
	Independent VDDUSB power supply	Battery charging detection (BCD) support for device
		Independent VDDUSB power supply
Buffer memory	• 1.25-Kbyte [FS]/4-Kbyte [HS] data FIFOs • Management of up to 6[FS]/9[HS] dedicated Tx-IN FIFOs (one for each active IN EP), to put less load on the application	2048 bytes of dedicated packet buffer memory SRAM
Low-power modes	**FS mode:** • USB suspend and resume • Link power management (LPM) support **HS mode:** • LPM supported	USB revision 2.0 including link power management (LPM) support

5.5 Migration of analog peripherals

5.5.1 Analog-to-digital converter (ADC)

STM32H523/533 devices embed two ADCs: ADC1 and ADC2. These both consist of a 12-bit successive approximation ADC, are tightly coupled, and can operate in dual mode (ADC1 is the controller).

STM32F446 devices embed three ADCs: ADC1, ADC2, and ADC3 (12-bit resolution).

The table below presents the ADC differences between STM32F446 and STM32H523/533 devices.

Table 30. **ADC differences between devices**

ADC	STM32F446	STM32H523/533
Instances	x3	x2
Resolution	12-bit	
Number of channels	Up to 24	Up to 20
Configurable resolution	12-bit, 10-bit, 8-bit, or, 6-bit	
Maximum sampling speed	2.4 MSPS 7.2 MSPS in triple interleaved mode	5 MSPS
Conversion modes	• Single • Continuous • Scan • Discontinuous • Dual mode	
DMA support	Yes	
Data register	16-bit data register	
Analog watchdog feature	This feature allows the application to detect if the input voltage goes outside the user-defined high or low threshold	
ADC input range:	VREF– ≤ VIN ≤ VREF+	VSSA ≤ VIN ≤ VREF+
New features	NA	• The ADC conversion time is independent from the AHB bus clock frequency • Manage single-ended or differential inputs • Low-power features • Three analog watchdogs per ADC • Self-calibration • The oversampling ratio is adjustable from 2 to 256 • Programmable data shift up to 8 bits

5.5.2 Digital-to-analog converter (DAC)

STM32H523/533 devices implement some enhanced DAC features compared to STM32F446 devices. Refer to the table below for the main DAC differences between these devices.

Table 31. **DAC differences**

DAC	STM32F446	STM32H523/533
Instances	x1 with two output channels	x1 with maximum two output channels
Resolution	12 bits	
Output buffer	Yes	
Dual DAC channel	For independent or simultaneous conversions	
New features	NA	• Double-data DMA • Buffer offset calibration • Sample and hold mode for low-power operation in Stop mode

5.6 Migration of timer peripherals

STM32H523/533 and STM32F446 devices include two advanced-control timers, up to six general-purpose timers, two basic timers, two watchdog timers, and two SysTick timers (one for STM32F446).

Furthermore, STM32H523/533 devices include two low-power timers.

This section compares the features of the above-listed timers and RTC in STM32H523/533 and STM32F446 devices.

5.6.1 Advanced-control timers (TIM1/TIM8)

STM32H523/533 and STM32F446 devices include two advanced-control timers, TIM1 and TIM8, with almost identical features, detailed in the table below.

Table 32. Advanced-control timer (TIM1/8) features

Feature	STM32F446	STM32H523/533
Counter resolution and type	16-bit up, down, up/down autoreload counter	
Prescaler factor	16-bit programmable prescaler, allowing the division (also "on the fly") of the counter clock frequency, by any factor between 1 and 65536	
Channels	Up to four independent channels for: • Input capture • Output compare • PWM generation (edge- and center-aligned modes) • One-pulse mode output	Up to six independent channels for: • Input capture (channels 5 and 6) • Output compare • PWM generation (edge- and center-aligned modes) • One-pulse mode output
Complementary outputs	Complementary outputs with programmable dead-time	
Synchronization with external signals and general-purpose timers	• Synchronization circuit to control the timer with external signals and to interconnect several timers together • The advanced-control (TIM1/TIM8) and general-purpose (TIMy) timers are completely independent, and do not share any resources	
Repetition counter	Repetition counter to update the timer registers only after a given number of cycles of the counter	
Break inputs	One break input to put the timer's output signals in reset state or in a known state	Two break inputs to put the timer's output signals in reset state or in a known state
Interrupt/DMA generation	Interrupt/DMA generation on the following events:	
	• Update: counter overflow/underflow or counter initialization (by software or internal/external trigger) • Trigger event (counter start, stop, initialization, or count by internal/external trigger) • Input capture • Output compare • Break input	• Update: counter overflow/underflow or counter initialization (by software or internal/external trigger) • Trigger event (counter start, stop, initialization, or count by internal/external trigger) • Input capture • Output compare
Encoders and sensors	Supports incremental (quadrature) encoder and hall-sensor circuitry for positioning purposes	
Trigger input	Trigger input for external clock or cycle-by-cycle current management	
Application examples	• Measuring the pulse lengths of input signals (input capture) • Generating output waveforms (output compare, PWM, complementary PWM with dead-time insertion)	

5.6.2 GP timers with up, down, and up-down autoreload counter (TIM2/3/4/5)

The GP (general-purpose) timers consist of a 16-bit or 32-bit autoreload counter driven by a programmable prescaler.

STM32H523/533 and STM32F446 devices include GP timers with an up, down, or up/down autoreload counter (TIM2, TIM3, TIM4, and TIM5), with identical features.

Table 33. **GP timer (TIM2/3/4/5) features**

Feature	STM32H523/533 and STM32F446
32-bit resolution	TIM2 and TIM5
16-bit resolution	TIM3 and TIM4
Counter resolution and type	16-bit or 32-bit up, down, up/down autoreload counter
Prescaler factor	16-bit programmable prescaler, used to divide (also “on the fly”) the counter clock frequency by any factor between 1 and 65535
Channels	Up to four independent channels for: • Input capture • Output compare • PWM generation (edge- and center-aligned modes) • One-pulse mode output
Synchronization with external signals and other timers	Synchronization circuit to control the timer with external signals and to interconnect several timers
Interrupt/DMA generation	Interrupt/DMA generation on the following events: • Update: counter overflow/underflow or counter initialization (by software or internal/external trigger) • Trigger event (counter start, stop, initialization, or count by internal/external trigger) • Input capture • Output compare
Encoders and sensors	Supports incremental (quadrature) encoder and hall-sensor circuitry for positioning purposes
Trigger input	Trigger input for external clock or cycle-by-cycle current management
Application examples	• Measuring the pulse lengths of input signals (*input capture*) • Generating output waveforms (*output compare and PWM*)

5.6.3 GP timers with autoreload up-counter

STM32H523/533 and STM32F446 devices include 16-bit resolution GP timers with a 16-bit autoreload up-counter:

- TIM15 for STM32H523/533 devices
- TIM9 to TIM14 for STM32F446 devices

Table 34. GP timer (with autoreload up-counter) features

Feature	STM32F446		STM32H523/533	
16-bit resolution	TIM10/TIM11 and TIM13/TIM14	TIM9/TIM12	TIM15	
Counter resolution and type	16-bit autoreload up-counter			
Prescaler factor	16-bit programmable prescaler used to divide the counter clock frequency by any factor between 1 and 65535			
Channels	Independent channel for: • Input capture • Output compare • PWM generation (edge-aligned mode) • One-pulse mode output	Up to two independent channels for:		One channel for:
Complementary outputs	NA		Complementary outputs with programmable dead-time (for channel 1 only)	Complementary outputs with programmable dead-time
Break input	NA		Break input to put the timer's output signals in the reset state or a known state	
Synchronization with external circuits and other timers	NA	Synchronization circuit to control the timer with external signals and to interconnect several timers together		NA
Repetition counter	NA		Repetition counter to update the timer registers only after a given number of cycles of the counter	
Interrupt generation	Interrupt generation on the following events: • Update: counter overflow or counter initialization (by software) • Input capture • Output compare	• Update: counter overflow or counter initialization (by software or internal trigger) • Trigger event (counter start, stop, initialization, or count by internal trigger) • Input capture • Output compare	Interrupt/DMA generation on the following events: • Update: counter overflow or counter initialization (by software or internal/ external trigger) • Trigger event (counter start, stop, initialization, or count by internal/external trigger) • Input capture • Output compare • Break input (interrupt request)	• Update: counter overflow • Input capture • Output compare • Break input
Application examples	• Measuring the pulse lengths of input signals (input capture) • Generating output waveforms (output compare, PWM).			

5.6.4 Basic timers (TIM6/7)

The basic timers TIM6 and TIM7 consist of a 16-bit autoreload counter driven by a programmable prescaler. These timers are completely independent, and do not share any resources.

STM32H523/533 and STM32F446 devices have the same basic timer features.

Table 35. **Basic timers**

Feature	STM32F446 and STM32H523/533
Counter resolution and type	16-bit autoreload up-counter
Prescaler factor	16-bit programmable prescaler, used to divide (also “on the fly”) the counter clock frequency by any factor between 1 and 65535
Synchronization signals	Synchronization circuit to trigger the DAC
Interrupt/DMA generation	Interrupt/DMA generation on the update event: counter overflow

5.6.5 Low-power timers (LPTIM1/2)

The LPTIM is a 16-bit timer that benefits from the ultimate developments in power-consumption reduction. This is a new feature in STM32H523/533 that is not available on STM32F446 devices. The table below describes the LPTIM features on STM32H523/533 devices.

Table 36. **LPTIM features**

Feature	STM32H523/533
LPTIMx	LPTIM1 and LPTIM2
Counter resolution and type	16 bit up-counter
Prescaler factor	3-bit prescaler with 8 possible dividing factors (1,2,4,8,16,32,64,128)
Selectable clock	• Internal clock sources: configurable internal clock source (see RCC section) • External clock source over LPTIM input (working with no LP oscillator running, used by pulse counter application)
Autoreload	16 bit ARR auto reload register
Capture/compare	16 bit capture/compare register
Continuous mode	Continuous/one-shot mode
Trigger mode	Selectable software/hardware input trigger
Glitch filter	Programmable digital glitch filter
Configurable output	Configurable output: pulse, PWM
Polarity	Configurable I/O polarity
Encoder mode	Yes
Repetition counter	Yes
Input capture, PWM, and one-pulse channels	Up to two independent channels for: • Input capture • PWM generation (edge-aligned mode) • One-pulse mode output
DMA requests	DMA request generation on the following events: • Update event • Input capture

5.6.6 Watchdogs (WWDG/IWDG)

STM32H523/533 and STM32F446 devices embed two watchdogs:

- A system window watchdog (WWDG) with the same features
- An independent watchdog (IWDG) with differences

Table 37. IWDG features

Feature	STM32F446	STM32H523/533
Clock	Clocked from an independent RC oscillator	• Independent clock • LSI used as IWDG kernel clock (iwdg_ker_ck)
Window option(1)	-	X
Early wake-up interrupt generation (1)	-	X
Reset generation(1)	X	

1. *"X" = supported, "-" = not supported.*

5.6.7 Real-time clock (RTC)

The following table describes the different RTC features between STM32F446 and STM32H523/533 devices. For more information about RTC, refer to the RTC section of the product reference manual.

Table 38. RTC features

RTC	STM32F446	STM32H523/533
Feature	Calendar with subseconds, seconds, minutes, hours (12- or 24-hour format), weekdays, dates, months, and years	
	Two programmable alarms	
	Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision	
	Timestamp function	
	Daylight saving time	
	Automatic wake-up	
	Digital calibration circuit with 0.95 ppm resolution	
	Alarm A, alarm B, wake-up interrupt, timestamp, tamper detection	Alarm A, alarm B, wake-up timer, and timestamp individual privilege protection
	NA	• Binary mode with 32-bit free-running counter • On-the-fly correction from 1 to 32767 RTC clock pulses • RTC TrustZone® support
Tamper and backup registers	• 20x 32-bit backup registers • 2x tamper pins/2 events • Edge or level detection with configurable filtering	• 32x 32-bit backup registers • Up to 11 tamper pins for 8 external tamper detection events • 13 internal tamper events • TrustZone® support

5.6.8 SysTick timer

The SysTick timer is dedicated to real-time operating systems, but can also be used as a standard down-counter.

The Cortex®-M33 processor with TrustZone® in STM32H523/533 devices embeds two SysTick timers. When TrustZone® is activated, the two SysTick timers are available, but when TrustZone® is disabled, only one SysTick timer is available.

STM32F446 embeds a Cortex®-M4, with just one SysTick timer.

5.7 Migration of external memory interface peripherals

5.7.1 Flexible memory controller (FMC)

The following table presents the FMC interface differences between STM32F446 and STM32H523/533 devices.

Table 39. **FMC features**

FMC		STM32F446	STM32H523/533
External memory interfaces		• SRAM • NOR/NAND memories • PSRAM (four memory banks) • One bank of NAND flash memory with ECC hardware	• SRAM • NOR flash memory/one NAND flash memory • PSRAM • Ferroelectric RAM (FRAM) • NAND flash memory with ECC hardware to check up to 8 Kbytes of data
Data bus width		8 or 16 bits	8 or 16 bits
FMC Bank memory mapping	**Bank 1** **4x 64 Mbytes**	NOR/PSRAM/SRAM	NOR/PSRAM/SRAM
	Bank 2 **4x 64 Mbytes**	Reserved	Not used
	Bank 3 **4x 64 Mbytes**	NAND flash memory	NAND flash memory
	Bank 4 **4x 64 Mbytes**	Reserved	Not used
	SDRAM Bank 1 **4x 64 Mbytes**	SDRAM	NA
	SDRAM Bank 2 **4x 64 Mbytes**		

For STM32H523/533, the FMC registers can be configured as secure through the TZSC controller (refer to the reference manual for more details).

5.7.2 Octo-SPI interface (OCTOSPI)

The OCTOSPI peripheral provides a serial interface that enables communication with external serial memories such as flash memory, PSRAM, HyperRAM™, and HyperFlash™.

The Octo-SPI specialized communication interface targets single-, dual-, quad-, or octal-SPI memories, and can be configured in three modes: indirect, status-polling, and memory-mapped.

The OCTOSPI peripheral is available on STM32H523/533 devices with the following features:

- Functional modes: indirect, status-polling, and memory-mapped
- Read and write support in memory-mapped mode
- Dual-quad configuration
- SDR (single-data rate) and DTR (double-transfer rate)
- Data strobe (DS, DQS)
- GPDMA interface

Note: Octo-SPI is not supported by STM32F446.

Revision history

Table 40. **Document revision history**

Date	Version	Changes
08-Mar-2024	1	Initial release.
03-Apr-2024	2	Fixed typo.

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