50 W converter using HVLED101 quasi-resonant HPF flyback controller with primary side regulation

Introduction

The EVLHV101PSR50W is intended to provide a stable and insulated 60 V voltage, for a maximum power of 50 W, when a wide range of AC or DC input voltages is applied at its input.

It can be used as a standalone power supply or as a front-end stage in a dimmable (or non-dimmable) offline LED driver.

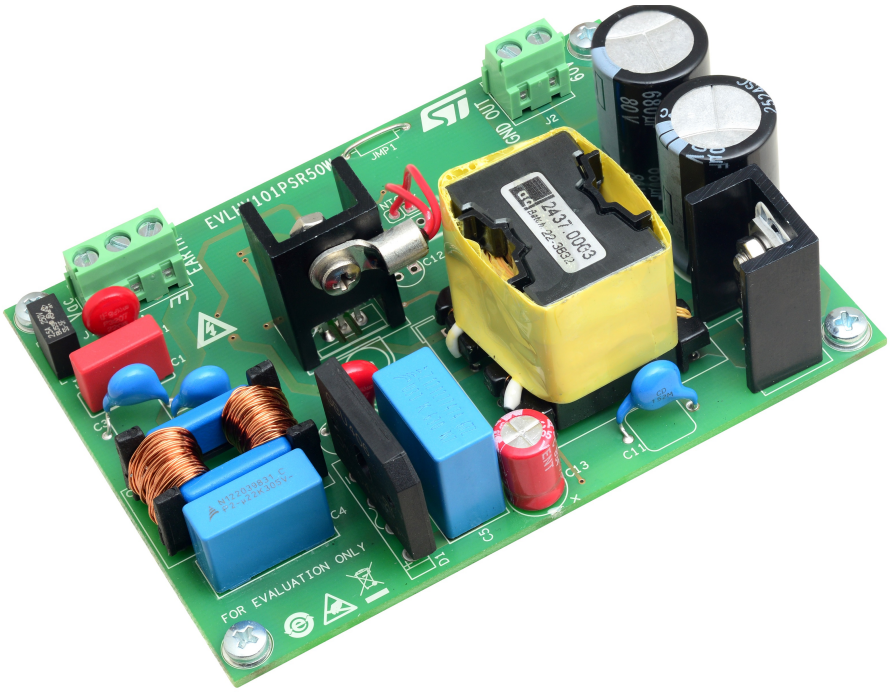
A very high power factor and low THD are obtained from this demonstration board thanks to the features of the HVLED101 which adopts a patented THD optimizer and frequency foldback with valley locking operation to reduce the switching losses and avoid acoustic noise.

Maximum input power is automatically limited by HVLED101's internal algorithm (MPC), which helps increase system safety.

Input voltage variations, excessive input voltage (overvoltage like surge or bursts), and insufficient input voltage are managed by the HVLED101 protections, which improve the reliability of the application.

Output short-circuit and overload protection with auto-restart behavior is implemented.

Figure 1. EVLHV101PSR50W evaluation kit (75 x 100 mm)



1 Main characteristics

- Input voltage: V_{IN}: 90 - 265 V_{RMS}, f: 45-66 Hz
- Output voltage: 60 V / 833 mA
- High power factor, low THD
- PF / THD:
- – >0.99 / < 5% at 115 V_{AC} and 230 V_{AC} @ full load
  – >0.99 / < 6% at 115 V_{AC}, > 0.93 / < 7% @ 230 V_{AC} @ half load
  – >0.99 / < 6% at 115 V_{AC}, > 0.99 / < 8% @ 230 V_{AC} @ 1/3 load
- 4 points (25%, 50%, 75%, 100% load) average efficiency > 91%
- Efficiency > 50% in standby (Pout = 240 mW)
- Frequency foldback with valley locking for noise-free operation
- Startup time < 200 ms.
- $T_{AMB-MAX}$ = 60 °C
- Open load voltage limiting (< 65 V)
- Short-circuit protection with auto-restart
- NTC overtemperature protection for switching MOSFET
- Safety acc. to EN60065
- EMI acc to EN55022 – conducted emission
- RoHS compliant

Table 1. Main components

Main components	
HVLED101	Quasi-resonant flyback controller
STF14N80K5	N-channel 800 V, 0.400 Ohm typ., 12 A MDmesh K5 Power MOSFET in a TO-220FP package
STTH16R04C	Ultrafast diode 400 V, 4 A in TO-220AB package
STTH108A	Ultrafast diode 800 V, 1 A in SMA package

Table 2. Description of connector signals

Con.	Pin	Signal name	Dir.	Description and use
J1	1	V_{AC}	Input	First connection to AC mains – warning high voltage
	2	V_{AC}	Input	Second connection to AC mains – warning high voltage
	3	EARTH	Earth	Earth connection
J2	1	GND_{OUT}	Output	Ground
	2	60 V	Output	60 V output (isolated)

Figure 2. **Board connections**

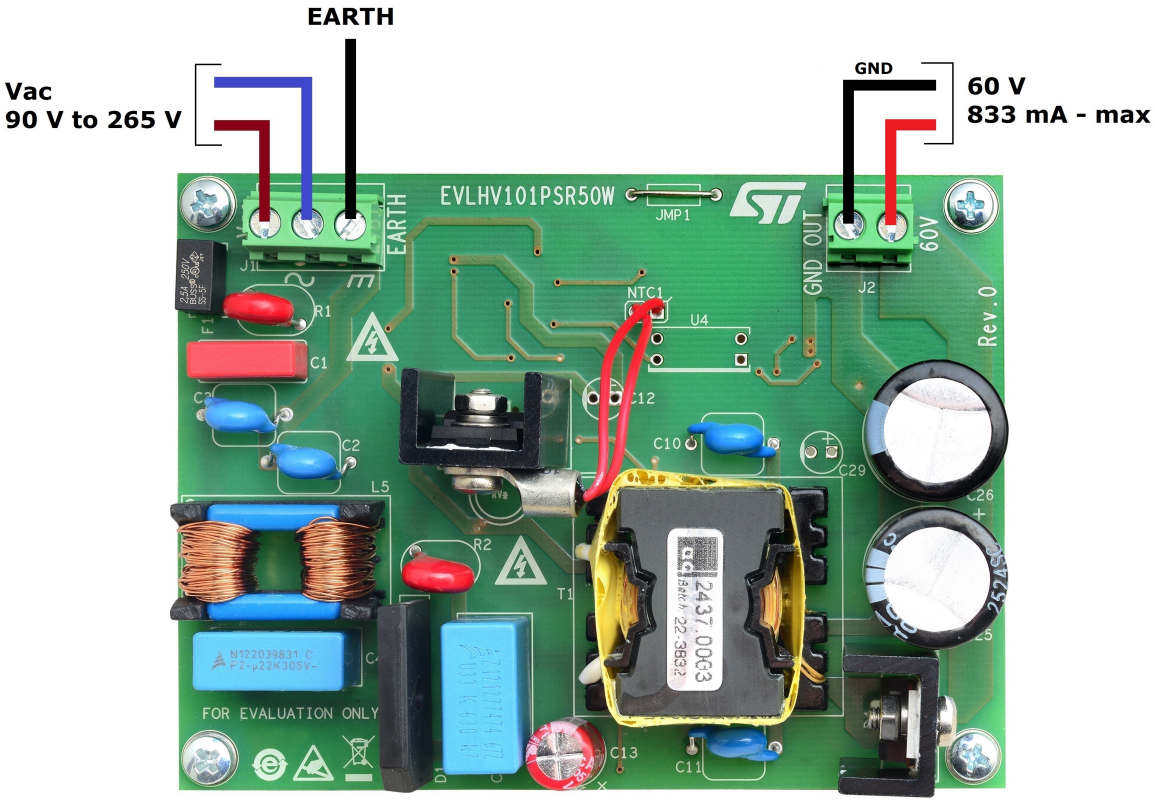


Figure 3. **Schematic diagram**

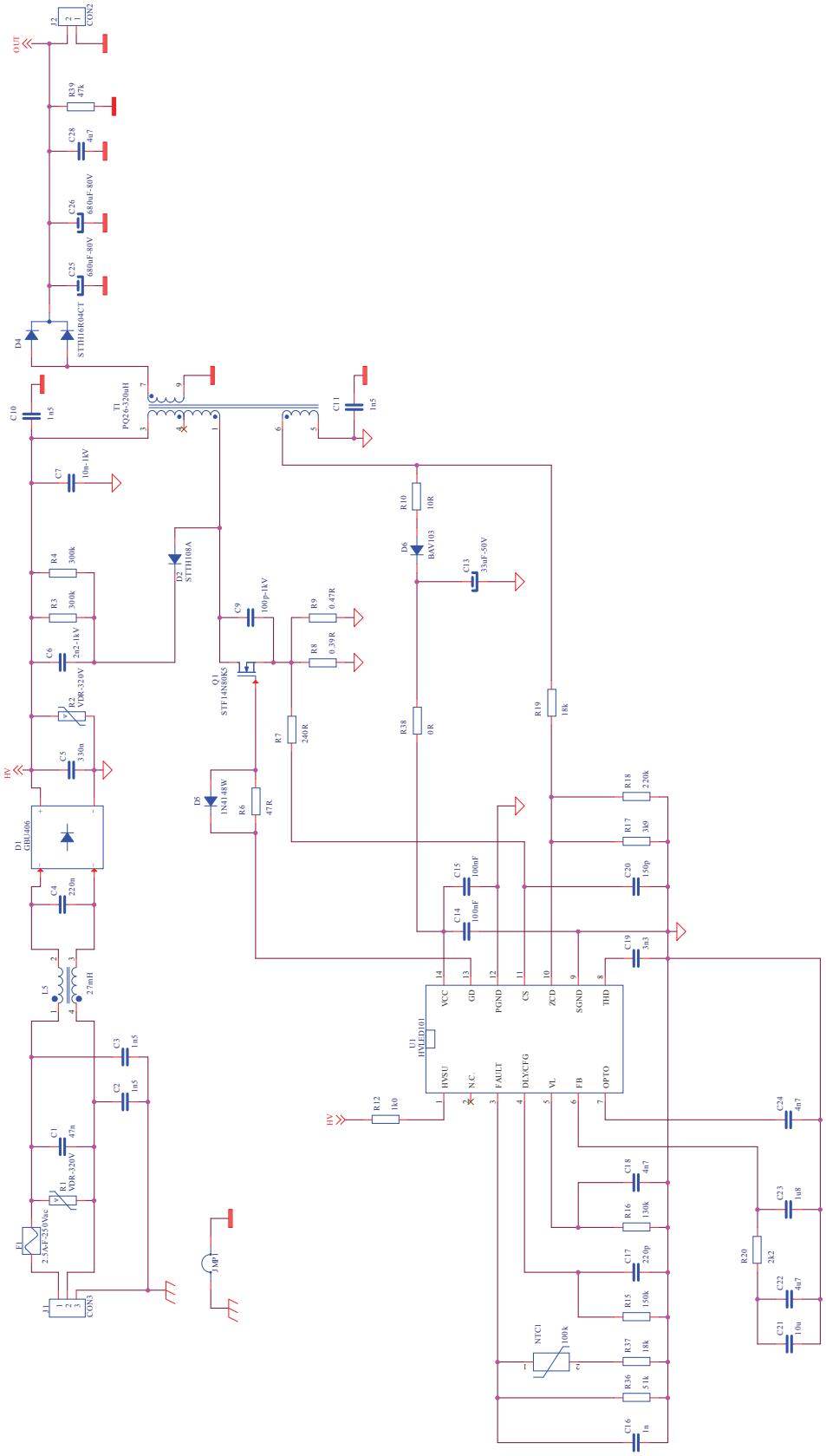


Table 3. Part list

Item	Q.ty	Ref. Des.	Value - Rating	Description	Manufacturer	Part number
1	1	C1	47n - 305V_{AC}	X2 film capacitor 305 V_{AC} (MKP)	Wurth	890334023015CS
2	2	C2, C3	1n5	X1-Y2 ceramic capacitor 440-300 V_{AC} CS series	TDK	CS75ZU2GA152MANKA
3	1	C4	220n - 305V_{AC}	X2 film capacitor 305 V_{AC} (MKP)	TDK	B32922C3224K
4	1	C5	330n	Polypropylene film capacitor 630 VDC-310 V_{AC}	TDK	B32672Z6334K000
5	1	C6	2n2 - 1kV	Multilayer ceramic capacitor X7R 1kV	AVX	1206AC222KAT1A
6	1	C7	10n - 1kV	Multilayer ceramic capacitor X7R 1kV	AVX	1812AC103KAT1A
7	1	C9	100p - 1kV	Multilayer ceramic capacitor C0G 1kV	AVX	1206AA101JAT1A
8	2	C10, C11	1n5 - 400V_{AC}	X1-Y1 ceramic capacitor 440-400 V_{AC} CD series	TDK	CD45-E2GA152M-NKA
9	1	C13	33u - 50V	Aluminum ELCAP - YXF series - 105°C	Wurth	860240674004
10	1	C14	100n - 50V	Cercap P X7R - SMD-0805	---	---
11	1	C15	100n - 50V	Cercap X7R - SMD-1206	---	---
12	1	C16	1n - 50V	Cercap X7R - SMD-0805	---	---
13	1	C17	220p - 50V	Cercap C0G -SMD-0805	---	---
14	2	C18, C24	4n7 - 50V	Cercap X7R -SMD-0805	---	---
15	1	C19	3n3 - 50V	Cercap X7R -SMD-0805	---	---
16	1	C20	150p - 50V	Cercap C0G -SMD-0805	---	---
17	1	C21	10u - 25V	Cercap X7R -SMD-1206	---	---
18	1	C22	4u7 - 25V	Cercap X7R - SMD-1206	---	---
19	1	C23	1u8 - 25V	Cercap X7R - SMD-0805	---	---
20	2	C25,C26	680uF - 80V	Aluminium ELECAP FS series - 105°C	Panasonic	EEUFS1K681
21	1	C28	4u7 - 100V	Cercap X7R - SMD-2020	AVX	22201C475KAT2A
22	1	D1	---	4A glass passivated bridge rectifier - GBU	Diodes Incorporated	GBU406
23	1	D2	---	High-voltage ultrafast rectifier 800 V - SMA	STMicroelectronics	STTH108A
24	1	D4	---	2X ultrafast recovery diode 400 V - TO220 AB	STMicroelectronics	STTH16R04CT
25	1	D5	---	Small signal switching diode - SOD-123	Vishay	1N4148W
26	1	D6	---	Small signal switching diode - SOD80 (MiniMELF)	Vishay	BAV103-GS18
27	1	F1	2.5A - 250V_{AC}	FUSE SS-5F series 2.5 A - 250 V_{AC} fast acting	Bussmann	SS-5F-2.5A
28	1	J1	---	PCB connector 3 PIN	Weidmuller	PM 5.08/03/90 3.5SN BK BX - 1760520000

Item	Q.ty	Ref. Des.	Value - Rating	Description	Manufacturer	Part number
29	1	J2	---	PCB connector 2 PIN	Weidmuller	PM 5.08/02/90 3.5SN BK BX - 1760510000
30	1	JMP1	---	Tinned copper wire jumper DIA 0.7MM	---	---
31	1	L5	27mH	27 mH common-mode choke filter	Epcos	B82732F2901B001
32	1	NTC1	100k	NTC - 100k - 1% - wired thermostat with metallic ring	Vishay	NTCALUG01A104FA
33	1	Q1	---	N-channel power MOSFET 800V 0.4 OHM	STMicroelectronics	STF14N80K5
34	2	R1,R2	VDR - 320V	Metal-oxide varistor LA series	Littelfuse	V320LA7P
35	2	R3,R4	300k - 200V	Stand. film RES - 1/4W - 5% - SMD-1206	---	---
36	1	R6	47R - 150V	Stand. film RES - 1/8W - 5% - SMD-0805	---	---
37	1	R7	240R - 200V	Stand. film RES - 1/4 W - 1% - SMD-1206	---	---
38	1	R8	0.39R - 200V	Stand. film RES - 1/4 W - 1% - SMD-1206	---	---
39	1	R9	0.47R - 200V	Stand. film RES - 1/4W - 1% - SMD-1206	---	---
40	1	R10	10R	Stand. film RES - 1/8W - 5% - SMD-0805	---	---
41	1	R12	1k0 - 150V	Stand. film RES - 1/8W - 5% - SMD-0805	---	---
42	1	R15	150k - 150V	Stand. film RES - 1/8W - 1% - SMD-0805	---	---
43	1	R16	130k - 150V	Stand. film RES - 1/8W - 1% - SMD-0805	---	---
44	1	R17	3k9 - 150V	Stand. film RES - 1/8W - 1% - SMD-0805	---	---
45	1	R18	220k - 150V	Stand. film RES - 1/8W - 1% - SMD-0805	---	---
46	2	R19, R37	18k - 150V	Stand. film RES - 1/8W - 1% - SMD-0805	---	---
47	1	R20	2k2 - 150V	Stand. film RES - 1/8W - 1% - SMD-0805	---	---
48	1	R36	51k - 150V	Stand. film RES - 1/8W - 5% - SMD-0805	---	---
49	1	R38	0R	Stand. film RES - SMD-0805	---	---
50	1	R39	47k - 200V	Stand. film RES - 1/4W - 1% - SMD-1206	---	---
51	1	T1	---	PQ26/22.5 flyback transformer 320 uH	Magnetica	Custom
52	1	U1	---	High power factor controller – HVLED101	STMicroelectronics	HVLED101

Figure 4. **EVLHV101PSR50W top side**

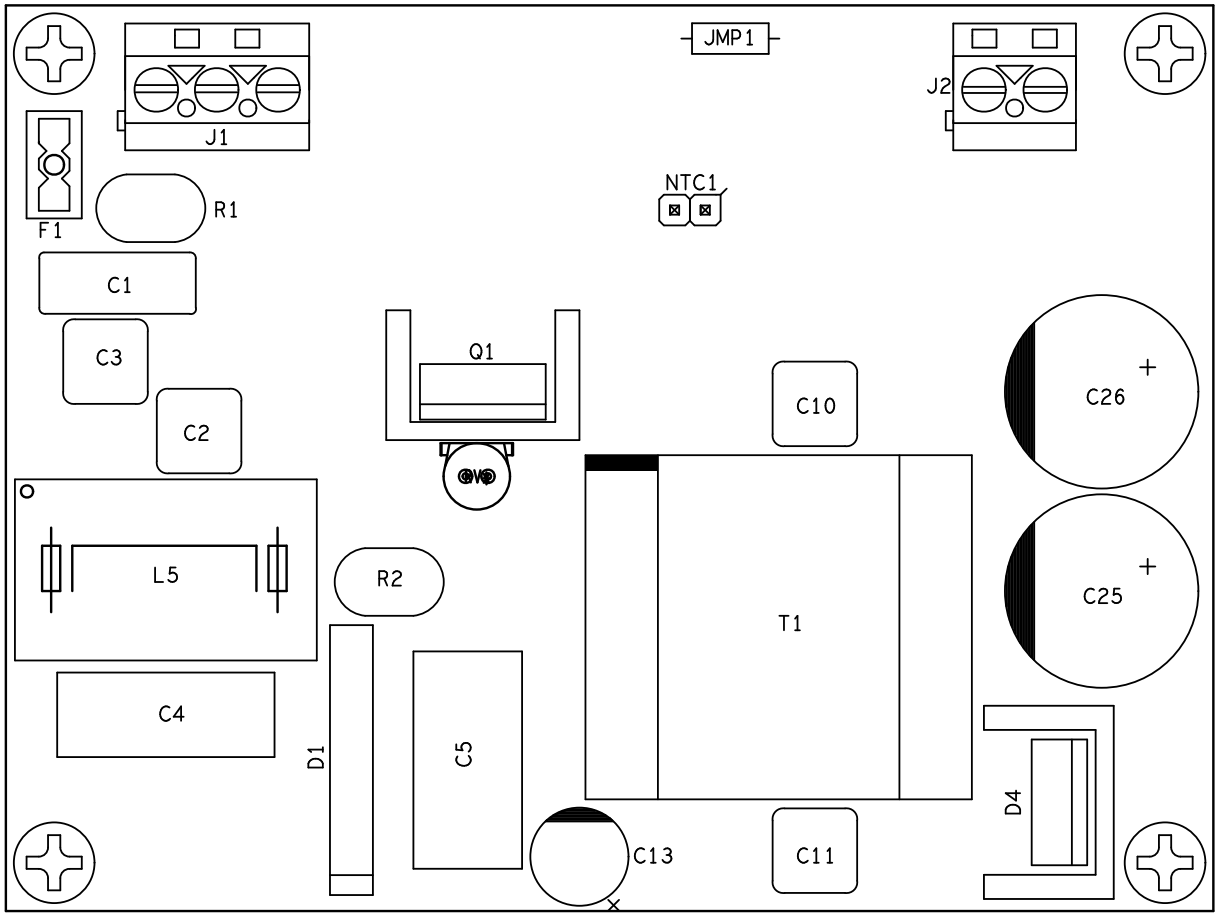
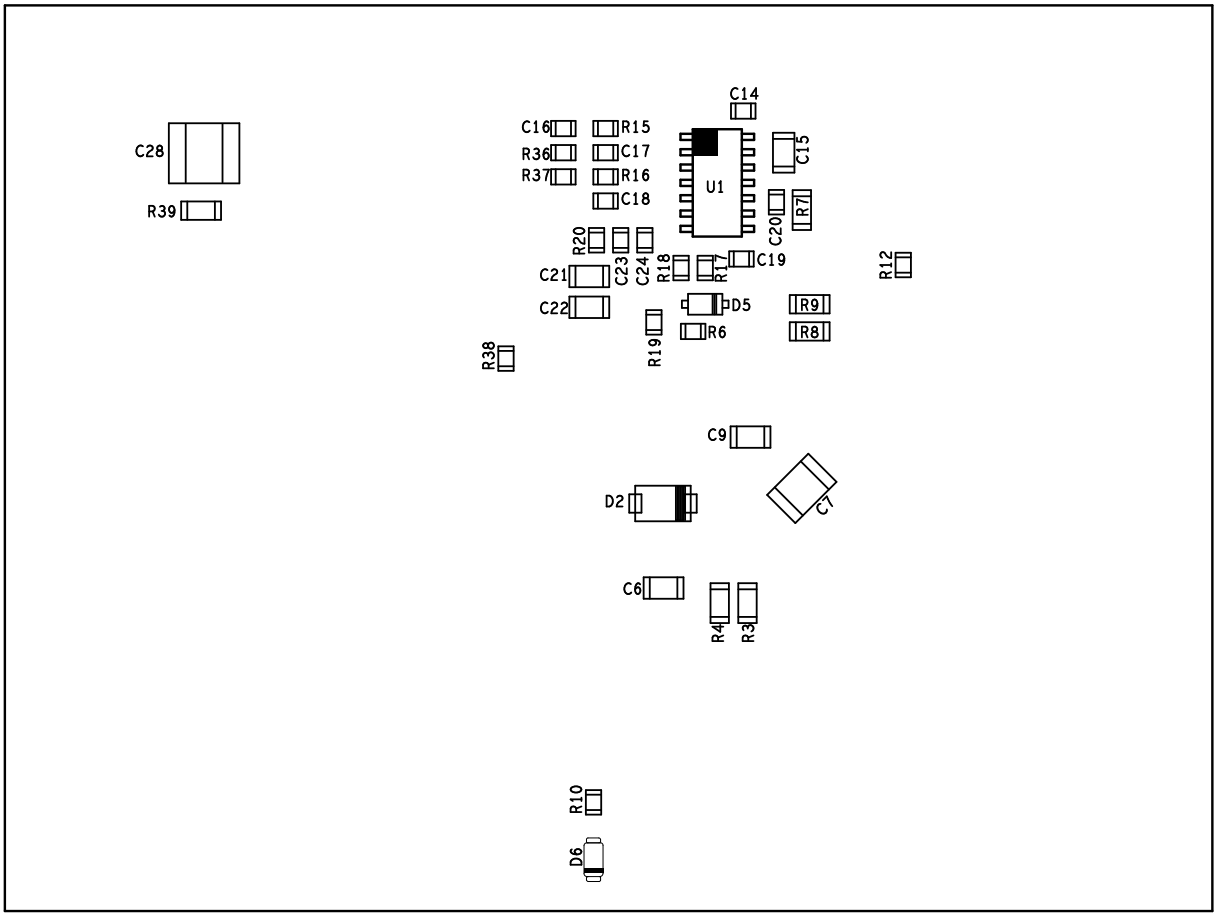


Figure 5. **EVLHV101PSR50W bottom side**



2 Flyback transformer specification

Figure 6. **Flyback transformer – electrical diagram**

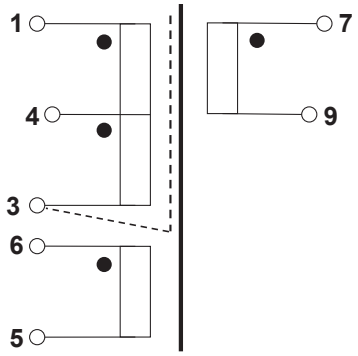


Table 4. **Flyback transformer - pins description**

No.	Description	Note
1	Primary drain	
2	Not connected	
3	Primary +Vb & Shield	
4	Pry. center tap	
5	Auxiliary ground	15 V - 25 mA
6	Auxiliary	
7	Secondary	60 V - 1.7 A
8	Not connected	
9	Secondary ground	
10	Not connected	
11	Not connected	
12	Not connected	

Note: Pin with the same subscript must be short circuited on the PCB.

Table 5. Flyback transformer – windings technical data

Parameter	Pin	Min.	Typ.	Max.	Um	Note
Inductance	1 - 3	272	320	368	µH	Measure 1KHz, T_A 20°C
	6 - 5	3.57	4.20	4.83	µH	
	7 - 9	56.33	66.27	76.21	µH	
Resistance	1 - 3	146	172	198	mΩ	Measure DC, T_A 20°C
	6 - 5	125	147	169	mΩ	
	7 - 9	127	149	171	mΩ	
Transformer ratio	1 - 3 → 6 - 5		9		-	Measure 100 kHz, T_A 20 °C
	1 - 3 → 7 - 9		2.21		-	

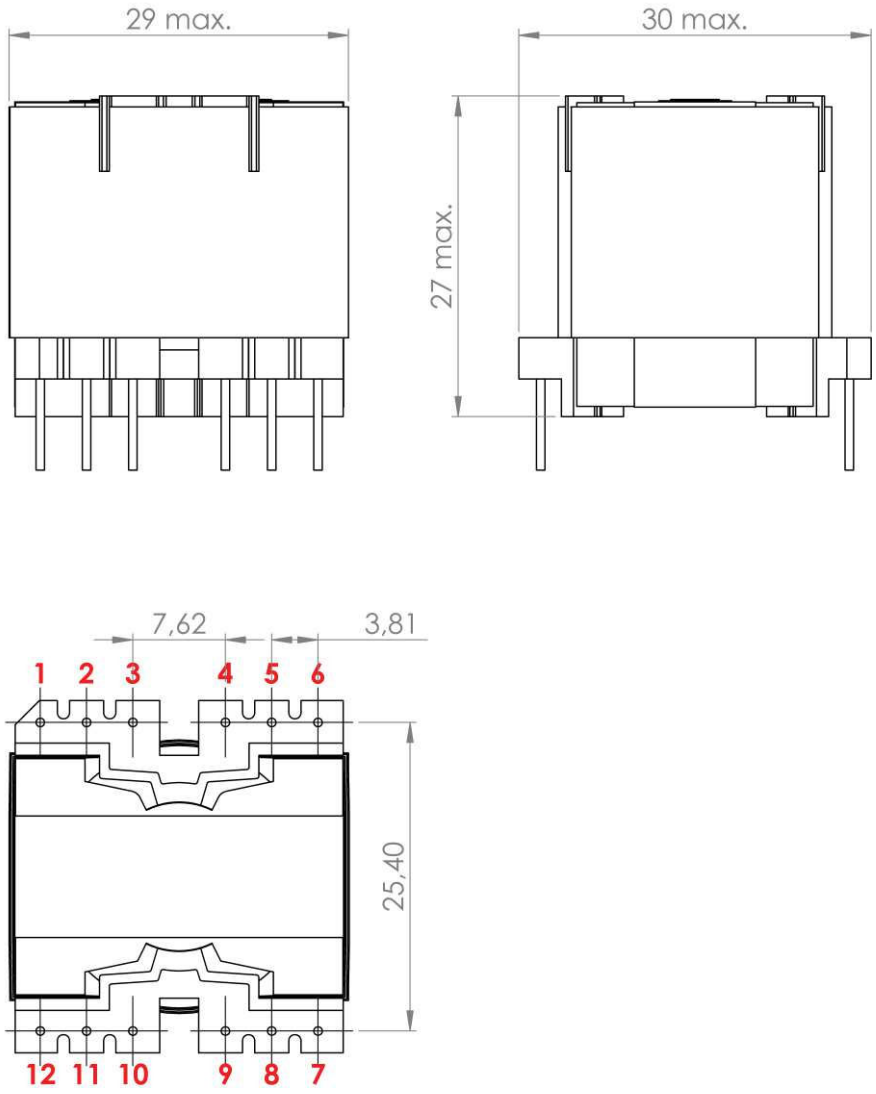
Table 6. Flyback transformer – electrical parameters

Parameter	Value	Um.	Note
Leakage inductance	2.88	µH	Measure 1-3, PIN 6-5 IN S.C., F 10KHz, T_A 20°C
Parasitic capacitance	16.1	pF	Measure 1-3, F_{RES} 2.20MHz, T_A 20°C
Operating current	3.7	Ap	Maximum peak current
Saturation current	6.2	A	Measure DC, L≥50% NOM, T_A 20°C
Operating frequency	60	kHz	Minimum frequency
Insulation	2.5	KV_{AC}	F 50Hz, test duration 2", T_A 20°C

Table 7. Flyback transformer – physical parameters

Parameter	Value	Um.	Note
Thermal class	B	-	
Ambient temp. range	-20 ÷ +85	°C	P_{MAX} 50W with max. self T_{rise} 45°C
Storage temp. range	-20 ÷ +85	°C	
Maximum dimensions	30 x 29 x H 27	mm	
Weight	45.4	g	

Figure 7. **Flyback transformer – mechanical aspect**



3 Circuit description and components selection

The EVLHV101PSR50W is a quasi-resonant High Power Factor (HPF) flyback converter working with Primary Side Regulation (PSR), so no external error amplifier and relevant optocoupler are required.

All of the control and protection required for the converter is integrated in the new HVLED101 quasi-resonant HPF flyback controller (U1) that enables the converter to draw a theoretically sinusoidal input current from the power line and adopts frequency foldback with valley locking operation to reduce the switching losses and minimize acoustic noise.

Here below the new features of the HVLED101 are described and the calculation of the relevant components is explained.

For the design and selection of power components it is possible to refer to a standard high power factor flyback (see, for example, AN4932). Using the HVLED101 allows more freedom in the selection of transformer primary inductance and reflected voltage with respect to the HVLED001A and B because of reduced ZCD blanking time and integrated THD optimizer.

- ***HVLED101 supply management and Line voltage monitoring function***

The HVLED101 is supplied applying a DC voltage source between the V_{CC} pin and PGND.

This voltage is obtained, during normal operation, by the primary auxiliary winding of the transformer (T1) through R10, D6, and C13.

At startup and during low consumption mode the IC is powered by the input voltage of the board that is applied to the HVSU pin using a low value resistor (R12 = 1 kΩ typ.).

The pin is internally connected to the high-voltage startup generator that starts its operation when the applied voltage is higher than 20 V (typ.). The charging current ensures a quick startup, independent of the voltage applied to the HVSU pin.

During operational mode, the input voltage is read through an internal resistor divider connected to the HVSU pin to obtain high power factor and to detect both input overvoltage and undervoltage, according to protection configuration, selected on the DLY/CFG pin (see Configuration programming and parameters selection).

- ***Primary side regulation feature***

The HVLED101 regulates the output voltage of the converter without the need of an error amplifier and relevant optocoupler.

The IC reads the Vout sensing the voltage developed across the primary auxiliary winding during the off-time of the MOSFET.

Primary auxiliary voltage, connected to the ZCD pin through the voltage divider R19 and R17//R18, is detected at the demagnetization instant and its amplitude is used as feedback signal to regulate the Vout.

In fact, the voltage present on the ZCD pin is compared to the reference voltage of the internal error amplifier (OTA) to generate the control voltage.

The ZCD network is composed by a simple resistor voltage divider, R19 and R17//R18.

R19 must be selected in order not to exceed the maximum ZCD pin current (I_{ZCDmax} from datasheet recommended **operating conditions**) during MOSFET on-time.

$$R19_{min} = \frac{V_{PKmax}}{I_{ZCDmax}} \cdot \frac{Naux}{Nprim} = \frac{\sqrt{2} \cdot 264V}{3mA} \cdot \frac{1}{9} = 13.8k\Omega \quad (1)$$

The selected R19 is 18 kΩ.

The lower part of the divider must be selected to regulate the desired output voltage according to the following equation:

$$R_{ZCDlow} = \frac{R19}{\frac{V_{OUT}}{V_{REF-PSR}} \cdot \frac{N_{aux}}{N_{sec}} - 1} = \frac{18k\Omega}{\frac{60}{2.6} \cdot \frac{1}{4} - 1} = 3.77k\Omega \quad (2)$$

Considering the standard resistor values and after having performed a fine-tuning on the real board, the following values have been chosen:

R17 = 3.9 kΩ

R18 = 220 kΩ

The output of the OTA is applied to a “MIN selection” block together with OPTO pin voltage and MPC internal signal (see Maximum power control (MPC)).

The output of this block is multiplied by the input voltage, opportunely scaled by the internal resistor divider connected to the HVSU pin and normalized to unity. The output of the multiplier passes through the THD optimizer, and its output is used as the threshold for the PWM comparator that turns off the power MOSFET (Q1) when the voltage across the primary current sense resistor (R8//R9) reaches that reference.

The output of the OTA is brought to external through the FB pin where the type 2 compensation network (C23//R20 + C22) is connected.

The pole is placed at a very low frequency so that the gain at twice line frequency is notably less than unity, while the zero boosts the phase in the neighborhood of the open-loop crossover frequency to provide a good phase margin.

The THD optimization unit is placed between the multiplier output and the current sense threshold limiter to minimize the distortion of the absorbed AC current (THD) and to maximize the Power Factor (PF).

This unit uses the external capacitor C19, connected between the THD pin and GND to filter the switching frequency from the VCS threshold. The value of such a capacitor must be selected according to the following relationship:

$$C19 = \frac{4}{R_{THD} \cdot f_{SW.min}} \quad (3)$$

Where:

R_{THD} is the THD optimizer internal resistor and $f_{SW.min}$ is the minimum switching frequency.

For the EVLHV101PSR50W, the calculation is the following:

$$C19 = \frac{4}{22k\Omega * 70kHz} = 2.597nF \rightarrow 3n3F \quad (4)$$

The OPTO pin is not used, and it is pulled up internally. A small filter capacitor (C24 = 4.7 nF) is placed between the pin and GND to prevent possible noise pickup.

- ***Maximum power control (MPC)***

Maximum input power is automatically limited by the HVLED101 internal algorithm (MPC), which helps increase system safety.

The MPC defines the value of the primary current sense resistor R8//R9 according to the following equation:

$$R8//R9 = \frac{K_M \cdot K_{MPC}}{4 \cdot P_{in-lim}} \quad (5)$$

Where:

KM is the multiplier gain = 0.176 V/V.

KMPC is the scaling factor = 270 V^2.

P_{in-lim} is the required limiting input power.

P_{in-lim} can be calculated by considering the maximum output power and an efficiency of 0.9.

MPC block automatically detects if input voltage is AC or DC and applies the correct gain to have the required power limitation in both cases.

For the EVLHV101PSR50W, the calculation for primary current sense resistor is the following:

$$R8//R9 = \frac{0.176\frac{V}{V} \cdot 270V^2}{4 \cdot \frac{50W}{0.9}} = 0.213\Omega \quad (6)$$

Selected values are:

R8 = 0.39 Ω

R9 = 0.47 Ω

- ***Frequency foldback with valley locking operation***

The HVLED101 adopts frequency foldback with valley locking operation to reduce the switching losses and avoid acoustic noise. The level of the frequency foldback depth is determined by the voltage on the VL pin (proportional to control voltage) which is compared to the VL1-VL6 internal thresholds defining the number of valleys skipped.

The resistor R16 allows the tuning of VL voltage, and consequently the number of valleys skipped, according to the following relationship:

$$R16_{max} = \frac{VL_x}{K_{LV1}\left(\frac{4}{\sqrt{2}*V_{IN}}*\frac{P_{out}}{\eta}*\frac{R8//R9}{K_M} + V_{OS}\right)} \quad (7)$$

Where:

VLx is the valley threshold, internal to the IC, which is compared to the voltage on the VL pin.

K_{LV1} is the valley lock block gain (10 uA/V, it can be derived from the datasheet parameter $I_{VL\text{-}P\text{-}UP}$: if V_{OPTO} changes from 1 V to 2 V, the VL current changes from 10 uA to 20 uA.).

K_M is the multiplier gain = 0.176 V/V.

V_{OS} is the FB and OPTO pin internal offset.

V_{IN} is the AC mains voltage at the input of the board.

Pout is the output power.

η is the expected efficiency.

R8//R9 are the primary sensing resistors.

A fine-tuning of the R16 resistor may be required.

EVLHV101PSR50W has been designed to skip one valley at full load and V_{IN} = 230 V_{AC}.

The relevant VLx threshold is therefore VL1 and so the calculation is the following:

$$R16_{max} = \frac{1.75V}{10\mu A/V*\left(\frac{4}{\sqrt{2}*230V}*\frac{50W}{0.9}*\frac{0.213\Omega}{0.176V/V} + 0.5V\right)} = 131894\Omega \rightarrow 130\text{k}\Omega \quad (8)$$

As the load decreases, the voltage on the VL pin (proportional to control voltage) drops, and the HVLED101 increases the number of valleys skipped.

The controller stays locked in a valley until the load changes significantly.

After skipping 6 valleys, the system operates in discontinuous conduction mode (DCM) and when the output power is very small, the flyback converter enters burst-mode operation to maintain the output regulation.

If the V_{IN} changes, the HVLED101 adjusts the frequency foldback depth accordingly.

At V_{IN} = 115 V_{AC} with full load the system operates in transition mode and starts to skip the valleys when the load decreases.

- ***PSR burst-mode operation***

When the load is very light, the FB pin voltage decreases below V_{BM} threshold, the HVLED101 enters burst-mode operation (deep low-consumption mode), and the IC starts the dedicated burst-mode algorithm. The burst-mode algorithm provides 4 consecutive switching cycles with a repetition time T_{REP} whose duration is inversely proportional to FB pin voltage.

As the control loop forces FB pin voltage above V_{BM}+V_{BM_HYST}, the normal mode operation is restored.

- ***Configuration programming and parameters selection***

MOSFET (Q1) always turns on when the demagnetization occurs, but in order to minimize the switching losses it is convenient to turn on the MOSFET on the minimal oscillation (valley switching).

In the HVLED101, this is achieved by programming the delay time (T_{DLY}) between ZCD detection and MOSFET turn-on by means of R15 connected to the DLY/CFG pin.

The required T_{DLY} can be calculated starting from the frequency ringing after demagnetization as follows:

$$f_{ring} = \frac{1}{2\pi*\sqrt{L_P*C_{DRAIN}}} \quad (9)$$

Where:

Lp is primary inductance of transformer.

C_{DRAIN} is the estimated total drain node capacitance.

$$T_{ring} = 2\pi*\sqrt{L_P*C_{DRAIN}} \quad (10)$$

$$T_{dly} = \frac{T_{ring}}{4} \quad (11)$$

For EVLHV101PSR50W, the calculations are as follows:

$$f_{ring} = \frac{1}{2*3.14*\sqrt{320\mu H*200nF}} = 628.115kHz \quad (12)$$

$$T_{ring} = 2*3.14*\sqrt{320\mu H*200nF} = 1.59\mu s \quad (13)$$

$$T_{dly} = \frac{1.59\mu s}{4} = 397.384ns \quad (14)$$

The relationship between the required T_{DLY} and R15 is expressed by the following formula:

$$R15 = \frac{T_{dly} - T_{dly0}}{K_{dly}} \quad (15)$$

Where:

T_{DLY0} is the minimum delay time, 100 ns.

K_{DLY0} is ZCD to GD on gain, 2.13 ns/kΩ.

For EVLHV101PSR50W, the calculation is the following:

$$R15 = \frac{397.384ns - 100ns}{2.13ns/k\Omega} = 139.617k\Omega \quad (16)$$

Considering the standard resistor values, after a fine-tuning on the real board 150 kΩ has been chosen.

The actual T_{DLY} programmed is:

$$T_{dly} = \left(K_{dly}{}^{*}R15\right) + T_{dly0} = 419.5ns \quad (17)$$

Maximum waiting time (T_{WAIT}) is proportional to the programmed delay time (T_{DLY}) configured by R15 as per the following relationship:

$$T_{wait} = 8^{*}\left(T_{dly} - T_{dly0}\right) + T_{dly0} \quad (18)$$

$$T_{wait} = 8^{*}(419.5ns - 100ns) + 100ns = 2.656\mu s \quad (19)$$

The HVLED101 can be programmed with 5 different configurations of input range, brownout, and surge protections according to user needs (CFG1-CFG5).

Configuration can be chosen selecting the value of the time constant (Tau_{CFGn}) associated with the RC network placed between DLY/CFG and GND.

Table 8. Programming configurations

Tau_{CFGn} (µs)	CFG	iOVP	BrOut	K_{HV}	DC Det.	I_{BLEED} @ iOVP
30µs ... 45 µs	CFG1	ON	Low	High	Low	ON
100 µs ... 140 µs	CFG2	OFF	OFF	Low	Low	N.A.
300 µs ... 410 µs	CFG3	ON	High	High	High	ON
860 µs ... 1.2 ms	CFG4	OFF	Low	Low	Low	N.A.
> 2.05 ms	CFG5	ON	Low	High	Low	OFF

Note that CFG2 has the brownout detection disabled. This is intended to be used mainly for debug purposes because an input voltage lower than 80 V could lead to unpredictable V_{out} behavior.

The following table summarizes the suggested combination of R_{DLY} and C_{CFG} to obtain both delay time and configuration programming.

Table 9. **Suggested R_{DLY} - C_{CFG} programming values**

T_{DLY} (ns)	R_{DLY} (kΩ) (1%)	C_{DLY} (nF) (5% - >6.3V rated)				
		CFG1	*CFG2*	*CFG3*	*CFG4*	*CFG5*
163.9	30	1.2n	3.9n	12n	33n	82n
183.1	39	1n	2.7n	8.2n	27n	56n
219.3	56	680p	2.2n	6.2n	18n	39n
259.8	75	470p	1.5n	4.7n	12n	33n
355.6	120	270p	1n	2.7n	8.2n	18n
419.5	150	220p	680p	2.2n	6.8n	15n
483.4	180	180p	560p	1.8n	5.6n	12n
568.6	220	150p	470p	1.5n	4.7n	10n
675.1	270	120p	390p	1.2n	3.3n	8.2n
802.9	330	100p	330p	1n	2.7n	6.8n
1101.1	470	82p	220p	680p	2.2n	4.7n
1292.8	560	68p	180p	560p	1.8n	3.9n

On the EVLHV101PSR50W, R_{DLY} = R15 is 150 k ohm to fix T_{DLY} = 419.5 ns, and the C_{CFG} = C17 is 220 pF to select CFG1 configuration, suggested for universal input range (90 V_{AC} – 305 V_{AC}).

Protections

The HVLED101 provides a set of protections for safe and reliable operation of the application also during abnormal conditions.

The following protections are provided:

- 2nd overcurrent protection (2nd OCP).
- Input overvoltage protection (iOVP - against input voltage surge).
- Brownout protection (against insufficient input voltage).
- Output undervoltage protection.

In the HVLED101, the information on the input voltage is read through the HVSU pin, which is connected to the bridge diodes D1 through the series resistor R12.

When the voltage input (V_{IN}) decreases below the brownout threshold (V_{BO}) for a time longer than the brownout activation time (T_{BO}), the protection is entered: the IC stops switching and the high-voltage startup current generator is activated periodically to charge V_{CC} between V_{CC-OFF} and V_{CC-ON} to keep the IC alive, using the highest current level (I_{CHG-H}).

During the charging phase, the IC monitors the HVSU pin, whose voltage is the input reduced by the drop on the R12 resistor. If the measured voltage goes over the brownout threshold again, the device restarts when V_{CC} reaches V_{CC-ON} threshold.

The voltage drop on R12 represents therefore the hysteresis between brownout and brown-in and its value has to be chosen to have a correct amount of such hysteresis.

When the IC sources I_{CHG-H} to the V_{CC} pin, it sinks about 7 mA from the HVSU pin.

In the EVLHV101PSR50W demonstration board, R12 = 1 kΩ provides about 7 V of hysteresis on the peak of V_{IN}, that is, about 5 V_{AC}.

This is usually acceptable for most applications. In case a different hysteresis may be required, it is sufficient to modify accordingly the value of the HVSU series resistor.

The HVLED101 also embeds the general-purpose FAULT pin, intended to disable the switching activity and to move the IC into low consumption if the voltage on this pin falls below the $V_{FLT-OFF}$ threshold or it is left floating.

The FAULT pin is mainly used to manage an NTC thermistor: in fact, the lower threshold has a well-defined hysteresis and the pin sources a precise current (50 uA) to create the desired thermal hysteresis for final application.

On the EVLHV101PSR50W, the NTC1 is physically located on the dissipator of the switching MOSFET (Q1) and it is linearized using a resistor network consisting of one resistor in series (R37) and one in parallel (R38).

The design has been done so that the value of FAULT voltage is equal to $V_{FLT-OFF}$ (thermal protection activated) at about 100 °C.

If NTC is not used, a fixed resistor (22 kΩ to 47 kΩ) must be connected to GND.

The small capacitor C16 (1nF) connected from pin to ground reduces switching noise pick-up helping obtain clean operation.

The limit on the maximum capacitance value stems from the fact that the internal current generator is switched off during the idle periods of burst-mode operation. During these time intervals, the FAULT voltage falls to zero and it takes some time (dependent on the time constant of the RC network connected to it) for the voltage to be pulled up and to reach its final value.

The generator is turned back on about 120 us before the 4 consecutive switching cycles where the voltage on the FAULT pin is read, so the V_{FLT-ON} threshold must be exceeded before the end of the 120 µs latency (see Figure 8 and Figure 9).

The time constant of the equivalent resistance of the NTC and linearizing resistors with the filtering capacitor must be low enough to fulfill the above condition. This must be verified for all the values that the NTC may have during operation (that is, over all temperature operating range).

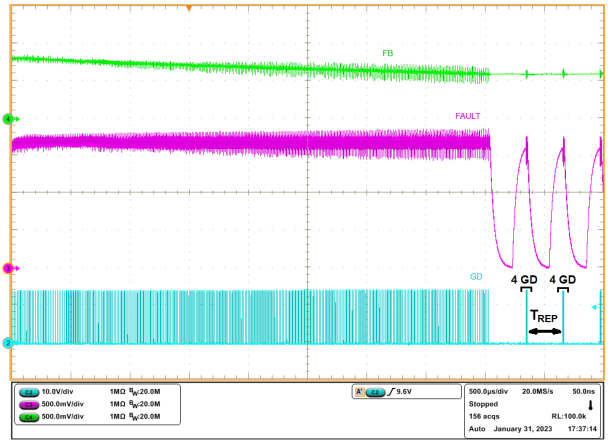
The following images show the behavior of the FAULT pin taken on the EVLHV101PSR50W demo board.

CH2 – blue = GD gate driver pin

CH3 – red = FAULT pin

CH4 – green = FB pin

Figure 8. FAULT pin behavior burst mode



In Figure 8 the IC enters in burst mode and the FAULT voltage drops to zero during idle periods.

Figure 9. FAULT pin zoom at switching restart

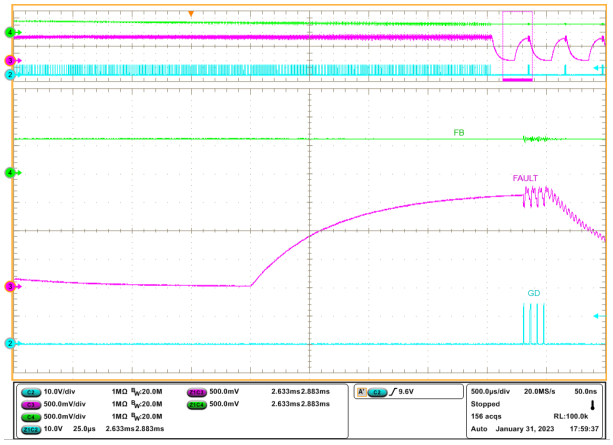


Figure 9 zooms in on the FAULT voltage rising and overcoming the V_{FLT-ON} threshold (850 mV) before the 4 consecutive switching cycles.

4 Test results

In this section, efficiency, THD, and power factor measurements, under different line and load conditions, are reported.

The output voltage has been measured with a voltmeter on connector J2, while the current is measured with an amperometer.

THD, PF, and the input power have been captured using a digital power meter, while the output power has been calculated as the product between V_{OUT} and I_{OUT}.

Table 10. Efficiency

Load [%]	I_{out} [mA]	V_{out} [V]	P_{out} [W]	P_{in} [W]	THD [%]	PF	η [%]
V_{IN} = 90 V_{AC} / 50 Hz							
10	83	59.39	4.93	5.67	7.00	0.9869	87.00
25	208	59.39	12.35	13.65	4.70	0.9979	90.53
33	278	59.39	16.51	18.16	4.88	0.9980	90.94
50	417	59.39	24.77	27.18	4.12	0.9979	91.13
75	625	59.39	37.12	40.70	4.41	0.9976	91.21
100	833	59.42	49.50	54.64	3.51	0.9969	90.59
4 points avg.							90.86
V_{IN} = 115 V_{AC} / 60 Hz							
10	83	59.31	4.92	5.68	10.95	0.9476	86.62
25	208	59.35	12.34	13.57	5.90	0.9950	90.95
33	278	59.38	16.51	17.99	5.30	0.9975	91.74
50	417	59.37	24.76	26.91	5.20	0.9982	91.99
75	625	59.37	37.11	40.32	5.70	0.9977	92.02
100	833	59.40	49.48	53.94	4.90	0.9972	91.73
4 points avg.							91.67
V_{IN} = 230 V_{AC} / 50 Hz							
10	83	59.45	4.93	5.82	30.25	0.5575	89.92
25	208	59.39	12.35	13.70	9.50	0.8992	90.15
33	278	59.37	16.50	18.09	7.30	0.9390	91.22
50	417	59.39	24.77	26.98	6.20	0.9768	91.78
75	625	59.41	37.13	40.17	5.40	0.9913	92.43
100	833	59.40	49.48	53.43	4.70	0.9961	92.60
4 points avg.							91.73
V_{IN} = 265 V_{AC} / 50 Hz							
10	83	59.36	4.93	5.88	35.75	0.4655	83.72
25	208	59.36	12.35	13.87	11.70	0.8402	88.99
33	278	59.40	16.51	18.29	8.91	0.8929	90.26
50	417	59.41	24.77	27.10	6.55	0.9584	91.40
75	625	59.41	37.13	40.29	5.15	0.9851	92.15
100	833	59.43	49.51	53.54	4.35	0.9926	92.46
4 points avg.							91.25

Figure 10. **Load regulation**

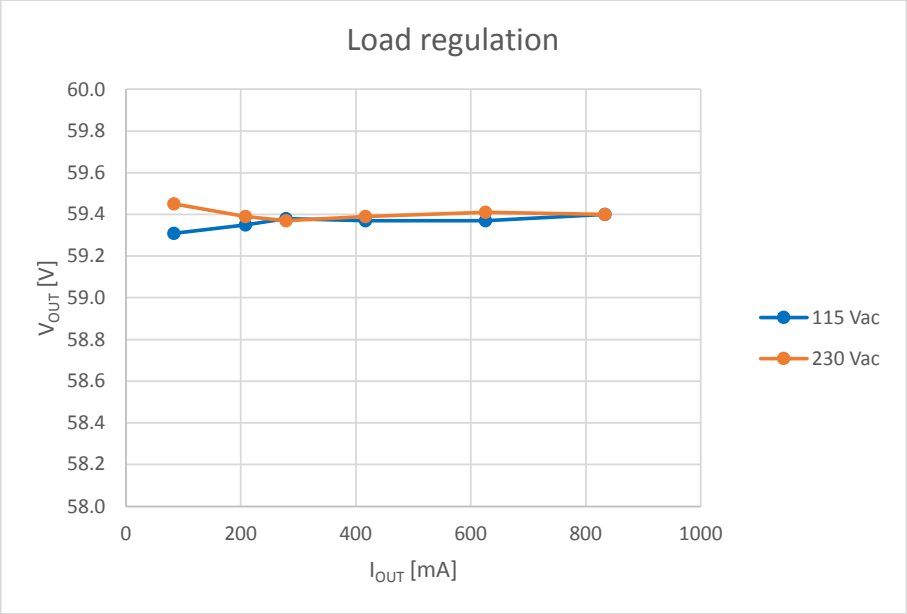


Figure 11. **Efficiency**

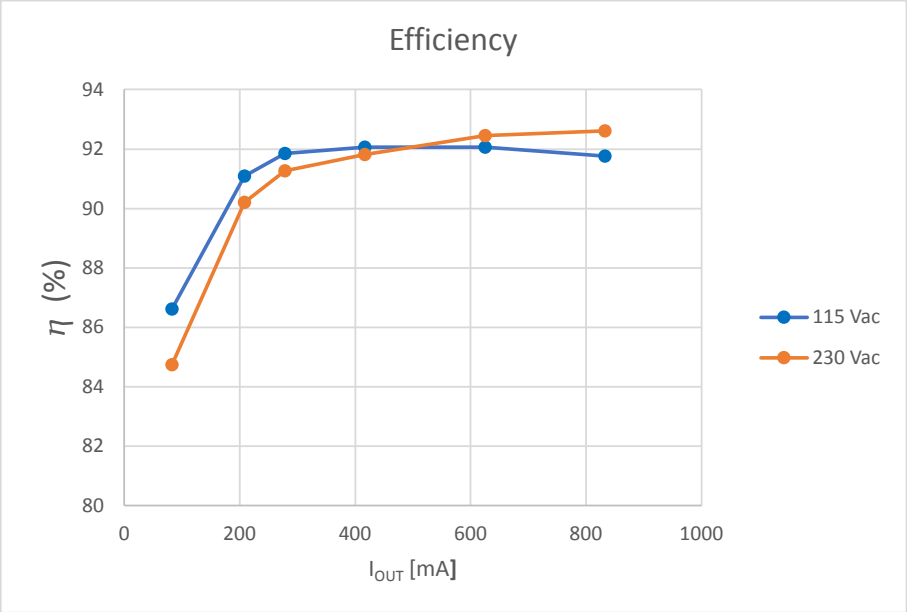


Figure 12. **THD**

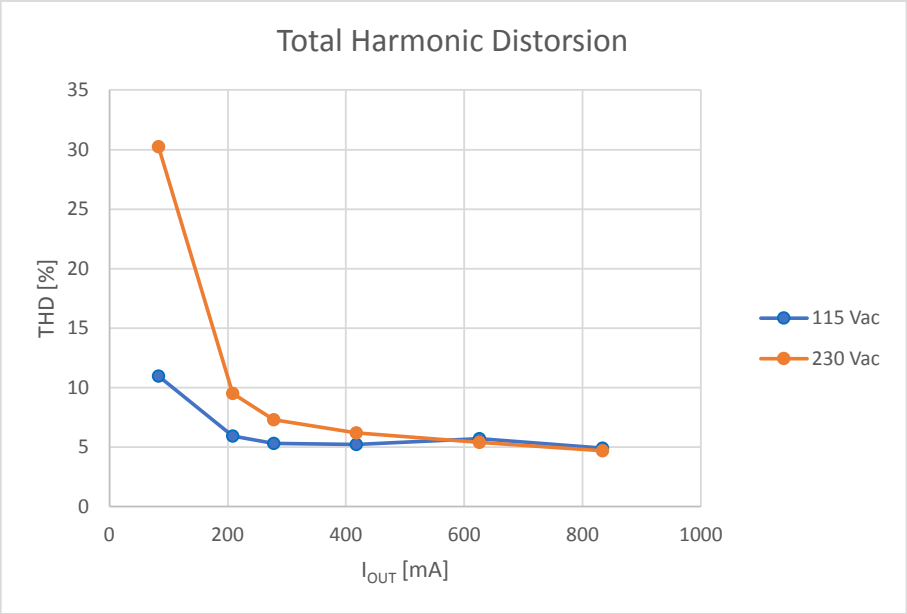


Figure 13. **Power factor**

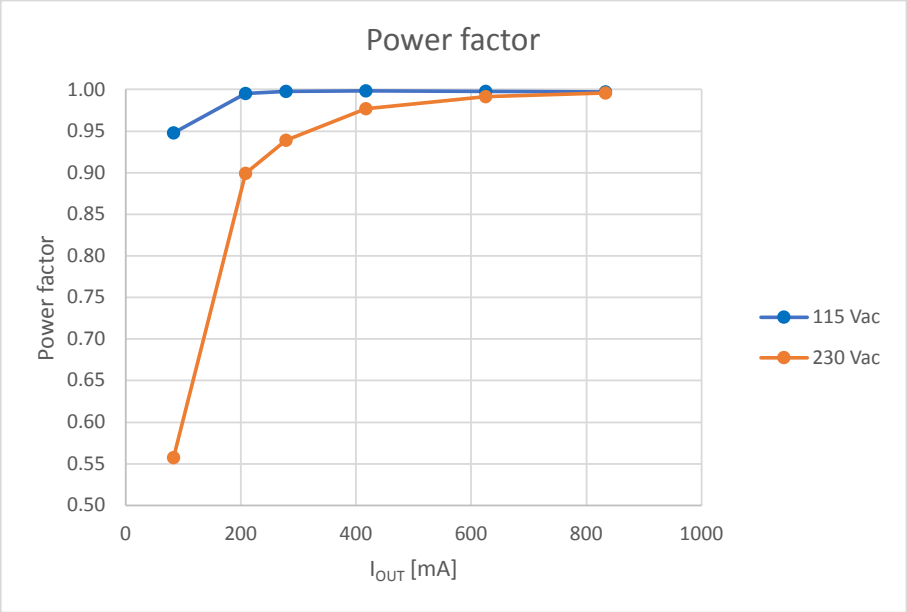


Figure 14. THD vs. V_{IN}

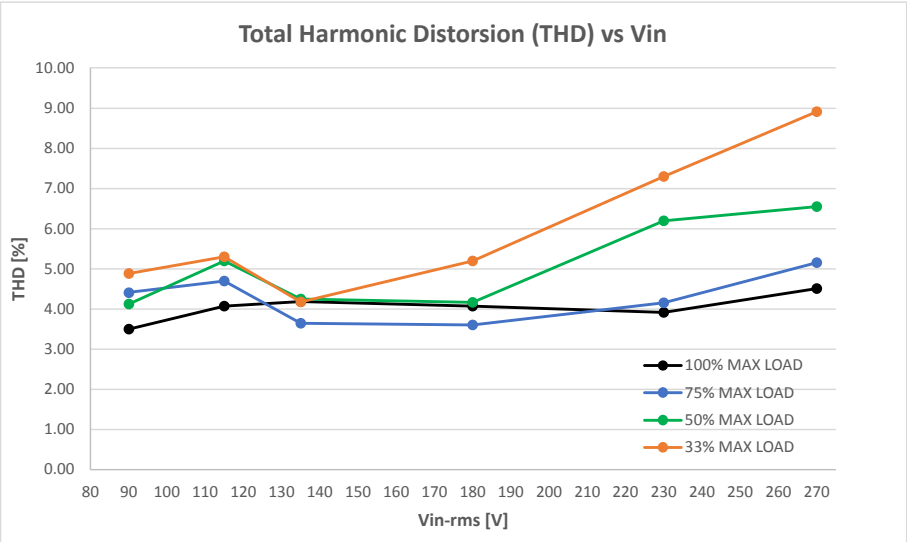


Figure 15. Power factor (PF) vs. V_{IN}

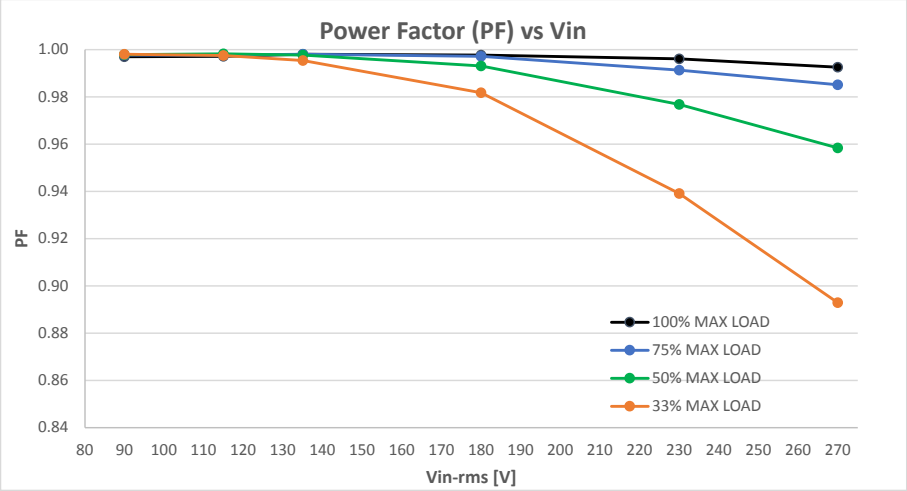
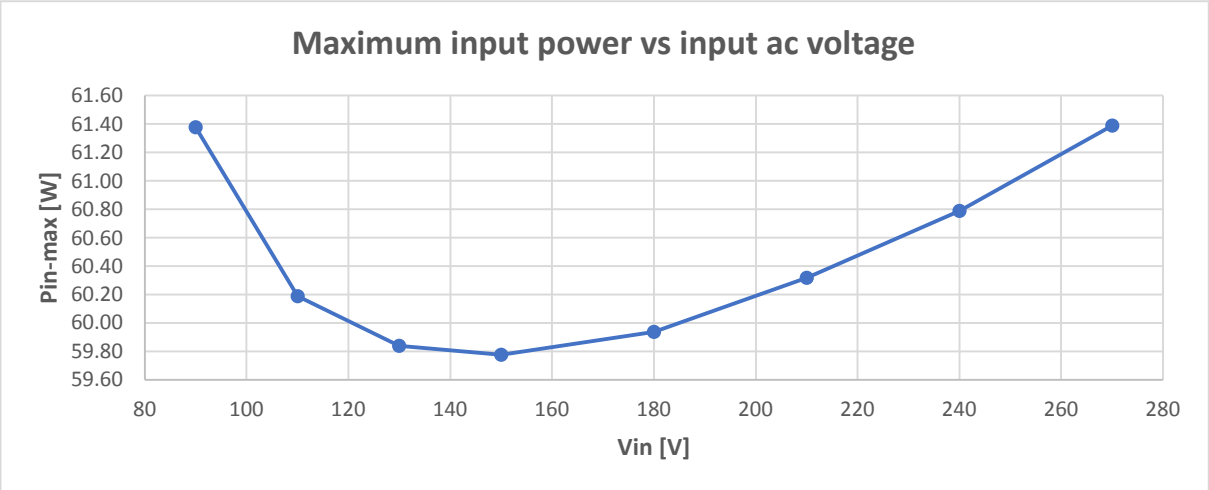


Figure 16. Pin-max vs. V_{IN}



5 No-load and standby consumption

The consumption of EVLHV101PSR50W in no-load and standby conditions at 115 V_{AC} and 230 V_{AC} are now reported. The measurements have been performed in the following ways:

- Consumption in no-load condition, nothing is connected to connector J2.
- Consumption in standby, 4.6 mA current is drawn from the output connector J2 (POUT= 4.6 mA * 60 V = 270 mW).

Table 11. No-load and standby consumption

Conditions	V_{IN} = 115 V_{AC}	V_{IN} = 230 V_{AC}
No-load	P_{IN} [mW]	P_{IN} [mW]
	185	132
Standby	419	415

6 Startup and steady-state

During the startup phase, the HVLED101 is able to control the input current in order to reduce the stress on all power components and provides a smooth rise of the output voltage.

The waveforms confirm that HVLED101 is able to achieve sinusoidal input current (extremely low THD).

Figures Figure 17, Figure 18, Figure 19 and Figure 20 show the startup phase and steady-state at full load with 115 V_{AC} and 230 V_{AC} input voltages.

In the following figures:

- CH1 – yellow = CS current sense pin
- CH2 – blue = V_{OUT}
- CH3 – red = HVSU pin
- CH4 – green = Input current

Figure 17. Startup at 115 V_{AC}, 100% load

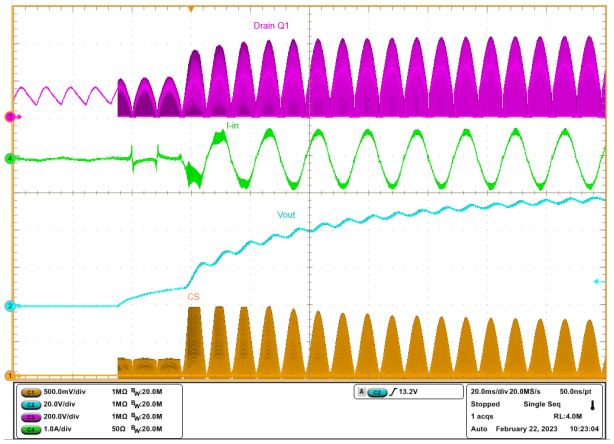


Figure 18. Steady-state at 115 V_{AC}, 100%

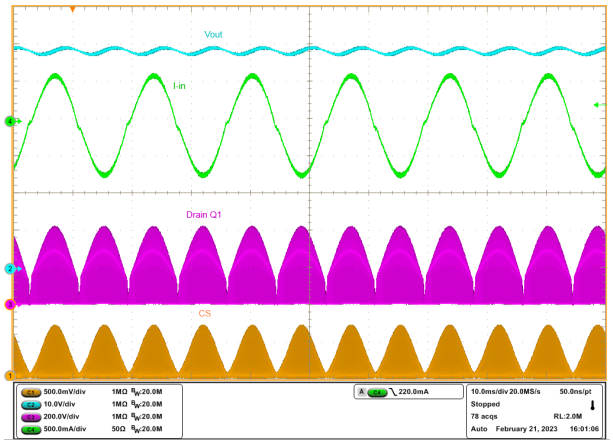


Figure 19. Startup at 230 V_{AC}, 100% load

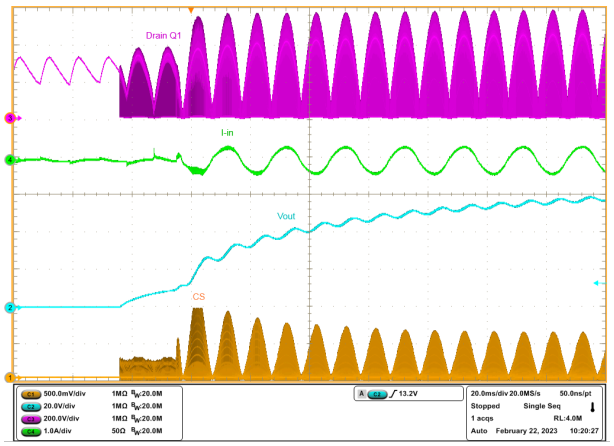
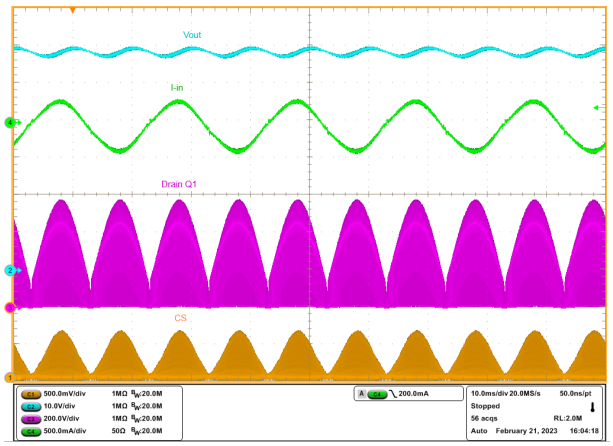


Figure 20. Steady-state at 230 V_{AC}, 100%



6.1 Startup at 90 V_{AC} with different load conditions

The HVLED101 embeds an 800 V startup structure that allows the fast startup of the system.
On the EVLHV101PSR50W, the startup time is always lower than 200 ms in all V_{IN} and load conditions.

In the following figures:

- CH1 – yellow = CS current sense pin
- CH2 – blue = V_{OUT}
- CH3 – red = V_{CC} pin
- CH4 – green = V_{AC} mains

Figure 21. Startup at 90 V_{AC}, 100% load

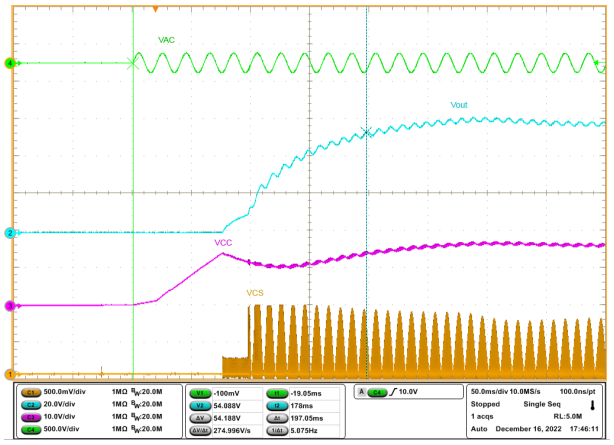


Figure 22. Startup at 90 V_{AC}, 75% load

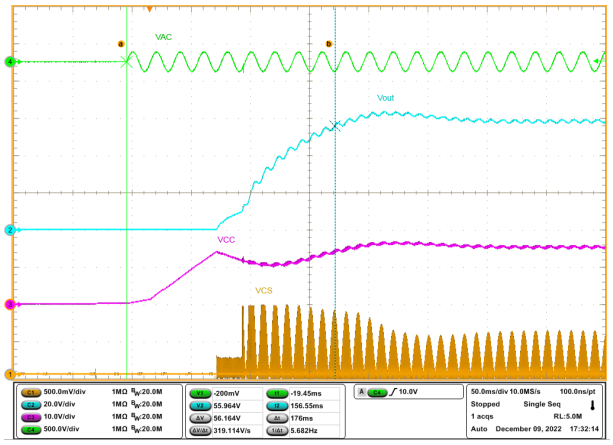


Figure 23. Startup at 90 V_{AC}, 50% load

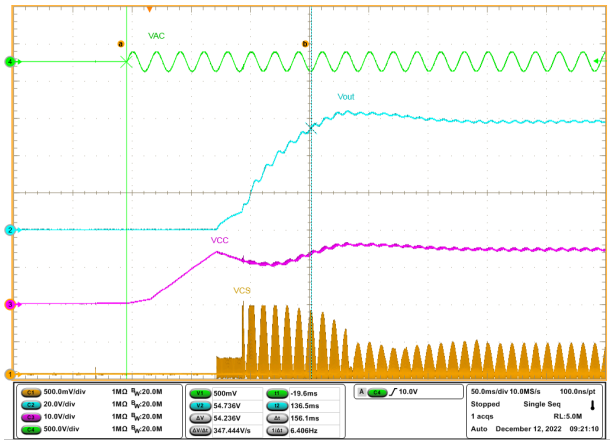


Figure 24. Startup at 90 V_{AC}, 25% load

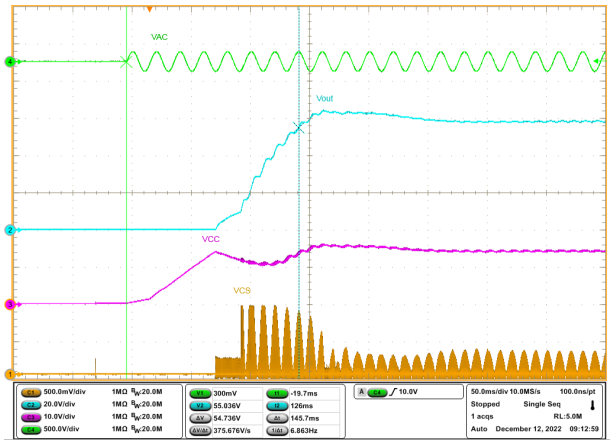


Figure 25. Startup at 90 V_{AC}, 270 mW load

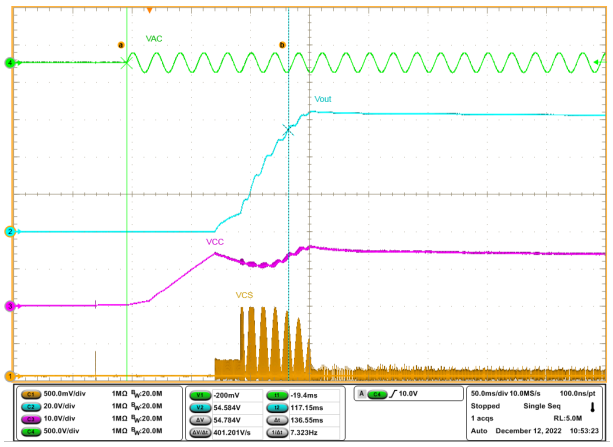
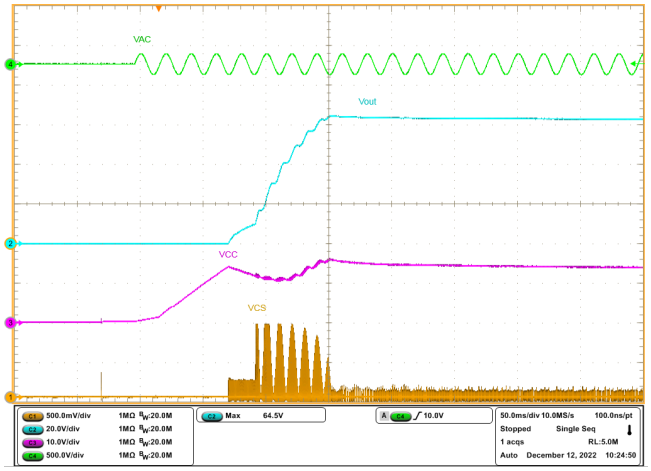


Figure 26. Startup at 90 V_{AC}, no load



6.2 Startup at 115 V_{AC} with different load conditions

Figure 27. Startup at 115 V_{AC}, 100% load

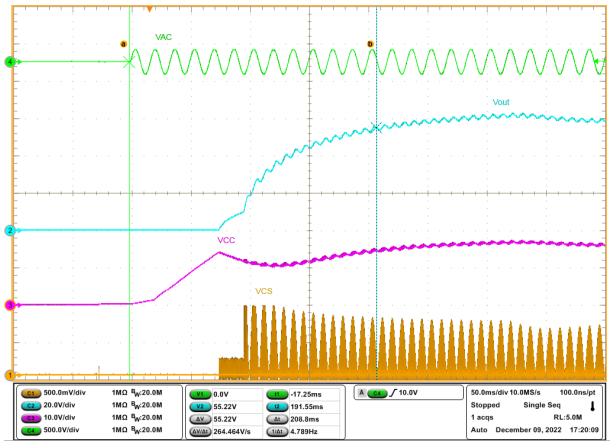


Figure 28. Startup at 115 V_{AC}, 75% load

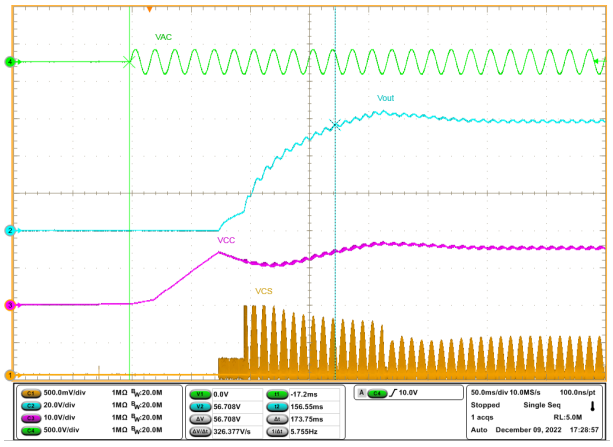


Figure 29. Startup at 115 V_{AC}, 50% load

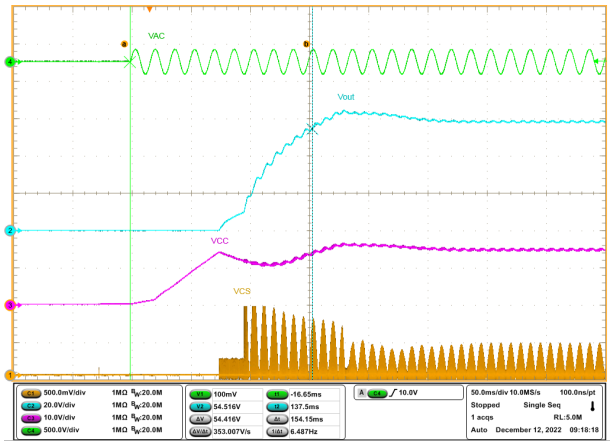


Figure 30. Startup at 115 V_{AC}, 25% load

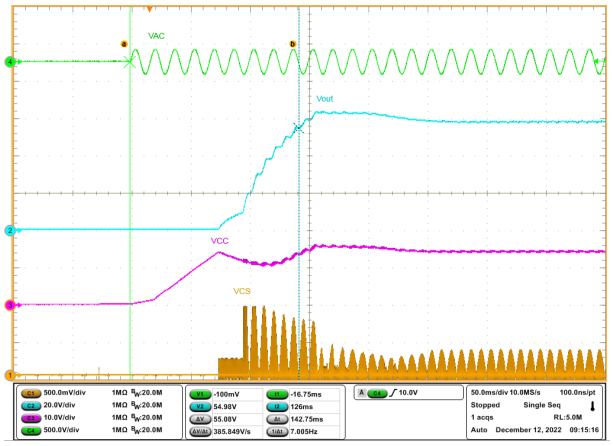


Figure 31. Startup at 115 V_{AC}, 270 mW load

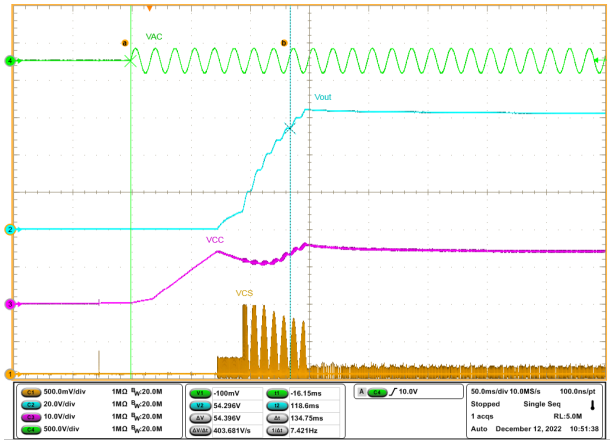
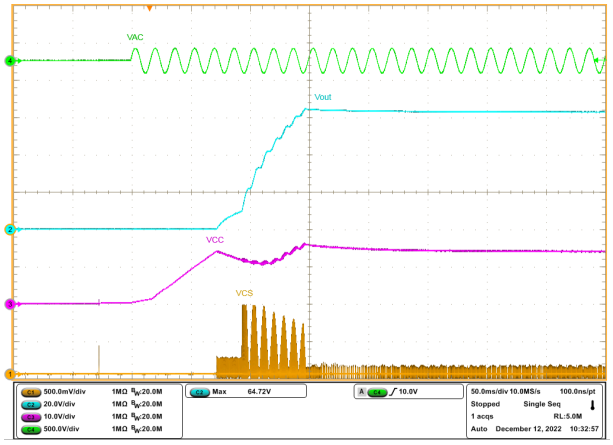


Figure 32. Startup at 115 V_{AC}, no load



6.3 Startup at 230 V_{AC} with different load conditions

Figure 33. Startup at 230 V_{AC}, 100% load

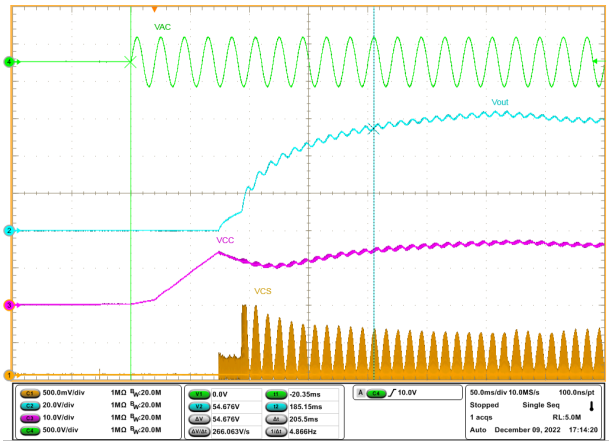


Figure 34. Startup at 230 V_{AC}, 75% load

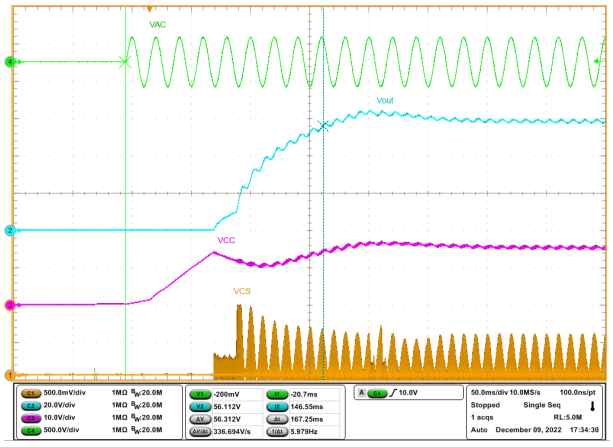


Figure 35. Startup at 230 V_{AC}, 50% load

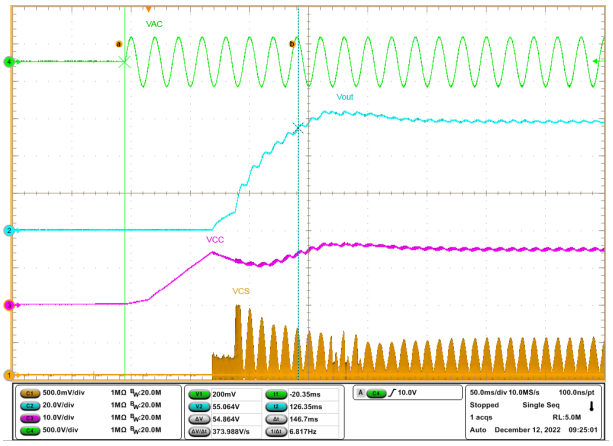


Figure 36. Startup at 230 V_{AC}, 25% load

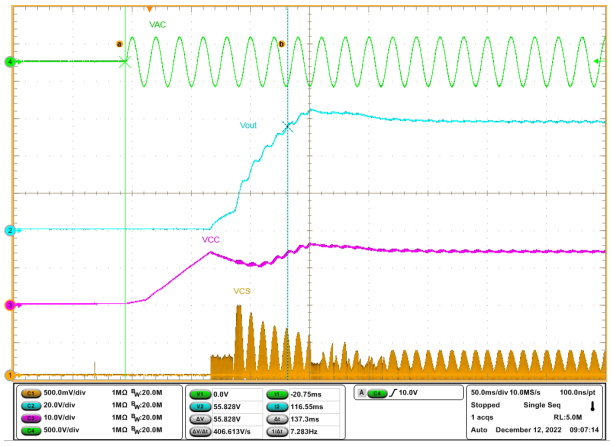


Figure 37. Startup at 230 V_{AC}, 270 mW load

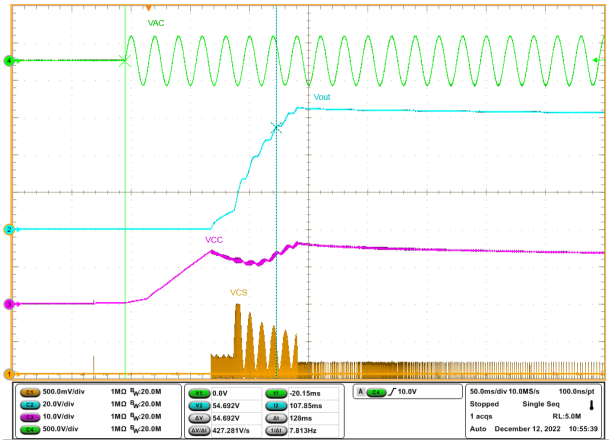
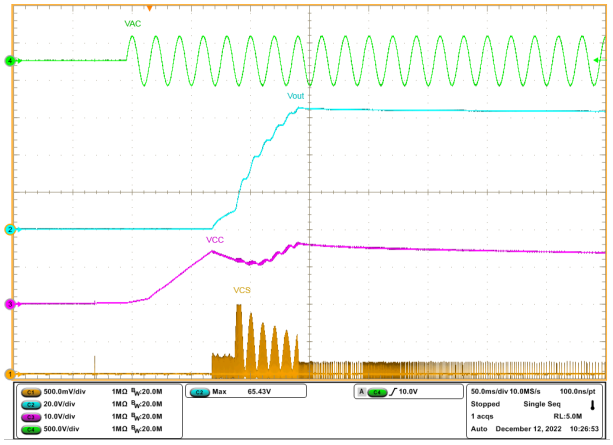


Figure 38. Startup at 230 V_{AC}, no-load



6.4 Startup at 265 V_{AC} with different load conditions

Figure 39. Startup at 265 V_{AC}, 100% load

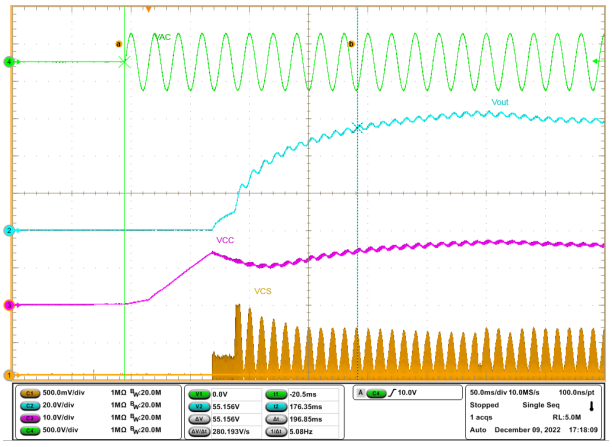


Figure 40. Startup at 265 V_{AC}, 75% load

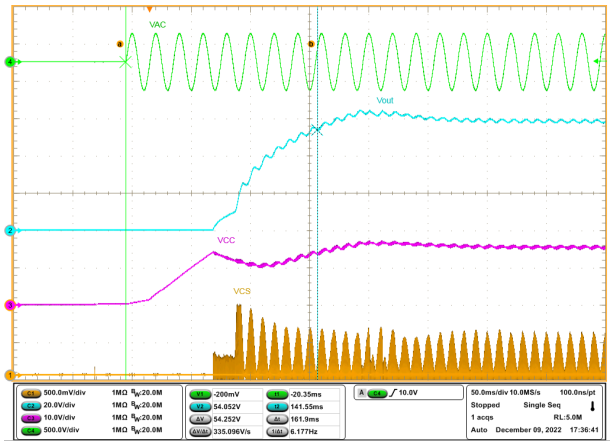


Figure 41. Startup at 265 V_{AC}, 50% load

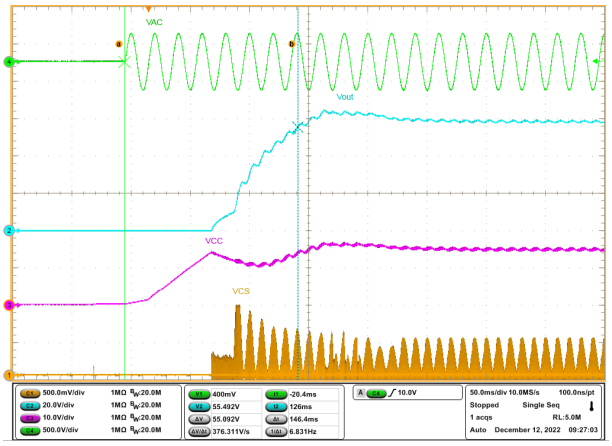


Figure 42. Startup at 265 V_{AC}, 25% load

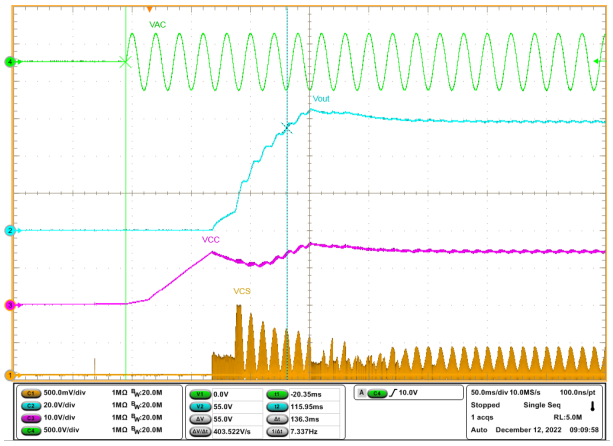


Figure 43. Startup at 265 V_{AC}, 270 mW load

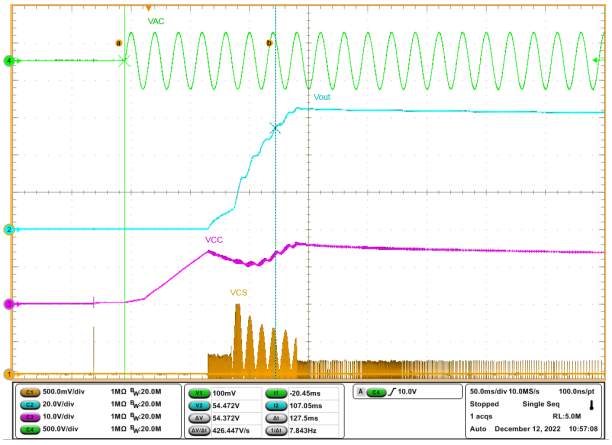
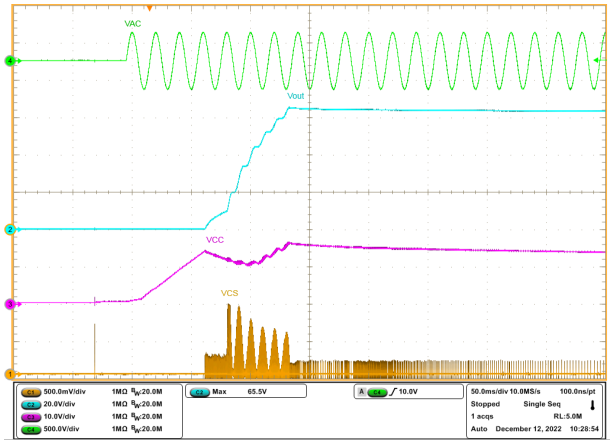


Figure 44. Startup at 265 V_{AC}, no-load



7 Operation modes

The following figures show the operation mode of the HVLED101 under different conditions. The test has been performed with 115 V_{AC}/60 Hz and 230 V_{AC}/50 Hz input voltage.

To change the mode of operation the maximum load has been slowly decreased until the minimum load value (0 A), and vice versa.

Starting from maximum load, with 115 V_{AC}, it is possible to observe the QR mode; decreasing the load, the system enters in valley skipping mode and finally at very low load the device is in burst mode and the reverse when the load is increased.

At 230 V_{AC} the system is already in valley skipping mode (1 valley skipped) also at full load.

The number of valleys skipped is in accordance with the voltage on the VL pin.

7.1 Valley skipping mode at 115 V_{AC}

In the following figures:

CH1 – yellow = CS current sense pin

CH2 – blue = GD gate driver pin

CH3 – red = Q1 drain voltage

CH4 – green = VL pin

Figure 45. Steady-state at 115 V_{AC}, 100% load

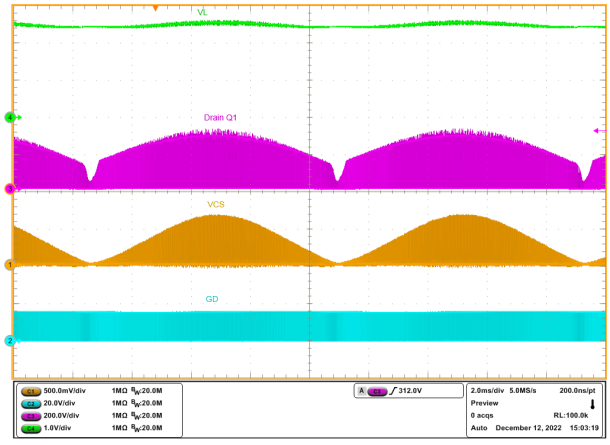


Figure 46. Steady-state at 115 V_{AC}, 100% load, AC peak – QR mode

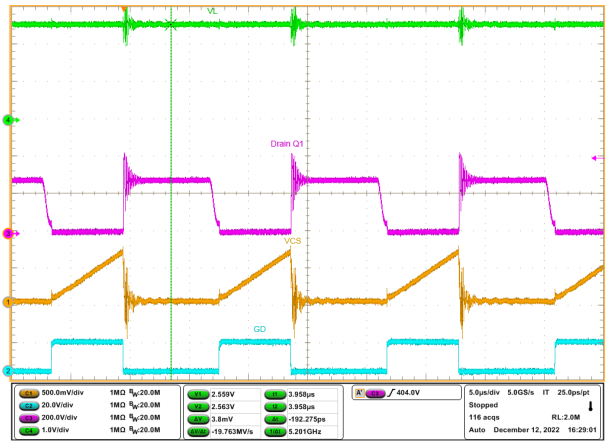


Figure 47. Steady-state at 115 V_{AC}, 50% load

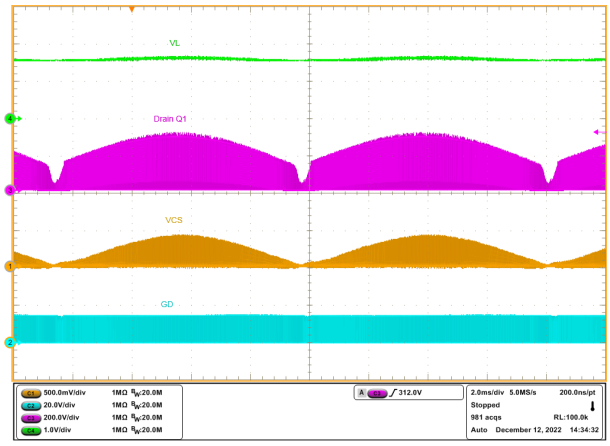


Figure 48. Steady-state at 115 V_{AC}, 50% load, AC peak – QR mode

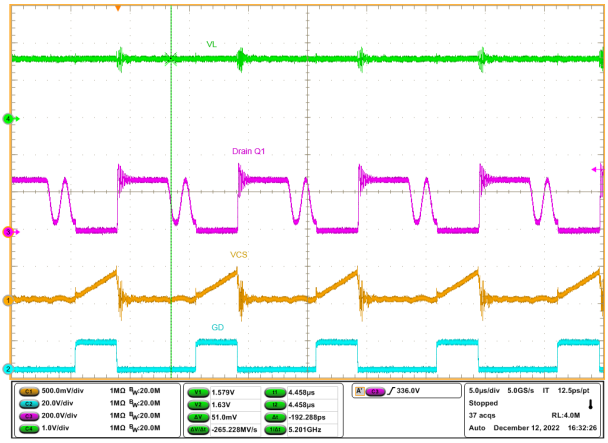


Figure 49. Steady-state at 115 V_{AC}, 25% load

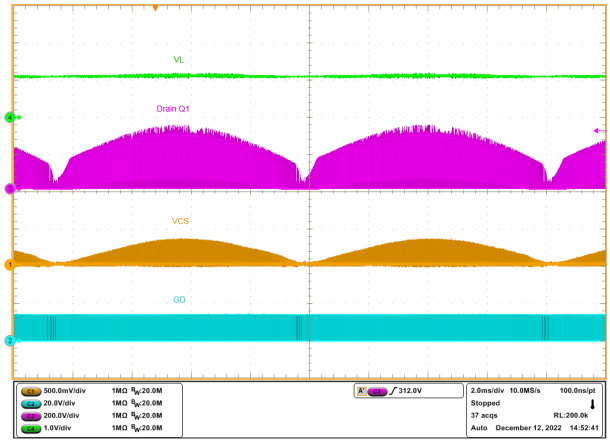


Figure 50. Steady-state at 115 V_{AC}, 25% load, AC peak – 4 valley skipped

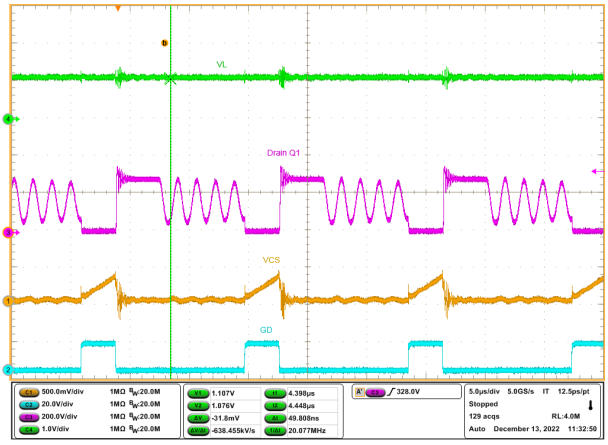


Figure 51. Steady-state at 115 V_{AC}, light load (50 mA)

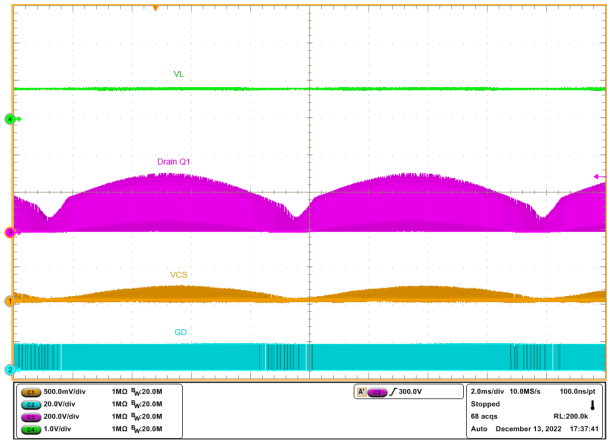


Figure 52. Steady-state at 115 V_{AC}, light load (50 mA), AC peak - DCM

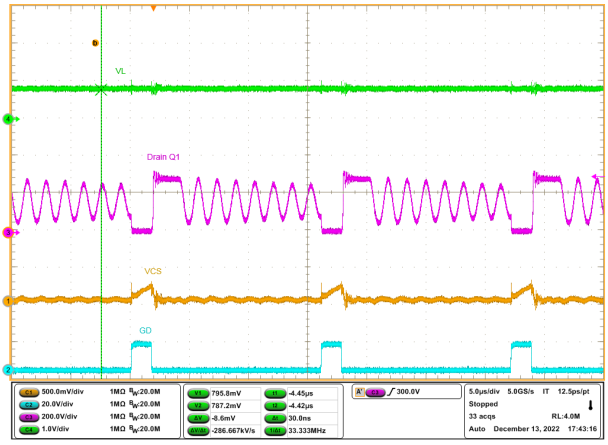


Figure 53. Burst mode at 115 V_{AC}, with no-load

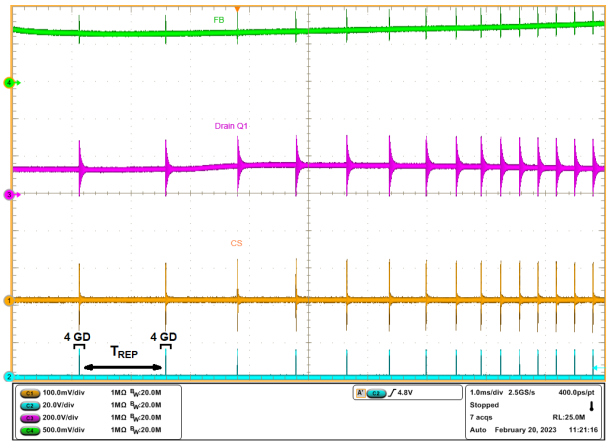
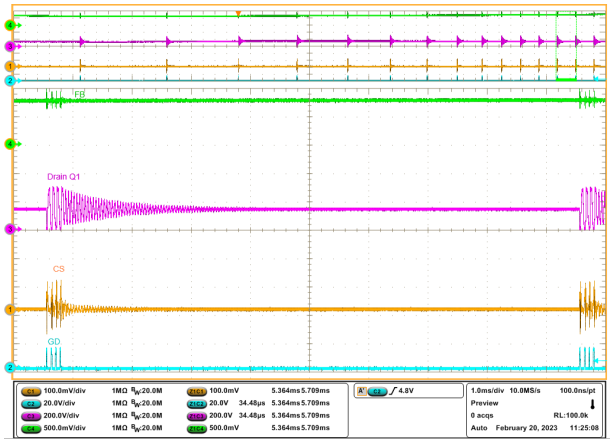


Figure 54. Burst mode at 115 V_{AC}, with no-load – zoom on 2 packets of 4 consecutive switching cycles



7.2 Valley skipping mode at 230 V_{AC}

Figure 55. Steady-state at 230 V_{AC}, 100% load

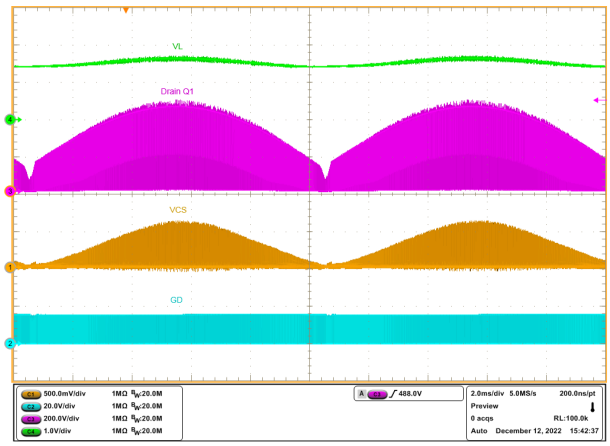


Figure 56. Steady-state at 230 V_{AC}, 100% load, AC peak – 1 valley skipped

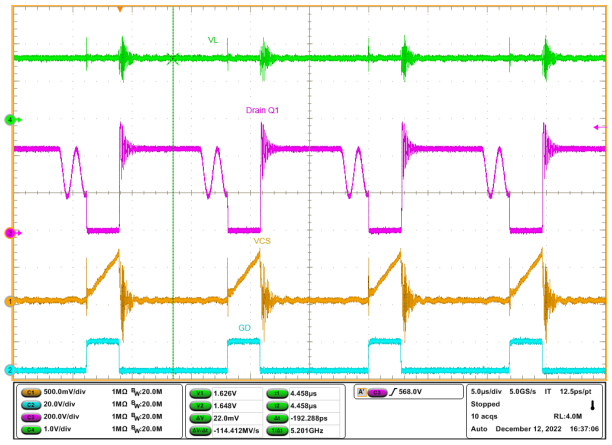


Figure 57. Steady-state at 230 V_{AC}, 50% load

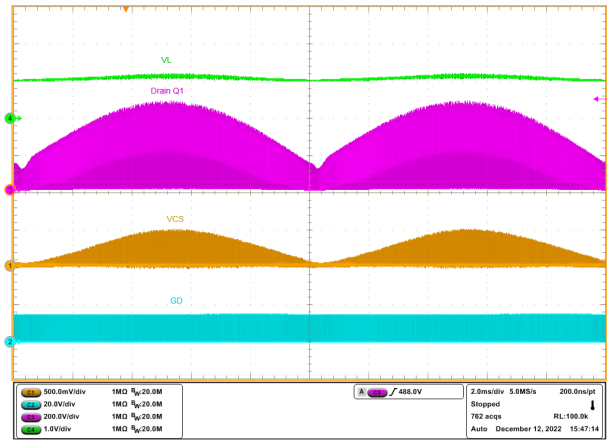


Figure 58. Steady-state at 230 V_{AC}, 50% load, AC peak – 4 valleys skipped

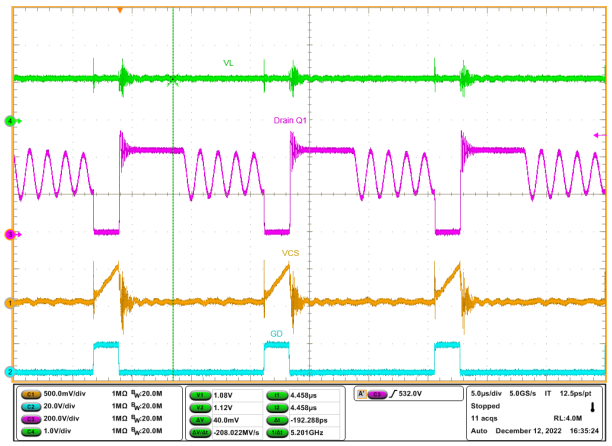


Figure 59. Steady-state at 230 V_{AC}, 25% load

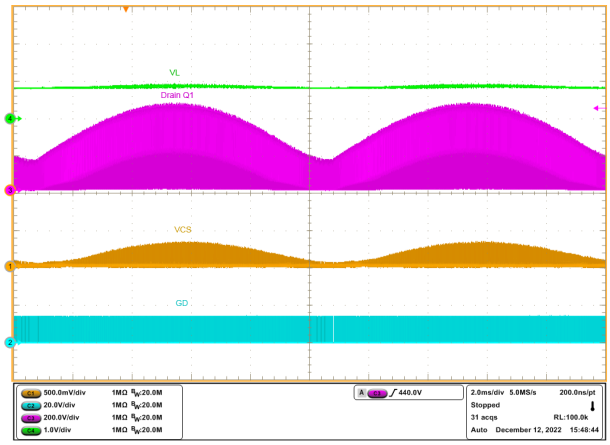


Figure 60. Steady-state at 115 V_{AC}, 25% load, AC peak – 5 valley skipped

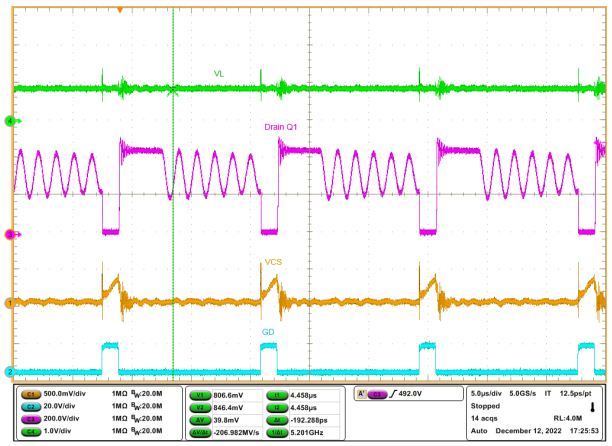


Figure 61. Steady-state at 230 V_{AC}, light load (150 mA)

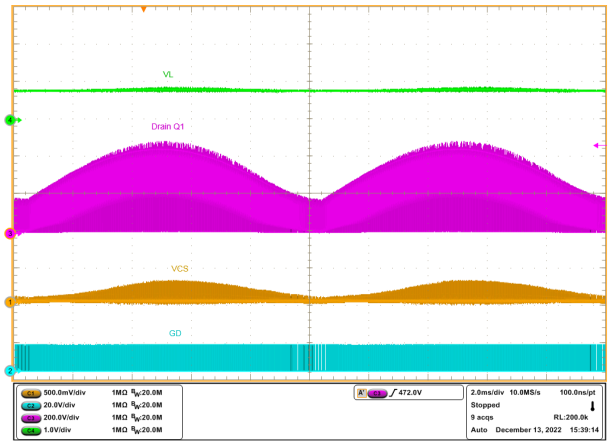


Figure 62. Steady-state at 230 V_{AC}, light load (150 mA), AC peak - DCM

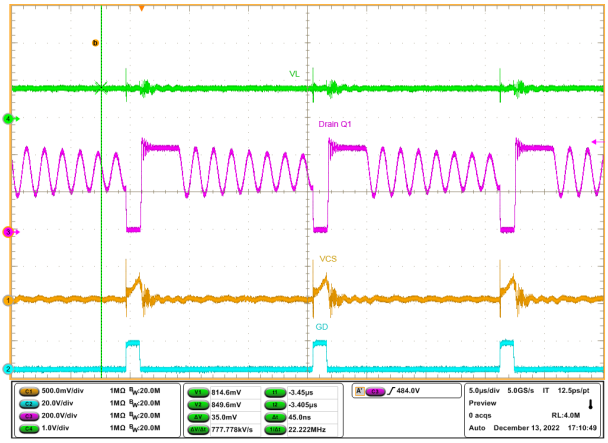


Figure 63. Burst mode at 230 V_{AC}, with no-load

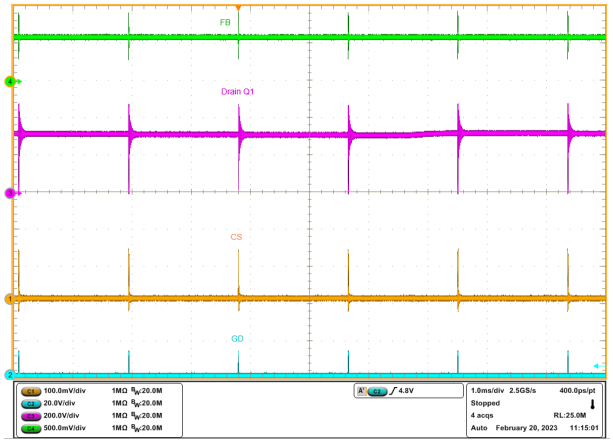
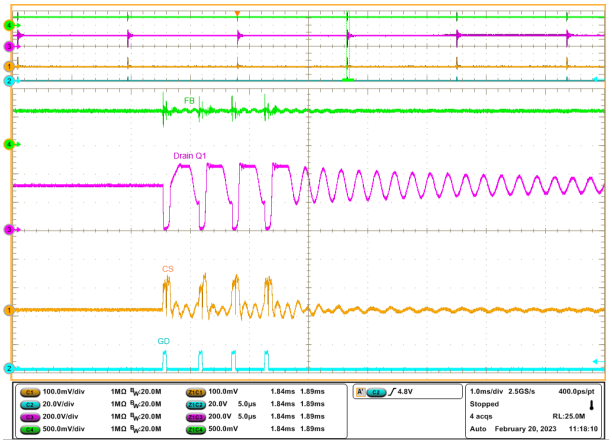


Figure 64. Burst mode at 230 V_{AC}, with no-load – zoom on 4 consecutive switching cycles



8 Load transients 100%-10%-100%

The following figures show the load transient response waveforms of the EVLHV101PSR50W when subjected to repetitive dynamic load transitions from 100% to 10% of the load at 115 V_{AC}/60 Hz and 230 V_{AC}/50 Hz.

The transition period is 1 s with a 50% duty cycle and a slew rate of 2.5 A/µs.

There are no abnormal oscillations in the output voltage and the overshoot and undershoot are 5 V max.

In the following figures:

- CH3 – red = I_{OUT}
- CH4 – green = V_{OUT}

Figure 65. Load transient 115 V_{AC}, 100% - 10% - 100%

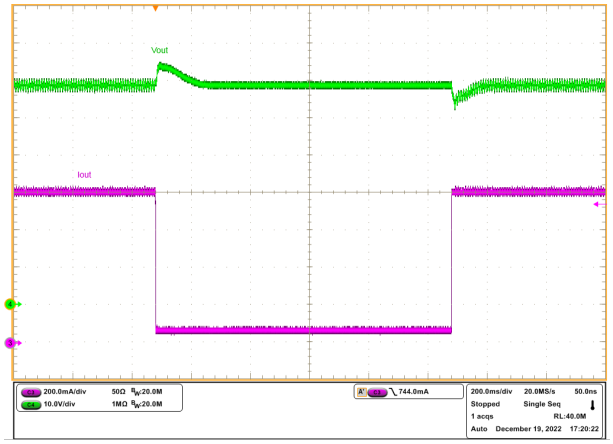
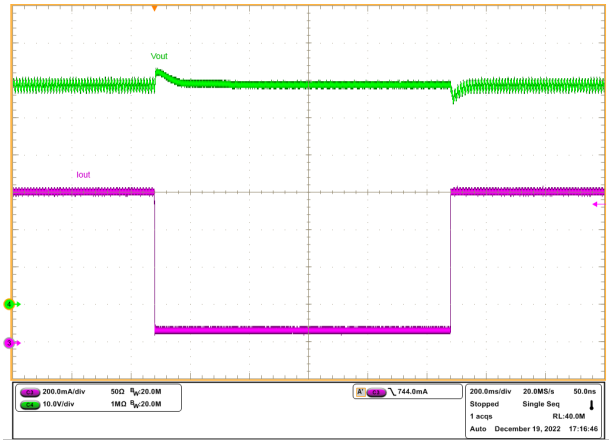


Figure 66. Load transients 230 V_{AC}, 100% - 10% - 100%



9 Load transients 75% - 25% - 75%

The following figures show the load transient response waveforms of the EVLHV101PSR50W when subjected to repetitive dynamic load transitions from 75% to 25% of the load at 115 V_{AC}/60 Hz and 230 V_{AC}/50 Hz. The transition period is 1 s with a 50% duty cycle and a slew rate of 2.5 A/µs.

There are no abnormal oscillations in the output voltage and the overshoot and undershoot are 3 V max.

In the following figures:

- CH3 – red = I_{OUT}
- CH4 – green = V_{OUT}

Figure 67. Load transient 115 V_{AC}, 75% - 25% - 75%

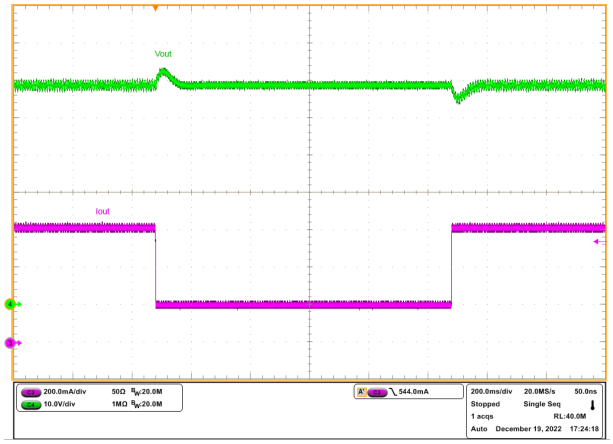
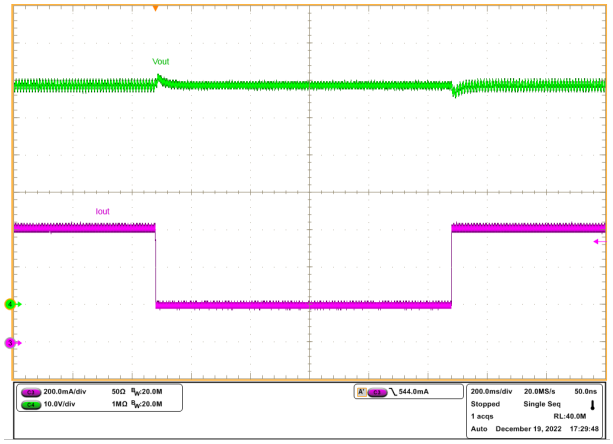


Figure 68. Load transients 230 V_{AC}, 75% - 25% - 75%



10 Thermal measurements

A thermal analysis of the board has been performed using an infrared thermal imaging camera. The test was performed at full load condition. The board has been submitted to 115 V_{AC} and 230 V_{AC} as inputs. The following figures show the thermal results 40 minutes after switching on the board.

The ambient temperature during the measurements was at 25 °C.

Figure 69. Thermal map at 115 V_{AC}

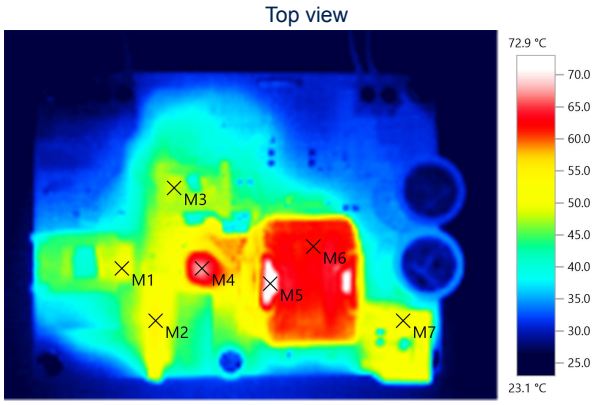


Figure 70. Thermal map at 115 V_{AC}

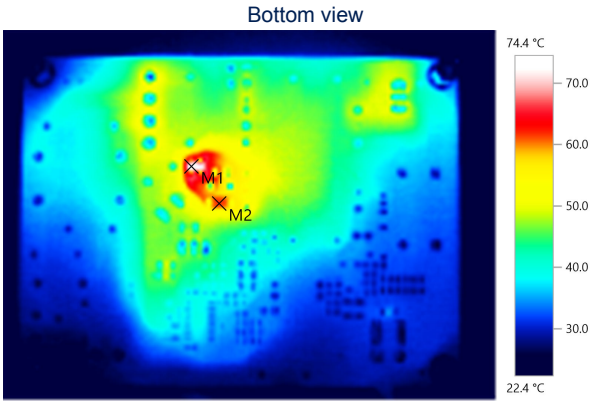


Table 12. Thermal map at 115 V_{AC}

Point	Reference	Description	Temperature
Top view			
M1	L5	Common-mode choke filter	50.1 °C
M2	D1	Bridge rectifier	54.5 °C
M3	Q1	MOSFET	48.6 °C
M4	R3 - R4	Top PCB area over R3 - R4 resistors	67.0 °C
M5	T1	Transformer winding	72.9 °C
M6	T1	Transformer ferrite	61.8 °C
M7	D4	Diode	50.5 °C
Bottom view			
M1	R3 - R4	Resistors	74.4 °C
M2	D2	Diode	61.4 °C

Figure 71. **Thermal map at 230 V_{AC}**

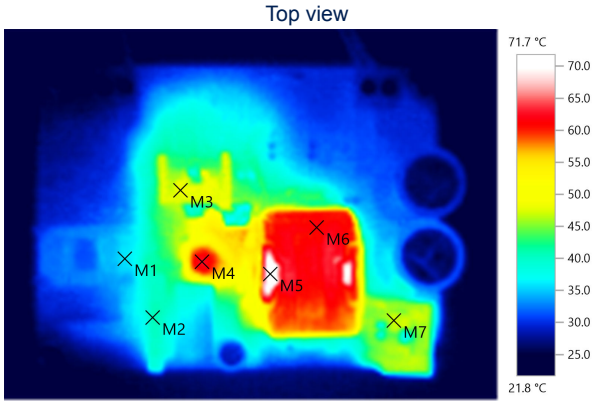


Figure 72. **Thermal map at 230 V_{AC}**

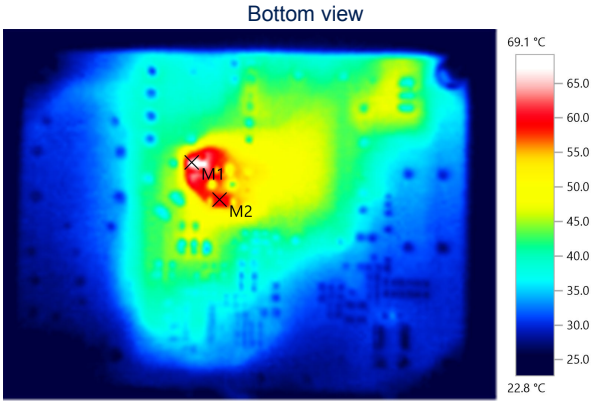


Table 13. **Thermal map at 230 V_{AC}**

Point	Reference	Description	Temperature
Top view			
M1	L5	Common-mode choke filter	36.0 °C
M2	D1	Bridge rectifier	40.3 °C
M3	Q1	MOSFET	48.2 °C
M4	R3 - R4	Top PCB area over R3 - R4 resistors	62.4 °C
M5	T1	Transformer winding	71.7 °C
M6	T1	Transformer ferrite	61.6 °C
M7	D4	Diode	48.9 °C
Bottom view			
M1	R3 - R4	Resistors	69.1 °C
M2	D2	Diode	59.8 °C

11 EMI measurements

The following figures show the measurements of the conducted emission with average mode detection at 115 V_{AC} and 230 V_{AC} as inputs.

Figure 73. EMI tests at 115 V_{AC} (output: 60V - 833mA)

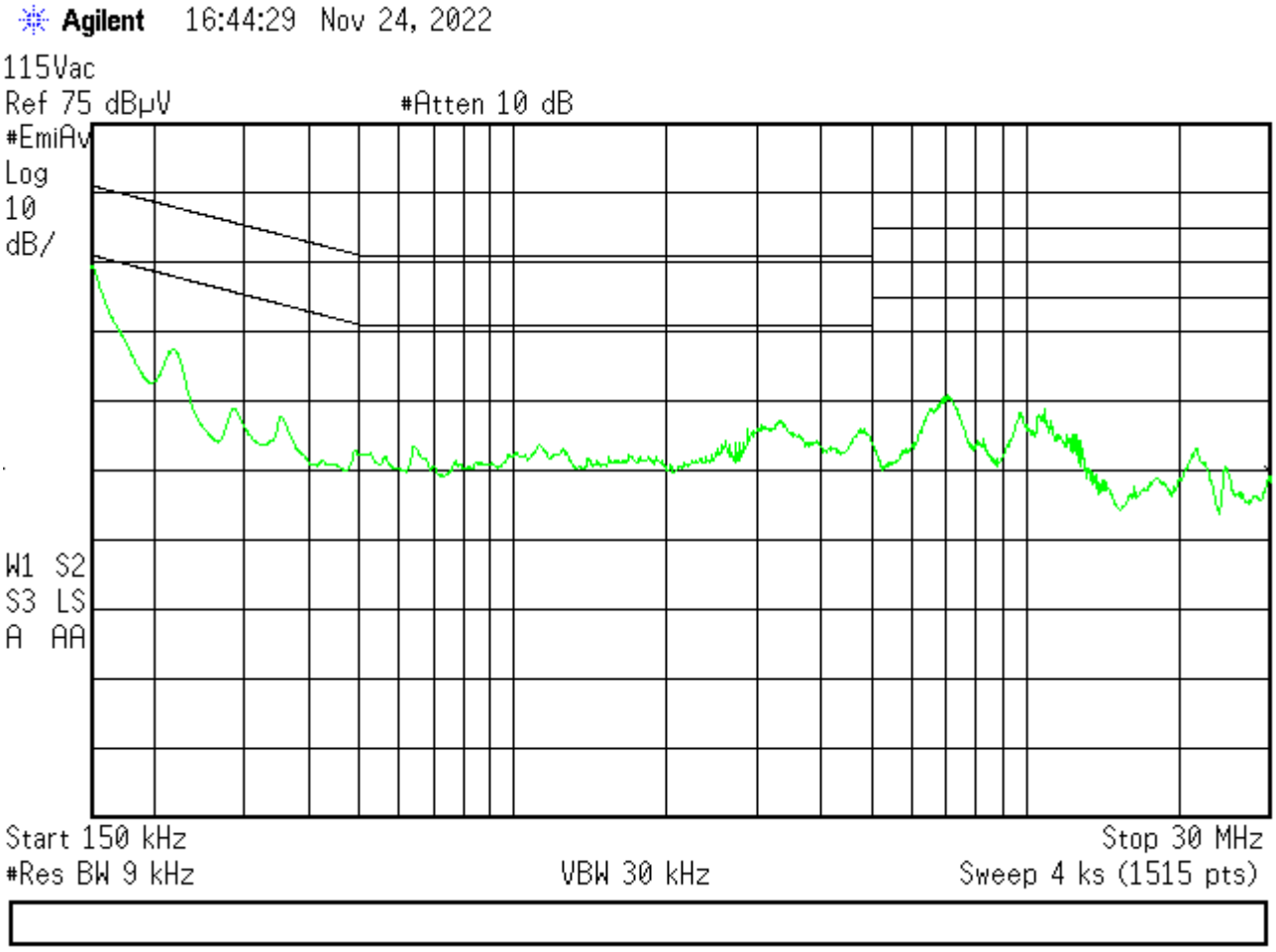
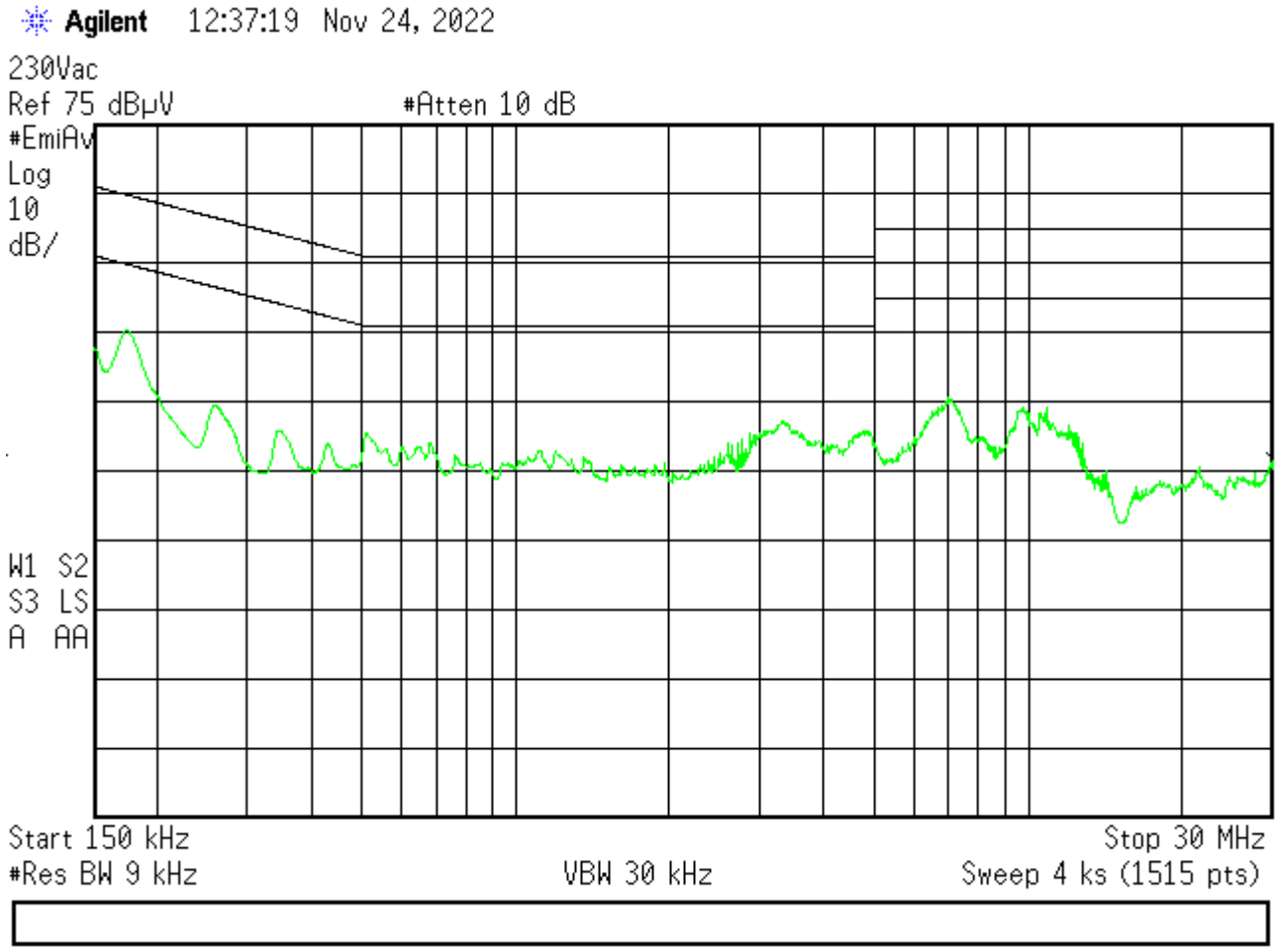


Figure 74. **EMI tests at 230 V_{AC} (output: 60V - 833mA)**



12 References

1. HVLED101 datasheet, see www.st.com.
2. AN4932, HVLED001A – enhanced QR high power factor flyback controller for LED drivers, see www.st.com.
3. AN5316, 35 W wide input range flyback converter using HVLED001B quasi-resonant flyback controller and STF10LN80K5, see www.st.com.
4. AN1059, design equations of high-power-factor flyback converters based on the L6561, see www.st.com.

Revision history

Table 14. **Document revision history**

Date	Version	Changes
19-Sep-2023	1	Initial release.

Contents

List of tables

List of figures