AN5969

Application note

Migrating between STM32G0 and STM32C0 MCUs

Introduction

This application note provides guidelines and methodology to migrate easily from an application between STM32G0 series and STM32C0 series. It groups all the most important information and lists the main aspects that must be addressed. It describes a simple procedure using the HAL (hardware abstraction layer), and STM32Cube software, to access a larger portfolio.

The STM32C0 series is a starting point for simple cost-focused applications.

The STM32G0 series is a starting point for simple applications requiring upgraded features in analog or low power.

Both series share the same technology and peripheral platform while having a consistent pinout between them. This is to ensure an easy migration between the two series.

It offers easy further migration within a wide range of STM32 products, depending on the application needs (focused on costs, tailored to low-power consumption).

This document provides details about the hardware, peripheral, and firmware migration.

For a better understanding, the user must be familiar with STM32 microcontrollers.

To benefit fully from this application note, the user must be familiar with the STM32 microcontroller documentation available on www.st.com, with a particular focus on the documents listed in Reference documents.

1 General information

The STM32C0 series and STM32G0 series MCUs are 32-bit microcontrollers based on the Arm® Cortex® processor.

Note: *Arm and Cortex are registered trademarks of Arm Limited (or its subsidiaries) in the US and/or elsewhere.*

Reference documents

[1] Datasheet *STM32G030x6/x8* (DS12991)

[2] Datasheet *STM32G050x6/x8* (DS13514)

[3] Datasheet *STM32G070CB/KB/RB* (DS12766)

[4] Datasheet *STM32G0B0KE/CE/RE/VE* (DS13565)

[5] Datasheet *STM32G031x4/x6/x8* (DS12992)

[6] Datasheet *STM32G051x6/x8* (DS13303)

[7] Datasheet *STM32G071x8/xB* (DS12232)

[8] Datasheet *STM32G0B1xB/xC/xE* (DS13560)

[9] Datasheet *STM32G041x6/x8* (DS12993)

[10] Datasheet *STM32G061x6/x8* (DS13513)

[11] Datasheet *STM32G081xB* (DS12231)

[12] Datasheet *STM32G0C1xC/xE* (DS13564)

[13] Datasheet *STM32C011x4/x6* (DS13866)

[14] Datasheet *STM32C031x4/x6* (DS13867)

[15] Datasheet *STM32C051x6/x8* (DS14721)

[16] Datasheet *STM32C071x8/xB* (DS14693)

[17] Datasheet *STM32C09xxB/xC* (DS14720)

[18] Reference Manual *STM32G0x1 advanced Arm®-based 32-bit MCUs* (RM0444)

[19] Reference Manual *STM32G0x0 advanced Arm®-based 32-bit MCUs* (RM0454)

[20] Reference Manual *STM32C0 series advanced Arm®-based 32-bit MCUs* (RM0490)

2 STM32C0 series and STM32G0 series overview

The STM32C0 series are the most affordable STM32 microcontrollers, making 32-bit capabilities accessible to all developers.

The STM32C0 series devices share the same technology platform, core, peripheral set as the STM32G0 series, and they offer a compatible pinout. While the STM32G0 series provides advanced features and capabilities (such as advanced analog functions and very low-power capabilities), the STM32C0 series focuses on essential functions for further cost optimization. As a result, some features like PLL, RTC domain, DAC, and comparators are not present in the STM32C0 series.

The STM32G0 series is available in two variants: Access line and Value line. The Access line is the most advanced with the full set of peripherals, option bytes or temperature range, and a variety of package options. The Value line, on the other hand, focuses on essential features, is available in a single temperature range, and comes in a more limited set of packages to enhance cost efficiency.

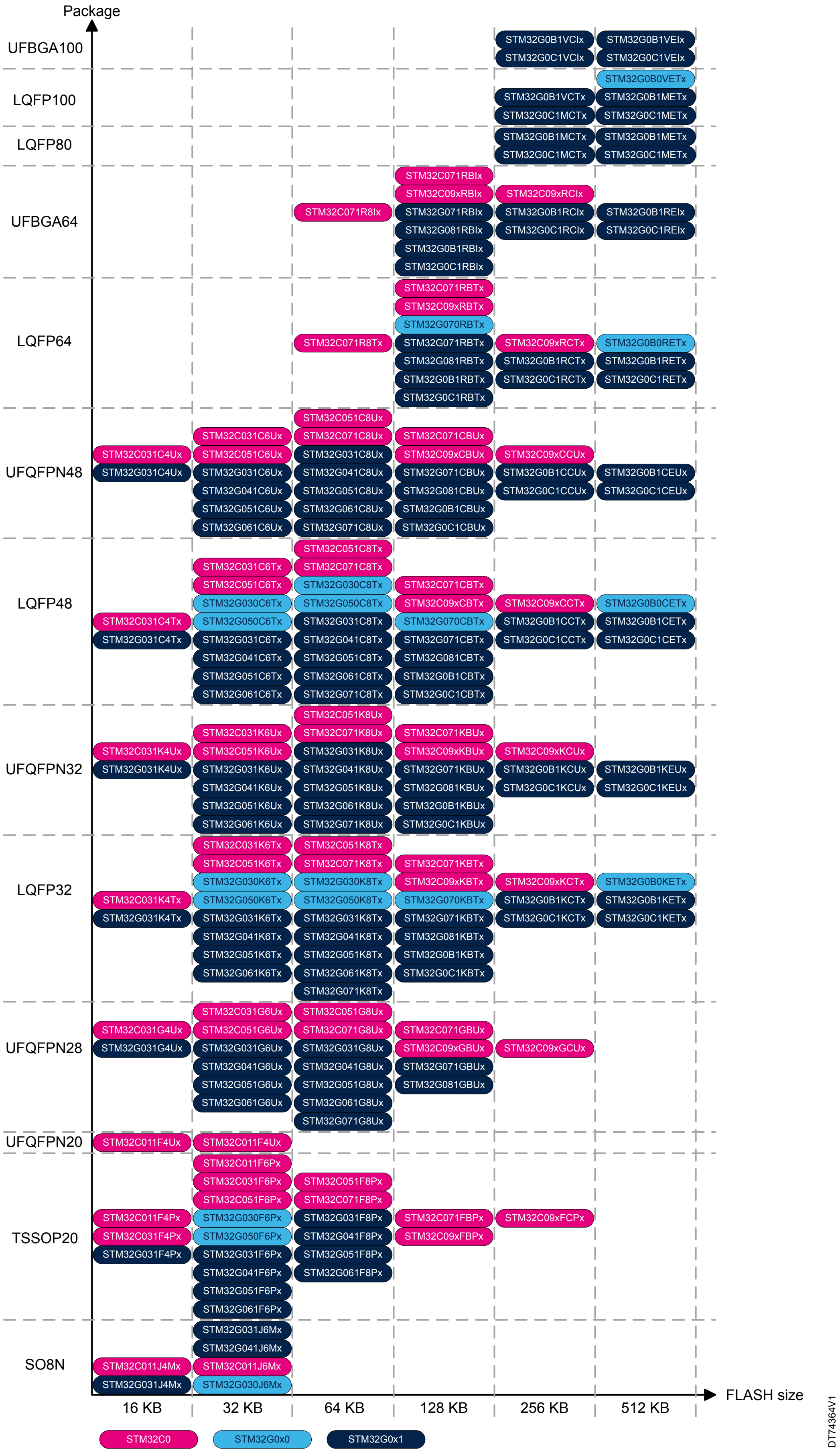
3 Migrating between STM32C0 series and STM32G0 series

All the STM32C0 series and STM32G0 series are pin-to-pin compatible and using the same platform. This compatibility is designed to simplify migration between the two series, helping users select and use the right product according to their needs. For example, it is possible to start developing an application by the biggest product with the highest number of peripherals (STM32G0 series access line) and then move to the right products to optimize the cost.

The inverse is also true: development can initially start on the STM32C0 series if the current project does not require upgraded features. For a new project using the same PCB but needing more peripherals, it is easy to transition to the STM32G0 series instead.

On smaller packages (< 32 pins), the STM32C0 series can support a bigger flash density compared to the STM32G0 series.

Figure 1. Comparison between STM32C0 series and STM32G0x0/G0x1 devices



Package	16 KB	32 KB	64 KB	128 KB	256 KB	512 KB
UFBGA100					STM32G0B1VCIx STM32G0C1VCIx	STM32G0B1VEIx STM32G0C1VEIx
LQFP100					STM32G0B1VCTx STM32G0C1MCTx	STM32G0B0VETx STM32G0B1METx STM32G0C1METx
LQFP80					STM32G0B1MCTx STM32G0C1MCTx	STM32G0B1METx STM32G0C1METx
UFBGA64			STM32C071R8Ix	STM32C071RBIx STM32C09xRBIx STM32G071RBIx STM32G081RBIx STM32G0B1RBIx STM32G0C1RBIx	STM32C09xRCIx STM32G0B1RCIx STM32G0C1RCIx	STM32G0B1REIx STM32G0C1REIx
LQFP64			STM32C071R8Tx	STM32C071RBTx STM32C09xRBTx STM32G070RBTx STM32G071RBTx STM32G081RBTx STM32G0B1RBTx STM32G0C1RBTx	STM32C09xRCTx STM32G0B1RCTx STM32G0C1RCTx	STM32G0B0RETx STM32G0B1RETx STM32G0C1RETx
UFQFPN48	STM32C031C4Ux STM32G031C4Ux	STM32C031C6Ux STM32C051C6Ux STM32G031C6Ux STM32G041C6Ux STM32G051C6Ux STM32G061C6Ux	STM32C051C8Ux STM32C071C8Ux STM32G031C8Ux STM32G041C8Ux STM32G051C8Ux STM32G061C8Ux STM32G071C8Ux	STM32C071CBUx STM32C09xCBUx STM32G071CBUx STM32G081CBUx STM32G0B1CBUx STM32G0C1CBUx	STM32C09xCCUx STM32G0B1CCUx STM32G0C1CCUx	STM32G0B1CEUx STM32G0C1CEUx
LQFP48	STM32C031C4Tx STM32G031C4Tx	STM32C031C6Tx STM32C051C6Tx STM32G030C6Tx STM32G050C6Tx STM32G031C6Tx STM32G041C6Tx STM32G051C6Tx STM32G061C6Tx	STM32C051C8Tx STM32C071C8Tx STM32G030C8Tx STM32G050C8Tx STM32G031C8Tx STM32G041C8Tx STM32G051C8Tx STM32G061C8Tx STM32G071C8Tx	STM32C071CBTx STM32C09xCBTx STM32G070CBTx STM32G071CBTx STM32G081CBTx STM32G0B1CBTx STM32G0C1CBTx	STM32C09xCCTx STM32G0B1CCTx STM32G0C1CCTx	STM32G0B0CETx STM32G0B1CETx STM32G0C1CETx
UFQFPN32	STM32C031K4Ux STM32G031K4Ux	STM32C031K6Ux STM32C051K6Ux STM32G031K6Ux STM32G041K6Ux STM32G051K6Ux STM32G061K6Ux	STM32C051K8Ux STM32C071K8Ux STM32G031K8Ux STM32G041K8Ux STM32G051K8Ux STM32G061K8Ux STM32G071K8Ux	STM32C071KBUx STM32C09xKBUx STM32G071KBUx STM32G081KBUx STM32G0B1KBUx STM32G0C1KBUx	STM32C09xKCUx STM32G0B1KCUx STM32G0C1KCUx	STM32G0B1KEUx STM32G0C1KEUx
LQFP32	STM32C031K4Tx STM32G031K4Tx	STM32C031K6Tx STM32C051K6Tx STM32G030K6Tx STM32G050K6Tx STM32G031K6Tx STM32G041K6Tx STM32G051K6Tx STM32G061K6Tx	STM32C051K8Tx STM32C071K8Tx STM32G030K8Tx STM32G050K8Tx STM32G031K8Tx STM32G041K8Tx STM32G051K8Tx STM32G061K8Tx STM32G071K8Tx	STM32C071KBTx STM32C09xKBTx STM32G070KBTx STM32G071KBTx STM32G081KBTx STM32G0B1KBTx STM32G0C1KBTx	STM32C09xKCTx STM32G0B1KCTx STM32G0C1KCTx	STM32G0B0KETx STM32G0B1KETx STM32G0C1KETx
UFQFPN28	STM32C031G4Ux STM32G031G4Ux	STM32C031G6Ux STM32C051G6Ux STM32G031G6Ux STM32G041G6Ux STM32G051G6Ux STM32G061G6Ux	STM32C051G8Ux STM32C071G8Ux STM32G031G8Ux STM32G041G8Ux STM32G051G8Ux STM32G061G8Ux STM32G071G8Ux	STM32C071GBUx STM32C09xGBUx STM32G071GBUx STM32G081GBUx	STM32C09xGCUx	
UFQFPN20	STM32C011F4Ux	STM32C011F4Ux				
TSSOP20	STM32C011F4Px STM32C031F4Px STM32G031F4Px	STM32C011F6Px STM32C031F6Px STM32C051F6Px STM32G030F6Px STM32G050F6Px STM32G031F6Px STM32G041F6Px STM32G051F6Px STM32G061F6Px	STM32C051F8Px STM32C071F8Px STM32G031F8Px STM32G041F8Px STM32G051F8Px STM32G061F8Px	STM32C071FBPx STM32C09xFBPx	STM32C09xFCPx	
SO8N	STM32C011J4Mx STM32G031J4Mx	STM32G031J6Mx STM32G041J6Mx STM32C011J6Mx STM32G030J6Mx				

4 Hardware migration

4.1 Pinout compatibility

The STM32C0 series and STM32G0 series share the same pinout, and are pin-to-pin compatible. When both series offer the same peripherals, the digital alternate functions and additional functions are mostly preserved.

However, when creating the PCB, the user must consider that the STM32C0 series lacks an RTC domain, which is replaced by a PF3 GPIO (indicated by the pink rectangle). Another difference is that, on the STM32C0 series, the pin PC14 is renamed to PC14-OSCX_IN and PC15 to PC15-OSCX_OUT. On this series, it is now possible to remap the HSE crystal oscillator pins (PF0-OSC_IN and PF1-OSC_OUT) to these pins (indicated by the yellow rectangle).

Below, two examples are available showing the differences described above.

Table 1. LQFP64 package comparison

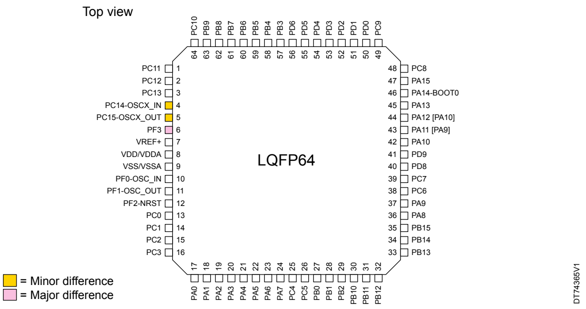
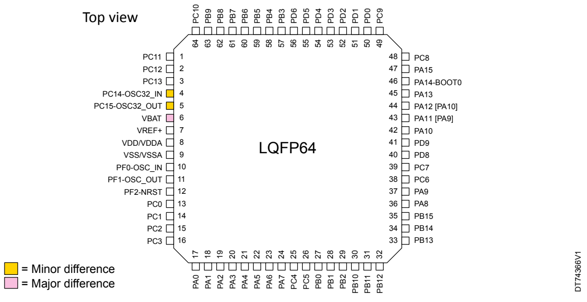
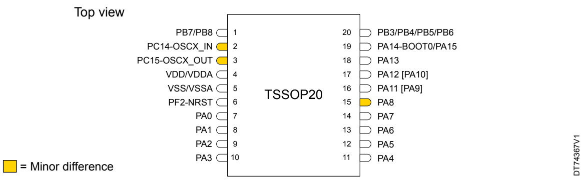
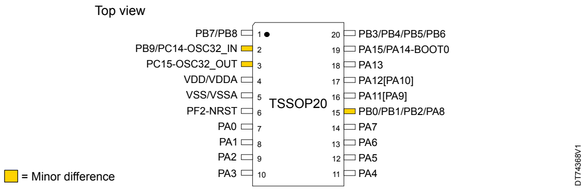
STM32C071RxT	STM32G071RxT
	

Table 2. TSSOP20 package comparison

STM32C051FxP	STM32G051FxP
	

Note: *On some TSSOP20 pinouts, STM32G0 series and STM32C0 series do not share the same multibonded pinout (see figures in Table 2 and). However, the alternate functions are preserved.*

4.2 Package availability

Some packages are available for both the STM32G0 series and STM32C0 series, as illustrated in Table 3. However, each product has its own WLCSP package. Since WLCSP is unique for each product, they are not included in Table 3.

Table 3. **Package availability on STM32C0 series and STM32G0 series**

Package	STM32C0 series					STM32G0 series			
	STM32C011	STM32C031	STM32C051	STM32C071	STM32C091 STM32C092	STM32G030 STM32G031 STM32G041	STM32G050 STM32G051 STM32G061[1]	STM32G070 STM32G071 STM32G081[1]	STM32G0B0 STM32G0B1 STM32G0C1[1]
SO8N (4.9 × 6 mm)	X	-	-	-	-	X	-	-	-
TSSOP20 (6.5 × 4.4 mm)	X	X	X	X	X	X	X	-	-
UFQFPN20 (3 × 3 mm)	X	-	-	-	-	-	-	-	-
UFQFPN28 (4 × 4 mm)	-	X	X	X	X	X	X	X	-
LQFP32 (7 × 7 mm)	-	X	X	X	X	X	X	X	X
UFQFPN32 (5 × 5 mm)	-	X	X	X	X	X	X	X	X
LQFP48 (7 × 7 mm)	-	X	X	X	X	X	X	X	X
UFQFPN48 (7 × 7 mm)	-	X	X	X	X	X	X	X	X
LQFP64 (10 × 10 mm)	-	-	-	X	X	-	-	X	X
UFBGA64 (5 × 5 mm)	-	-	-	X	X	-	-	X	X
LQFP80 (12 × 12 mm)	-	-	-	-	-	-	-	-	X
LQFP100 (14 × 14 mm)	-	-	-	-	-	-	-	-	X
UFGBA100 (7 × 7 mm)	-	-	-	-	-	-	-	-	X

1. *On STM32G0x0 devices (Value line), only SOxN and LQFP packages are available.*

Table 4. **WLCSP package list**

Product	WLCSP size
STM32C011	WLCSP12 (1.70 × 1.42 mm)
STM32C051	WLCSP15 (2.25 × 1.40 mm)
STM32G031 STM32G041	WLCSP18 (1.86 × 2.14 mm)
STM32C071	WLCSP19 (2.52 × 1.67 mm)
STM32G051 STM32G061	WLCSP20 (1.94 × 2.40 mm)
STM32C091 STM32C092	WLCSP24 (2.61 × 1.73 mm)
STM32G071 STM32G081	WLCSP25 (2.3 × 2.5 mm)
STM32G0B1 STM32G0C1	WLCSP52 (3.09 × 3.15 mm)

5 STM32 product cross-compatibility

STM32C0 series and STM32G0 series share the same peripheral platform with the same register basis. The parts below show only the differences between the two series.

Table 5. **Peripheral summary of STM32C0 series and STM32G0 series**

Feature		STM32C0 series				STM32G0 series							
		STM32C011 STM32C031	STM32C051	STM32C071	STM32C091 STM32C092	STM32G030	STM32G031 STM32G041	STM32G050	STM32G051 STM32G061	STM32G070	STM32G071 STM32G081	STM32G0B0	STM32G0B1 STM32G0C1
Flash memory		Up to 32 Kbytes	Up to 64 Kbytes	Up to 128 Kbytes	Up to 256 Kbytes	Up to 64 Kbytes	Up to 64 Kbytes	Up to 64 Kbytes	Up to 64 Kbytes	Up to 128 Kbytes	Up to 128 Kbytes	Up to 512 Kbytes	Up to 512 Kbytes
SRAM		6 Kbytes / 12 Kbytes	12 Kbytes	24 Kbytes	36 Kbytes / 30 Kbytes	8 Kbytes	8 Kbytes	18 Kbytes	18 Kbytes	36 Kbytes	36 Kbytes	144 Kbytes	144 Kbytes
V_{DD} minimum		2	2	2	2	2	1.7	2	1.7	2	1.7	2	1.7
V_{DD} maximum		3.6	3.6	3.6	3.6	3.6	3.6	3.6	3.6	3.6	3.6	3.6	3.6
Maximum speed		48 MHz	48 MHz	48 MHz	48 MHz	64 MHz	64 MHz	64 MHz	64 MHz	64 MHz	64 MHz	64 MHz	64 MHz
ADC channel		19 + 4	19 + 4	19 + 4	19 + 4	16 + 3	16 + 3	16 + 3	16 + 3	16 + 3	16 + 3	16 + 3	16 + 3
ADC resolution		12-bit	12-bit	12-bit	12-bit	12-bit	12-bit	12-bit	12-bit	12-bit	12-bit	12-bit	12-bit
DAC channel		0	0	0	0	0	0	0	2	0	2	0	2
COMP		0	0	0	0	0	0	0	2	0	2	0	3
VREFBUF		No	No	No	No	No	Yes	No	Yes	No	Yes	No	Yes
Timer	Advanced 16-bit	1	1	1	1	1	1	1	1	1	1	1	1
	General purpose 32-bit	0	1	1	1	0	1	0	1	0	1	0	1
	General purpose 16-bit	4	4	4	5	4	4	4	4	5	5	6	7
	Low-power	0	0	0	0	0	2	0	2	0	2	0	2
	Basic	0	0	0	0	0	0	2	2	2	2	2	2
	Watchdog	2	2	2	2	2	2	2	2	2	2	2	2

Feature		STM32C0 series				STM32G0 series							
		STM32C011 STM32C031	STM32C051	STM32C071	STM32C091 STM32C092	STM32G030	STM32G031 STM32G041	STM32G050	STM32G051 STM32G061	STM32G070	STM32G071 STM32G081	STM32G0B0	STM32G0B1 STM32G0C1
DMA channel		3	5	5	7	5	5	7	7	7	7	7 + 5	7 + 5
USART	Full	1	1	1	1	1	1	1	1	2	2	3	3
	Basic	1	1	1	3	2	1	2	1	4	2	6	3
LPUART		0	0	0	0	0	1	0	1	0	1	0	2
SPI		1	2	2	2	2	2	2	2	2	2	3	3
I^2C	Full	1	1	1	1	2	1	2	1	2	1	3	2
	Basic	0	1	1	1	0	1	0	1	0	1	0	1
HDMI-CEC		0	0	0	0	0	0	0	0	0	1	0	1
AES		No	No	No	No	No	No / Yes	No	No / Yes	No	No / Yes	No	No / Yes
RNG		No	No	No	No	No	No / Yes	No	No / Yes	No	No / Yes	No	No / Yes
UCPD		0	0	0	0	0	0	0	0	0	2	0	2
USB		0	0	1	0	0	0	0	0	0	0	0	1
FDCAN		0	0	0	0 / 1	0	0	0	0	0	0	0	2
RTC		1	1	1	1	1	1	1	1	1	1	1	1
Temperature minimum		-40 °C	-40 °C	-40 °C	-40 °C	-40 °C	-40 °C	-40 °C	-40 °C	-40 °C	-40 °C	-40 °C	-40 °C
Temperature maximum		Up to 125 °C	Up to 125 °C	Up to 125 °C	Up to 125 °C	85 °C	Up to 125 °C	85 °C	Up to 125 °C	85 °C	Up to 125 °C	85 °C	Up to 125 °C

5.1 RCC

Table 6. RCC differences between STM32C0 series and STM32G0 series

Feature	STM32C0 series	STM32G0 series
PLL	No	Yes
HSI clock frequency	48 MHz	16 MHz
LSI clock frequency	32 kHz	32 kHz
f_{HCLK}	Up to 48 MHz	Up to 64 MHz
f_{PCLK}	Up to 48 MHz	Up to 64 MHz
System clock source	• HSI48 • HSE • LSE • LSI • HSIUSB48	• HSI16 • HSE • PLL • LSE • LSI
System clock divider	Yes	No
HSE crystal pin can be remapped to PC14-PC15	Yes	No
LSE oscillator drive capability	• Medium-high driving capability • High driving capability	• Low driving capability • Medium-low driving capability • Medium-high driving capability • High driving capability

5.2 Power

Both the STM32C0 series and STM32G0 series share the same power supply scheme:

- V_{DD}: This is the external power supply for the internal regulator and the system analog such as reset, power management, and internal clocks. It consists of one pair V_{DD}/V_{SS}.
- V_{DDA}: This is the analog power supply for the A/D converter. It is shorted to V_{DD} to reduce the number of power supply pins.
- V_{DDIOx}: This is the power supply for the I/Os. It is typically shorted to V_{DD} to reduce the number of supply pins. However, on some products a second V_{DDIO2} power supply is available.
- V_{REF+}: This is the input reference voltage for the ADC. In lower pin-count packages, V_{REF+} is shorted to V_{DDA}.

Table 7. PWR differences between STM32C0 series and STM32G0 series

Feature	STM32C0 series	STM32G0x1 devices	STM32G0x0 devices
V_{DD} range	2.0 V to 3.6 V	1.7 V to 3.6 V	2.0 V to 3.6 V
V_{DDIO2} range	1.65 V to 3.6 V(1)	1.65 V to 3.6 V(1)	No
VREFBUF	No	Yes	No
VBAT pin and RTC domain	No	Yes	Yes
Dynamic voltage scaling	No	Yes (2 ranges)	Yes (2 ranges)
Low-power regulator	No	Yes	Yes
Low-power modes	• Run • Sleep • Stop • Standby • Shutdown	• Run • Low-power run • Sleep • Low-power sleep • Stop 0 • Stop 1 • Standby • Shutdown	• Run • Low-power run • Sleep • Low-power sleep • Stop 0 • Stop 1 • Standby • VBAT

Feature	STM32C0 series	STM32G0x1 devices	STM32G0x0 devices
		• VBAT	
Ultralow power enable (ENB_ULP)	No	Yes	No
Power supply supervisor	• POR/PDR • BOR	• POR/PDR • BOR • PVD	• POR/PDR

1. *Available only on some devices.*

On the STM32G0 series, the registers inside the RTC domain are write protected. To disable this protection, the bit DBP in the PWR_CR1 register must be set. This write protection mechanism is not present in the STM32C0 series.

The STM32C0 series has fewer low-power modes compared to the STM32G0 series due to different architecture (no low-power regulator and RTC domain). To help to calculate the new power budget and ease the comparison between the low-power modes, the user can refer to the power consumption calculator included in STM32CubeMX.

Table 8. **STM32C0 series low-power modes**

Mode	Regulator	CPU	Flash memory	SRAM	Clock	Peripheral	Consumption(1) (STM32C071)	Wake-up time
Run	On	On	On	On	Any	All available	88.5 µA / MHz at 48 MHz	N/A
Sleep	On	Off	On	On	Any	All available	1.0 mA at 48 MHz	10 CPU cycles
Stop	On	Off	On	Retained	HSIKER or LSE	RTC, IWDG, USART1 and I2C1	85.5 µA	2.7 µS
Standby	Off	Off	Off	Off (all content lost)	LSI	IWDG	7.35 µA	23 µS
Shutdown	Off	Off	Off	Off (all content lost)	Off	Off	23 µA	385 µS

1. *All consumption values are the typical value at T_a = 25 °C and V_{DD} = 3.0 V.*

Table 9. STM32G0 series low-power modes

Mode	Regulator	CPU	Flash memory	SRAM	Clock	Peripheral	Consumption[1] (STM32G071)	Wake-up time
Run	Main regulator	On	On	On	Any	All available	91 µA / MHz at 64 MHz	N/A
Low-power run	Low-power regulator	On	On	On	Any	All available	198 µA / MHz at 2 MHz	5 µS
Sleep	Main regulator	Off	On	On	Any	All available	1.8 mA at 64 MHz	11 CPU cycles
Low-power sleep	Low-power regulator	Off	On	On	Any	All available	60 µA at 2 MHz	11 CPU cycles
Stop 0	Main regulator	Off	On	Retained	HSI16, LSE, LSI	RTC/TAMP, USART, I^2C, LPTIM, COMP	100 µA	2 µS
Stop 1	Low-power regulator	Off	On	Retained	HSI16, LSE, LSI	RTC/TAMP, USART, I^2C, LPTIM, COMP	7.3 µA	5 µS
Standby	Off	Off	Off	Optional	LSI, LSE	IWDG, RTC/ TAMP	200 nA	30 µS
Shutdown[2]	Off	Off	Off	Off (all content lost)	LSE	RTC/TAMP	33 nA	340 µS

1. *All consumption values are the typical value at T_a = 25 °C and V_{DD} = 3.0 V.*
2. *Not available on STM32G0x0 devices.*

5.3 RTC / TAMP and backup register

Table 10. RTC differences between STM32C0 series and STM32G0 series

Feature	STM32C0 series	STM32G0 series
Wake-up timer	No	Yes
Number of alarms	1	2
Timestamp feature	No	Yes
Low-power mode	All except Standby and Shutdown	All except Shutdown
Calendar overflow	No	Yes
TAMP	No	3 externals + 4 internals
Backup register	4 × 16-bit	5 × 32-bit

5.4 Embedded bootloader

Table 11. Bootloader interfaces on the STM32C0 series and STM32G0 series

Peripheral	Pins	STM32C0 series					STM32G0 series			
		STM32C011	STM32C031	STM32C051	STM32C071	STM32C091 STM32C092	STM32G030 STM32G031 STM32G041	STM32G050 STM32G051 STM32G061	STM32G070 STM32G071 STM32G081	STM32G0B0 STM32G0B1 STM32G0C1
USB DFU	USB_DM (PA11) USB_DP (PA12)	-	-	-	-	X	-	-	-	X[1]
USART1	USART1_RX (PA10) USART1_TX (PA9)	X	X	X	X	X	X	X	X	X
USART2	USART2_RX (PA3) USART2_TX (PA2)	-	-	X	X	X	X	X	X	X
USART3	USART3_RX (PC11) USART3_TX (PC10)	-	-	-	-	-	-	-	X	X
I2C1	I2C1_SCL (PB6) I2C1_SDA (PB7)	X	X	X	X	X	X	X	X	X
I2C2	I2C1_SCL (PB10) I2C1_SDA (PB11)	-	-	X	X	X	X	X	X	X
SPI1	SPI1_MOSI (PA7) SPI1_MISO (PA6) SPI1_SCK (PA5) SPI1_NSS (PA4)	-	-	X	X	X	-	-	X	X
SPI2	SPI2_MOSI (PB15) SPI2_MISO (PB14) SPI2_SCK (PB13) SPI2_NSS (PB12)	-	-	X	X	X	-	-	X	X
FDCAN	FDCAN1_RX (PD0) FDCAN1_TX (PD1)	-	-	-	-	X	-	-	-	X[1]

1. Not available on STM32G0B0 devices.

5.5 NVIC

Table 12. Interrupt vector differences between STM32C0 series and STM32G0 series

Position	STM32C0 series	STM32G0 series	Address
0	WWDG	WWDG	0x0000 0040
1	PVM	PVD / PVM	0x0000 0044
2	RTC	RTC / TAMP	0x0000 0048
3	FLASH	FLASH	0x0000 004C
4	RCC / CRS	RCC / CRS	0x0000 0050
5	EXTI0_1	EXTI0_1	0x0000 0054
6	EXTI2_3	EXTI2_3	0x0000 0058

Position	STM32C0 series	STM32G0 series	Address
7	EXTI4_15	EXTI4_15	0x0000 005C
8	USB	UCPD1 / UCPD2 / USB	0x0000 0060
9	DMA1_CH1	DMA1_CH1	0x0000 0064
10	DMA1_CH2_3	DMA1_CH2_3	0x0000 0068
11	DMAMUX / DMA1_CH4 to 7	DMAMUX / DMA1_CH4 to 7 / DMA2_CH1 to 5	0x0000 006C
12	ADC1	ADC / COMP	0x0000 0070
13	TIM1_BRK_UP_TRG_COM	TIM1_BRK_UP_TRG_COM	0x0000 0074
14	TIM1_CC	TIM1_CC	0x0000 0078
15	TIM2	TIM2	0x0000 007C
16	TIM3	TIM3 / TIM4	0x0000 0080
17	-	TIM6 / DAC / LPTIM1	0x0000 0084
18	-	TIM7 / LPTIM2	0x0000 0088
19	TIM14	TIM14	0x0000 008C
20	TIM15	TIM15	0x0000 0090
21	TIM16	TIM16 / FDCAN_IT0	0x0000 0094
22	TIM17	TIM17 / FDCAN_IT1	0x0000 0098
23	I2C1	I2C1	0x0000 009C
24	I2C2	I2C2 / I2C3	0x0000 00A0
25	SPI1	SPI1	0x0000 00A4
26	SPI2	SPI2 / SPI3	0x0000 00A8
27	USART1	USART1	0x0000 00AC
28	USART2	USART2 / LPUART2	0x0000 00B0
29	USART3 / USART4	USART3 / USART4 / USART5 / USART6 / LPUART1	0x0000 00B4
30	FDCAN_IT0	CEC	0x0000 00B8
31	FDCAN_IT1	AES / RNG	0x0000 00BC

Note: *As both series embed the same Cortex®-M0+ CPU, they also share the same CPU interrupt structure.*

5.6 EXTI

STM32C0 series and STM32G0 series share the same EXTI (external interrupt) mapping. When the same peripheral instances are available on both series, their EXTI source and type use the same EXTI line. For example, on both the STM32G0 series and STM32G0 series devices, the EXTI source "USART1 wake-up" is present and configurable on the EXTI line 25.

5.7 Memory mapping

STM32C0 series and STM32G0 series share the same memory mapping and register addresses for common peripherals. The primary distinction between the two series lies in the location of the backup registers: in the STM32G0 series, they are found within the TAMP registers, whereas in the STM32C0 series, they are located within the PWR registers.

5.8 FLASH

Table 13. **FLASH differences between STM32C0 series and STM32G0 series**

Feature	STM32C0 series	STM32G0 series
ECC	No	Yes
Dual Bank	No	Yes[1]
Data width	64-bit	72-bit (64-bit data + 8-bit ECC)
Page size	2 Kbytes	
Subpage size	512 bytes	
Number of wait-states	2 levels: Zero wait-state One wait-state	3 levels: Zero wait-state One wait-state Two wait-states

1. Available only on 256-Kbyte and 512-Kbyte flash memory size devices.

Table 14. **Option byte differences between STM32C0 series and STM32G0 series**

Feature	STM32C0 series	STM32G0x1 devices	STM32G0x0 devices
RDP level	Level 0: No protection Level 1: Read protection Level 2: No debug		
WRP	Two areas	Two areas per bank	Two areas per bank
PCROP	Two areas	Two areas per bank	No
Securable memory area	Yes	Yes	No
Boot lock	Yes	Yes	No
IRHEN	Yes	Yes	No
NRST pin configuration	Yes	Yes	No
UID	Yes	Yes	No

The STM32C0 series embeds two new option bits.

The first one called **HSE_NOT_REMAPPED** to remap or not the HSE between PF0/PF1 and PC14/PC14. Both clocks HSE and LSE cannot be used simultaneously. On packages smaller than 48 pins, this remap is always on (there is no PF0, PF1 pins) and this bit is ignored.

The second one is **SECURE_MUXING_EN**. This bit enables automatic I/O configuration to prevent conflicts on I/Os connected (bonded) into the same pin. When set, the software activates one of the I/Os connected to the same pin as active by configuring the SYSCFG_CFGR3 register. Enabling this bit automatically forces the other I/Os into digital input mode or disables the output buffer, regardless of their software configuration. When this bit is disabled, the SYSCFG_CFGR3 register setting is ignored, all GPIOs linked to a given pin can be set to the mode specified by the corresponding GPIOx_MODER register. In this case, the user software must ensure that there is no conflict between GPIOs.

5.9 SRAM

Both series have SRAM with parity check. The data bus width is 36 bits because 4 bits are allocated for parity check (1 bit per byte). By default, the parity check is disabled. To enable it, the option bit RAM_PARITY_CHECK in the user option byte must be set.

On STM32G0 series, it is possible to use the bits reserved for parity to gain additional SRAM (except for STM32G031, STM32G041, and STM32G030 devices). Enabling the parity check decreases the SRAM size by 13.8 % (for more details, see the product datasheet). For example, on STM32G0B1 devices, the SRAM size is 128 Kbytes with parity and 144 Kbytes without parity.

Table 15. **SRAM density between STM32C0 series and STM32G0 series**

FLASH size	STM32C0 series SRAM size	STM32G0 series SRAM size (parity check disabled)
16 Kbytes	STM32C011x4: 6 Kbytes	STM32G031x4: 8 Kbytes
	STM32C031x4: 12 Kbytes	
32 Kbytes	STM32C011x6: 6 Kbytes	STM32G031x6 / STM32G041x6 / STM32G030x6: 8 Kbytes
	STM32C031x6: 12 Kbytes	STM32G051x6 / STM32G061x6 / STM32G050x6: 18 Kbytes
64 Kbytes	STM32C051x8: 12 Kbytes	STM32G031x8 / STM32G041x8 / STM32G030x8: 8 Kbytes
	STM32C071x8: 24 Kbytes	STM32G051x8 / STM32G061x8 / STM32G050x8: 18 Kbytes
		STM32G071x8 / STM32G081x8: 36 Kbytes
128 Kbytes	STM32C071xB: 24 Kbytes	STM32G071xB / STM32G081xB / STM32G070xB: 36 Kbytes
	STM32C091xB: 36 Kbytes	
	STM32C092xB: 30 Kbytes	STM32G0B1xB / STM32G0C1xB: 144 Kbytes
256 Kbytes	STM32C091xB: 36 Kbytes	STM32G0B1xC / STM32G0C1xC: 144 Kbytes
	STM32C092xB: 30 Kbytes	
512 Kbytes	-	STM32G0B1xE / STM32G0C1xE / STM32G0B0xE: 144 Kbytes

5.10 GPIO

Table 16. **GPIO differences between STM32C0 series and STM32G0 series**

Feature	STM32C0 series	STM32G0 series
Analog switch booster	No	Yes
Clamping diode	No	Yes
Pin mux protection when multiple pins are bounded together	Yes	No

5.11 SYSCFG

The STM32C0 series and STM32G0 series implement the same SYSCFG features, except for the feature specific to each product:

STM32C0 series:

- CFGR3 Register: This register allows selecting the active GPIO that maintains the settings specified by its corresponding GPIOx_MODER register.
- For STM32C011xx, STM32C031xx, and STM32C071xx, the other GPIOs connected to the same pin are forced into digital input (passive) mode, regardless of their corresponding GPIOx_MODER register settings.
- For STM32C051xx and STM32C091xx/92xx, the output buffer of the other GPIOs connected to the same pin is disabled, regardless of their corresponding GPIOx_MODER register settings. It can be bypassed by resetting the SECURE_MUXING_EN bit (see Section 5.8).

STM32G0 series:

- BOOSTEN bit in the CFGR1 register: This bit enables or disables the analog voltage booster.
- XXX_CDEN bits in the CFGR2 register: These bits enable or disable the clamping diode.

5.12 ADC

Both the STM32C0 series and STM32G0 series share the same 12-bit ADC with a sampling rate of up to 2.5 Msps. The main differences between the two series are:

- Clock Frequency Flexibility: The STM32G0 series offers higher clock frequency flexibility thanks to the PLL.
- ADC Channels: The STM32C0 series offers more ADC channels.

Table 17. **ADC channel list comparison**

PIN	STM32C0 series		STM32G0 series	
	STM32C011 STM32C031 STM32C051	STM32C071 STM32C091 STM32C092	STM32G030 STM32G031 STM32G041 STM32G050 STM32G051 STM32G061	STM32G070 STM32G071 STM32G081 STM32G0B0 STM32G0B1 STM32G0C1
PA0	IN0	IN0	IN0	IN0
PA1	IN1	IN1	IN1	IN1
PA2	IN2	IN2	IN2	IN2
PA3	IN3	IN3	IN3	IN3
PA4	IN4	IN4	IN4	IN4
PA5	IN5	IN5	IN5	IN5
PA6	IN6	IN6	IN6	IN6
PA7	IN7	IN7	IN7	IN7
PA8	IN8	IN8	-	-
VSENCE	IN9	IN9	IN12	IN12
VREFINT	IN10	IN10	IN13	IN13
VBAT/3	-	-	IN14	IN14
PA11	IN11	-	IN15[1]	-
PA12	IN12	-	IN16[1]	-
PA13	IN13	IN13	IN17	-
PA14	IN14	IN14	IN18	-
VDDA	IN15	IN15	-	-
VSSA	IN16	IN16	-	-
PB0	IN17	IN17	IN8	IN8
PB1	IN18	IN18	IN9	IN9
PB2	IN19	IN19	IN10	IN10
PB10	IN20	IN20	IN11	IN11
PB11	IN21	IN21	IN15	IN15
PB12	IN22	IN22	IN16	IN16
PC4	-	IN11	-	IN17
PC5	-	IN12	-	IN18
PB7	-	-	IN11[1]	-

[1] *Only on packages below 48-pin.*

5.12.1 Temperature sensor

Table 18. Temperature sensor comparison

Feature	STM32C0 series	STM32G0x1 devices	STM32G0x0 devices
Number of TS_CAL	1	2	1
VTS linearity	Typ: ±1 °C, Maximum: ±5 °C	Typ: ±1 °C, Maximum: ±2 °C	Typ: ±1 °C, Maximum: ±2 °C

5.13 USB

Both series have a compatible peripheral. However, the version on the STM32C0 series received some correction to remove the limitation (for more information, refer to the product errata sheet)

5.14 USART, FDCAN, CRC, CRS, IWDG, WWDG, and I2C

Both series share the same peripheral and they are fully compatible.

5.15 SPI

Both series share the same peripheral and they are fully compatible. However, due to differences in maximum clock frequency, the maximum speed for the STM32C0 series is up to 24 MHz (f_{PCLK} / 2), while for the STM32G0 series, it is up to 32 MHz (f_{PCLK} / 2).

5.16 DMA and DMAMUX

Both series share the same peripheral architecture. When the same peripherals are available on both products, their DMA assignment of multiplexer inputs to resources, trigger inputs to resources, and synchronization inputs to resources are identical.

5.17 Timer

The STM32C0 series and STM32G0 series share the same timer features and instance name. They are described in Table 19. See Table 20 to compare the timer instances between both series.

Table 19. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/ compare channels	Complementary outputs
Advanced control	TIM1	16-bit	Up, down, up/ down	Integer from 1 to 2 × 16	Yes	4 + 2 internal	3
General purpose	TIM2	32-bit	Up, down, up/ down	Integer from 1 to 2 × 32	Yes	4	-
	TIM3	16-bit	Up, down, up/ down	Integer from 1 to 2 × 16	Yes	4	-
	TIM4	16-bit	Up, down, up/ down	Integer from 1 to 2 × 16	Yes	4	-
	TIM14	16-bit	Up	Integer from 1 to 2 × 16	No	1	-
	TIM15	16-bit	Up	Integer from 1 to 2 × 16	Yes	1	1
	TIM16 TIM17	16-bit	Up	Integer from 1 to 2 × 16	Yes	1	1
Basic	TIM6 TIM7	16-bit	Up	Integer from 1 to 2 × 16	Yes	-	-
Low-power	LPTIM1 LPTIM2	16-bit	Up	2 × n where n = 0 to 7	No	N/A	-

Table 20. **Timer instance comparison between STM32C0 series and STM32G0 series**

Feature	Time instance	STM32C0 series			STM32G0 series					
		STM32C011 STM32C031	STM32C051 STM32C071	STM32C091 STM32C092	STM32G031 STM32G041	STM32G051 STM32G061 STM32G071 STM32G081	STM32G0B1 STM32G0C1	STM32G030	STM32G050 STM32G070	STM32G0B0
Advance timer (16-bit)	TIM1	X	X	X	X[1]	X[1]	X[1]	X	X	X
General purpose (32-bit)	TIM2	-	X	X	X	X	X	-	-	-
General purpose (16-bit)	TIM3, TIM14, TIM16, TIM17	X	X	X	X	X	X	X	X	X
	TIM4	-	-	-	-	-	X	-	-	X
	TIM15	-	-	X	-	X[1]	X[1]	-	X	X
Basic	TIM6, TIM7	-	-	-	-	X	X	-	X	X
Low power	LPTIM1, LPTIM2	-	-	-	X	X	X	-	-	-

[1] *Timer with 2 × maximum CPU frequency capable*

6 Software migration

This section describes how to migrate an application based on the STM32Cube MCU package.

The STM32C0 series and STM32G0 series devices are part of the STM32Cube tool suite (STM32CubeMX, STM32CubeIDE, STM32CubeProgrammer, etc.). Both series have the same architecture and are CMSIS compliant; they use the same driver naming and the same APIs for all common peripherals. Concerning the software migration, they are using the same Cube firmware libraries methodology with HAL and LL, as with all STM32 products. Using HAL facilitates the migration between the series, while LL can be slightly different, especially for the RCC and PWR libraries.

There are two methods to do the software migration:

- Manual Library Replacement: This involves manually replacing the libraries.
- Using STM32CubeMX: This method is easier and reduces the risk of compilation errors.

The second method, using STM32CubeMX, is recommended as it simplifies the process and minimizes the potential for errors.

6.1 Software migration by replacing the libraries in hardware

To update the application code to run on the STM32C0xx library, follow the steps listed below:

1. Update the toolchain startup files:
   a. Project files: device connections and flash memory loader. These files are provided with the latest version of the toolchain that supports STM32C0xx devices. For more information, users must refer to the toolchain documentation.
   b. Linker configuration and vector table location files: templates of these files, developed following the CMSIS standard, are included in the Cube install package under the following directory: `Drivers\CMSIS\Device\ST\STM32C0xx\Source\Templates`.
2. Replace STM32C0xx library source files with the application sources:
   a. Replace the `stm32g0xx_conf.h` file with `stm32c0xx_conf.h`
   b. Replace the existing `stm32g0xx_it.c/stm32c0xx_it.h` files with `stm32c0xx_it.c/stm32c0xx_it.h`

However, the RCC and PWR parts must be manually reworked to adapt the software to the new clock tree and power scheme architecture (see dedicated part above).

Also, in the _it.c and _it.h files, the functions must be updated to the new names that can be found in the startup file.

6.2 Software migration by creating a new STM32CubeMX project

1. Create a new STM32CubeMX project with the chosen product.
   a. Pinout & configuration: configure the product according to the previous configuration (analog channel, USART).
   b. Clock configuration: choose the dedicated clock tree (system clock, peripheral clock, etc.) following the previous configuration.
   c. Project manager: in advanced settings, select the appropriate “Driver selector” based on the driver used in the previous configuration.
   d. Generate the project.
2. Open the desired IDE.
   a. Add all functions written in your previous project inside the STM32CubeMX tag (main.c, main.h, _it.c, and _it.h)
   b. Compile and run.

Some compilation errors could appear when a function is available on one product but not on the other. For example, functions linked to unlocking or locking the RTC domain are not available in the STM32C0 series.

7 Hardware development boards available

Nucleo-64 boards

These are the mainstream board designed to allow the user to learn about and evaluate the features.

They use a simple PCB that is common to all Nucleo-64 boards. This includes STLINK for chip debugging and to provide an RX-TX link between the computer and the MCU.

To help users with quick prototyping, the Nucleo board typically includes:

- Two buttons (one user button and one reset button).
- Two LEDs (one user LED and one power-up LED).

Additionally, the NUCLEO-C071RB and NUCLEO-C092RE offer added functionalities such as:

- An additional button and LED.
- A USB Type-C® connector for the full speed USB peripheral embedded inside the STM32C071 device.
- An FDCAN PHY for the FDCAN peripheral embedded inside the STM32C092 device.

It is also possible to use add-ons that are compatible with the ARDUINO® Uno and ST morpho connector.

Discovery boards

Discovery boards are more affordable compared to Nucleo boards. They are relatively simple pieces of hardware designed to test the key features of the product.

Evaluation board

The STM32 evaluation boards have been designed as a complete demonstration and development platform for the STM32 MCUs.

They include external circuitry such as transceivers, sensors, memory interfaces, displays, and many more components. The evaluation boards can be considered as a reference design for application development.

Table 21. Hardware development available on STM32C0 series

Board	STM32C011	STM32C051	STM32C051	STM32C071	STM32C091	STM32C092
Nucleo	-	NUCLEO-C031C6	NUCLEO-C051C8	NUCLEO-C071RB	-	NUCLEO-C092RC
Discovery	STM32C0116-DK	STM32C0316-DK	-	-	-	-

Table 22. Hardware development available on STM32G0 series

Board	STM32G030 STM32G031 STM32G041	STM32G050 STM32G051 STM32G061	STM32G070 STM32G071 STM32G081	STM32G0B0 STM32G0B1 STM32G0C1
Nucleo	NUCLEO-G031K8	-	NUCLEO-G071RB NUCLEO-G070RB	NUCLEO-G0B1RE
Discovery	STM32G0316-DISCO	-	STM32G071B-DISCO	-
Evaluation	-	-	STM32G081B-EVAL	STM32G0C1E-EV

Revision history

Table 23. **Document revision history**

Date	Version	Changes
28-Oct-2024	1	Initial release.

Glossary

ADC Analog-to-digital converter.

CRC Cyclic redundancy check calculation unit.

CRS Clock recovery system.

DAC Digital-to-analog converter.

DMA Direct memory access.

FDCAN FD controller area network.

GPIO General-purpose I/Os.

HSE High-speed oscillator with external crystal/ ceramic resonator or external clock source.

HSI High-speed fully-integrated RC oscillator.

I2S Integrated interchip sound.

IWDG Independent watchdog.

LPUART Low-power universal asynchronous receiver transmitter.

LSE Low-speed oscillator with external crystal/ceramic resonator or external clock source.

LSI Low-speed fully-integrated RC oscillator.

RNG Random number generator.

RTC Real-time clock.

SPI Serial peripheral interface.

UCPD USB Type-C®/USB Power Delivery.

USART Universal synchronous receiver transmitter.

USB Universal serial bus.

WWDG System window watchdog.

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